Micron Transitions to Next-Generation 3D NAND Replacement-Gate Technology

Introduction

With mobile technology advances, the explosive growth of 5G, the deluge of cloud data traffic, and the industry's appetite for solid-state drives (SSDs), the storage industry demands improved performance and increased capacity for storage and memory. NAND flash technology is being pushed to new heights in monolithic die capacity, power efficiency and throughput performance. Yet the restrictions in traditional NAND technology will eventually limit what can be achieved in best-in-class performance and capacity designs.

NAND technology demands innovation to surpass all benchmarks and create future flash technology with best-in-class performance.

Micron has overcome these barriers and transitioned from the traditional floating-gate design to 3D replacement-gate (RG) flash technology. RG NAND is an innovative storage solution that will satisfy the growing demands. With RG NAND, performance, power efficiency and capacity limitations are removed, creating a revolution in the storage-solution arena. Storage-solution customers spanning from data centers to mobile can expect robust and reliable performance with lower costs from Micron's latest innovative transformation to RG-based 3D NAND technology — now and in years to come.

Current 3D NAND Technology

3D NAND flash storage chips are composed of storage cells divided into blocks and planes. The cells have wordlines connected to allow the application of a voltage. Applying voltage to a cell creates operations known as the NAND read-and-write-program functions. The more cells on a NAND chip, the larger the storage capacity. One of the main focuses of each new NAND generation is to shrink the cell size to fit more cells in less space. 3D NAND has allowed this shrinkage by creating vertical cell stacks so that one 2D NAND cell footprint now contains x number of cells stacked vertically above it. In present-day NAND development, cell stacks have achieved 176 layers or levels of cells using TLC (three bits per cell) capabilities, with plans to extend the tier stacks even further each coming year.

NAND Cell Limitations

Technical challenges to enhance performance specifications arise as cell characteristics create cell-to-cell capacitive coupling, which leads to slower program times. The more capacitive coupling seen from one cell to

another, the more challenging the programming of the cell, which results in an increase in the time it will take to program or a reduction in performance.

Micron 3D RG NAND Technology

RG Design Innovation

Micron's 3D RG NAND flash storage creates a cell-to-cell approach that is closer to an interaction-free structure by using replacement-gate technology. The RG innovation is a nonconductive layer of silicon nitride (SiN) acting as a NAND storage cell to trap electrical charges. In 3D RG NAND, this layer surrounds the inside of the control gate of the cell, functioning as an insulator that stores charges. Figure 1 shows how this design significantly decreases the cell-to-cell capacitive coupling issues in traditional NAND that limit performance.

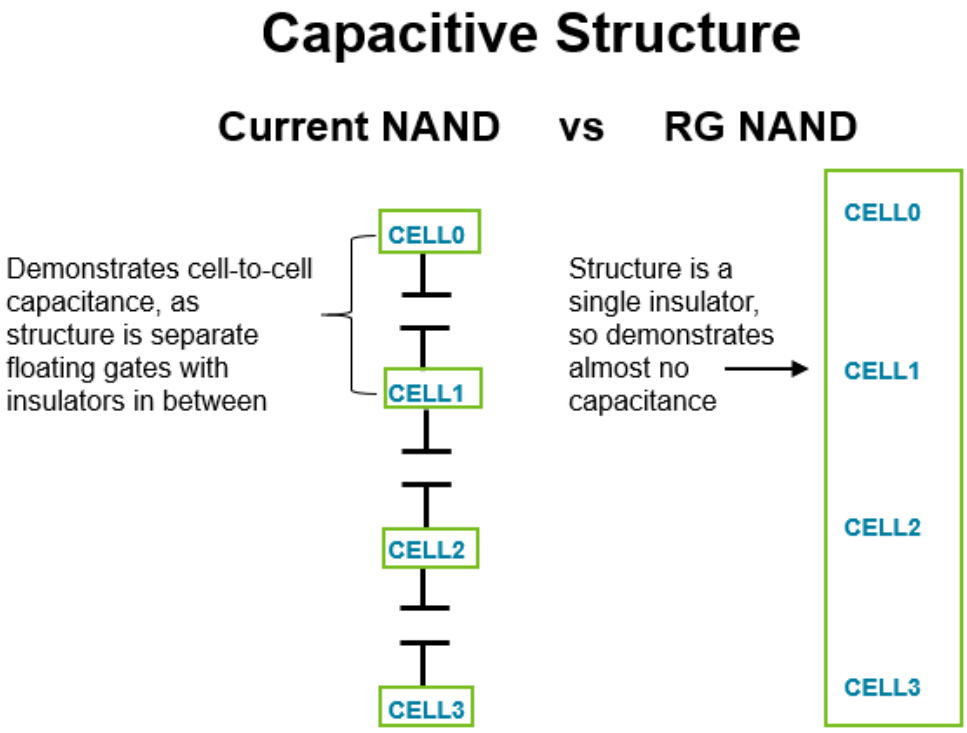

Figure 1: Current Traditional Gate NAND Capacitive Structure vs. Replacement Gate

The 3D RG NAND innovation improves NAND storage by providing:

- Higher endurance life span or capability of heavy data traffic
- Increased power efficiency to conserve energy
- Increased storage capacity
- Faster performance (write performance speed doubles the current NAND performance)

NAND flash speeds are based on the response of the cell and effectiveness of the program algorithms that write the data. Current 3D NAND flash design requires elaborate development using very complex program algorithms. These complex algorithms are required to create a more reliable programmed cell distribution that can overcome the inherent complications from cell-to-cell capacitive coupling. Unfortunately, these complex algorithms also add time delays to the cell's required program interval (creating slowdowns in the write time of the storage device). These delays have been a major downside when designing a cutting-edge data storage system.

Micron's RG 3D NAND solution significantly mitigates the cell-to-cell capacitive coupling complications seen with current NAND. A second benefit from the RG structure comes from changing the NAND control gate from polysilicon to metal, which uses a different method of etching memory cells onto the wafer.[1] Reducing resistance by using a metal control gate allows the program pulse to ramp up quickly and enables further overhead reductions in complexities of the program and the read algorithms. Using RG NAND to create new program algorithm simplifications, Micron's RG 3D NAND flash can write, read and erase up to two times faster than current 3D NAND, equipping storage systems and end users with smooth and superior performance.

Figure 2 below provides an example of how the reduction in capacitive coupling and needed program ramp time reduce program time.

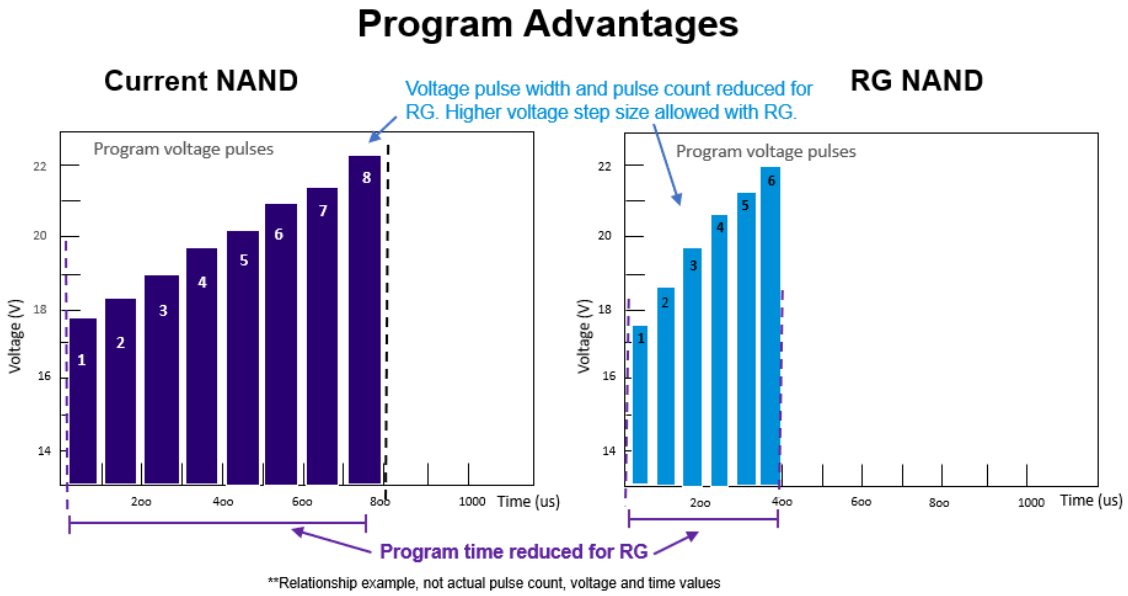

Figure 2: Comparison of Voltage Pulse Widths and Pulse Counts

Micron RG allows the NAND to reduce the electric field duration on the circuits. This can increase endurance while maintaining performance and power efficiency. The life of a NAND flash storage device is defined by the number of program cycles seen on a cell or endurance of the device. The strength and time of electric fields applied to the cell material and other NAND structures relate directly to the endurance of the NAND storage cell. The longer the electric field is applied, the more stress is created on the NAND, which reduces endurance. The innovative design of Micron's RG 3D NAND solution reduces the required time an electric field needs to be applied to the wordlines and cell structure to correctly program the NAND cells.

This RG benefit will increase endurance and enable an increase in the workload capability of a storage solution. Decreasing the electric field duration increases the life of the NAND, reducing data-storage replacement costs. Figure 3 shows the NAND circuit and voltage application. These improvements are due in part to an increase in the RG cell size and use of RG-based insulators. This RG advantage increases the VT (voltage threshold)

saturation of the cell, increasing the amount of charge the cell can store. The geometry and composition differentiation improvements in RG 3D NAND also reduce the overall cell attrition and cell-to-cell capacitive coupling complications. Through these enhancements, Micron's RG 3D NAND allows a pathway to increased endurance.

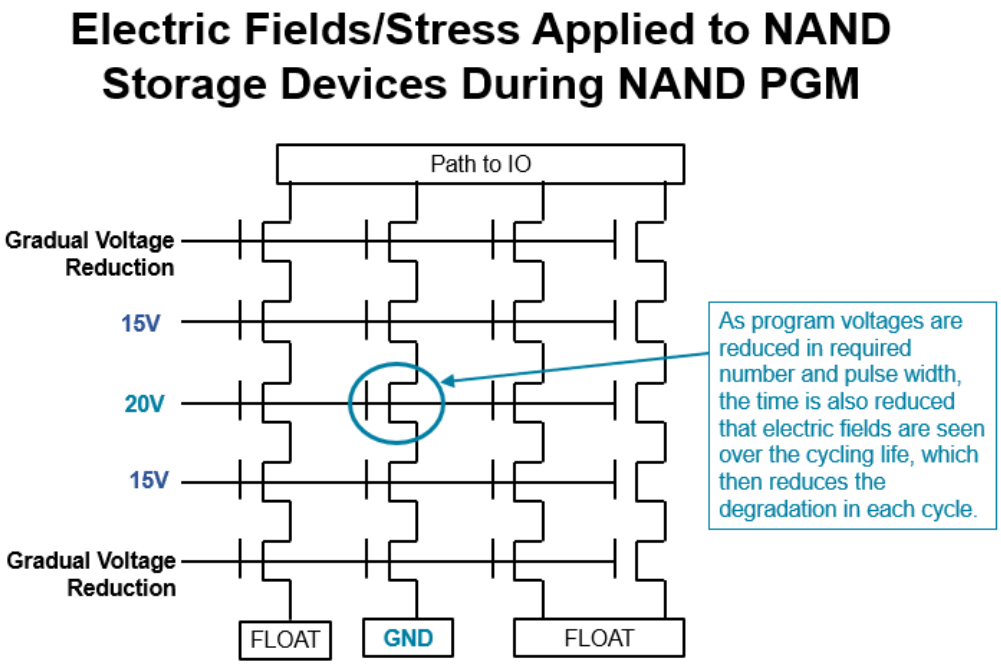

Figure 3: Reduction in Required Programming Voltage Pulses and Better Power Efficiency

Solving cell-to-cell capacitive coupling complications requires complex algorithms. Current 3D NAND supports these algorithms with an increase in programming voltage pulses. Micron's RG 3D NAND removes cell-to-cell capacitive coupling complications, which significantly reduces the number of programming pulses. Because NAND power consumption is highest when the voltage pulses are applied to the NAND cell, reducing the number of pulses makes writing data more power efficient.

RG NAND and Maximum Capacity

Cell Structure Limitations

The vertical integration of legacy 3D NAND cell layers requires technology to connect cells with one another vertically through a channel that runs through each column of the cell tiers. NAND cell geometries can affect allowable tier height due to limitations on the pillar diameter that ultimately limit the NAND structure height.

RG Capacity Innovation

3D RG NAND, in contrast, allows for a wider pillar etch that creates a pathway to even higher tier stacks and an increase in storage capacity (see Figure 4).

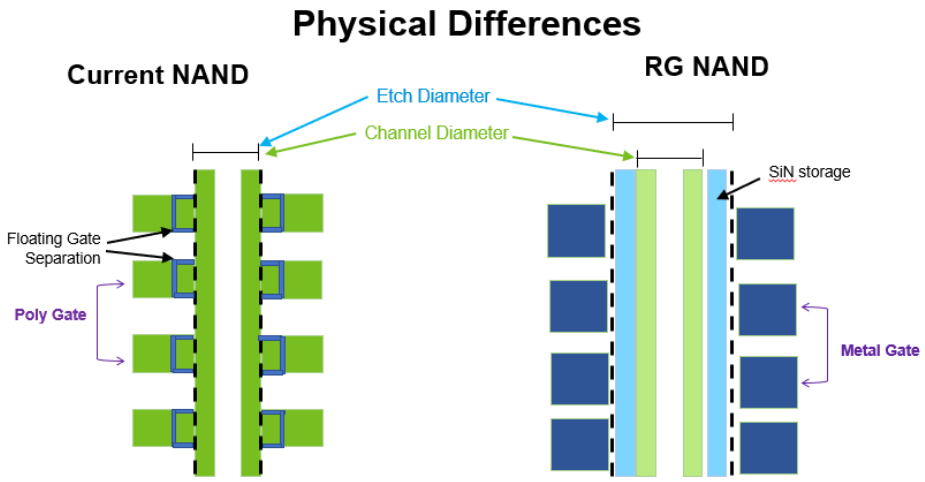

Figure 4: Higher Tier Stacks Mean More Storage Capacity

Current 3D NAND design has begun to reach the limits of its monolithic die-level maximum capacity. It will continue to fall short of the immense system-level storage capacities demanded by future data-driven applications. Cell-to-cell capacitive coupling complications and smaller etch requirements account for many of these limitations.

Micron's 3D RG NAND expands capacity by increasing the pillar etch, which enables more structural stability and creates a pathway to building higher-tier stacks. As a result, NAND storage solutions that manage heavy workloads can function at a higher level for longer periods of time by using the best-in-class capacity performance of RG NAND. This benefit will be seen in high-density, high-performance design solutions as well as in lower-density, lower-cost solutions.

Micron leads the way, with its long history in complementary metal oxide semiconductor (CMOS) manufacturing. Micron introduced CMOS under the array (CUA) to the NAND storage market, becoming a NAND market expert in CUA. The CUA process fabricates the flash memory layers on top of the logic array, so the NAND CMOS logic area no longer needs to be accommodated in the NAND memory circuit area when designing a NAND flash memory chip. NAND die size is thereby reduced in manufacturing, decreasing the overall storage capacity per unit area.

> Combining RG with Micron's industry leading CUA will provide customers with maximum NAND benefits by increasing capacity, speed, endurance and power efficiency.

As a result, 3D NAND manufacturing design gains more flexibility to increase capacity, create more innovation and enable possible cost advantages. Micron's CUA, partnered with Micron's new RG solution, provides the flash memory market with the maximum performance and flexibility needed in today's ever-increasing market demand for storage performance and capacity.

Conclusion

Current 3D NAND is hard-pressed to find pathways to improve NAND performance, power efficiency and capacity to accommodate the demands of tomorrow's best-in-class storage solutions. This difficulty is due to cell geometries and composition causing cell-to-cell capacitive coupling complications, as well as problems from smaller pillar-etch requirements. Micron's RG 3D NAND solution conquers these limitations by using an efficient design to insulate individual cells from capacitive noise, increasing write performance, and increasing power efficiency by reducing required program pulses and program pulse width. RG NAND's larger and more uniform pillar etch allows for higher stacks, increasing data density and overall storage capacity. The reduction in required program pulse count and pulse width enables NAND to reduce the overall stress time seen on devices and allows for increased endurance without reducing performance.

In summary, Micron's RG 3D NAND solution:

1. Removes stack height limitations to provide higher storage capacities.
2. Reduces the program time and algorithm complexity so that write performance and power efficiency are maximized.
3. Decreases the required electric field time to program cells, thereby increasing the endurance and lifetime of each part.
4. Aligns well with Micron's CUA to provide the flash memory market with significantly increased performance and flexibility.

Based on all that it offers, Micron's RG 3D NAND technology will become the go-to NAND silicon product for all future NAND storage system designs.

For More Information

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[1] When memory cells are etched onto a silicon wafer, it is done in bitlines, which are an array of columns, and in wordlines, which are the rows. The address of the memory cell is where the bitline and worldline intersect.