Technical Note

Micron N25Q to Micron MT25Q Migration

Introduction

This technical note provides information to help convert a system design from the Micron® N25Q Flash memory device to the Micron® MT25Q Flash memory device.

This document is written based on device information available at publication time. In case of inconsistency, information contained in the relevant N25Q or MT25Q data sheet supersedes the information in this technical note. This technical note does not provide detailed device information. The standard density specific device data sheet provides a complete description of device functionality, operating modes, and specifications.

Feature Differences

Table 1: Feature Differences

Features	N25Q	MT25Q
Densities (monolithic)	8Mb - 256Mb (This technical note covers only 128Mb to 1Gb)	128Mb - 512Mb
Densities (stacked)	512Mb (2 stack) 1Gb (4 stack)	1Gb (2 stack) 2Gb (4 stack)
Program	1 to 256 bytes	1 to 256 bytes
Sector architecture	Uniform sector (64KB)	Uniform sector (64KB)
Subsector	Uniform subsector (4KB)	Uniform subsector (4KB, 32KB)
Endurance	100,000 cycle	100,000 cycle
Retention	20 years	20 years
Industrial temperature range	–40 to +85°C	–40 to +85°C
Automotive temperature range	–40 to +125°C	–40 to +105°C

Stacked Devices

For additional details on N25Q and MT25Q stacked device features, see Micron TN-25-05: N25Q and MT25Q Serial Flash Stacked Devices.

Table 2: Stacked Devices Part Numbers and Densities

Micron Part Number	Monolithic Device Densites	Number of Stacked Devices	Stacked Device Densities
N25Q512Axxx	256Mb	2	512Mb
N25Q00AAxxx		4	1Gb
MT25Qx01Gxxx	512Mb	2	1Gb
MT25Qx02Gxxx		4	2Gb

Package Configurations

Table 3: Package Configurations

Package Name (Long)	Package Dimensions	Package Name (Short)	Part Number Code	Device Support	Density/ Voltage Support
8-pin SOP2	208 mils	SO8W	SE	Both	128Mb only
16-pin SOP2	300 mils	SO16W	SF	Both	All
24-ball T-PBGA	05/6mm x 8mm (5 x 5 array)	T-PBGA 24	12	Both	All
24-ball T-PBGA	05/6mm x 8mm (4 x 6 array)	T-PBGA 24	14	Both	MT25Q: All N25Q: 128Mb only
V-PDFN-8	6mm x 5mm Sawn (MLP8 6mm x 5mm) (F7 and W7 differ only in seated height)	DFN/6x5	F7	N25Q	128Mb
V-PDFN-8	8mm x 6mm (MLP8 8mm x 6mm) (F8 and W9 differ only in seated height)	DFN/8x6	F8	N25Q	All
W-PDFN-8	6mm x 5mm (MLP8 6mm x 5mm) (W7 and F7 differ only in seated height)	WDFN/6x5	W7	MT25Q	128Mb
W-PDFN-8	8mm x 6mm (MLP8 8mm x 6mm) (W9 and F8 differ only in seated height)	WDFN/8x6	W9	MT25Q	All
Wafer level chip-scale package	15 balls, 9 active balls	XFWLBGA 0.5P	54	MT25Q	128Mb, 1.8V
Wafer level chip-scale package	15 balls , 9 active balls	XFWLBGA 0.5P	55	MT25Q	256Mb, 1.8V
Wafer level chip-scale package	27 balls , 9 active balls	XFWLBGA 0.5P	56	MT25Q	512Mb, 1.8V

Signal Descriptions

Table 4: Signal Differences

Signals		Type	Description
N25Q	MT25Q		
S#	S#	Input	Chip select
C	C	Input	Serial clock
W#	W#	Input	Write protect, shared with DQ2
V_{PP}	-	Input	Enhanced program supply voltage, shared with DQ2
HOLD#	HOLD#	Input	HOLD or I/O, shared with DQ3
RESET#	RESET#	–	Reset, shared with DQ3 For N25Q devices: dedicated reset pin is available only for selected MPNs in 256Mb and 512Mb densities and it must be connected to an external pull-up resistor. For MT25Q devices: dedicated reset pin is available for selected MPNs in every density; it has an internal pull-up resistor and can be left unconnected if not used.
DQ[3:0]	DQ[3:0]	I/O	Serial data input or I/O
V_{CC}	V_{CC}	Input	Supply voltage
V_{SS}	V_{SS}	Input	Ground

Command and Protocol Differences

The following table shows only the differences between N25Q and MT25Q commands. For a complete list of commands, see the N25Q and MT25Q data sheets.

Table 5: N25Q and MT25Q Command Set Differences

Command	Command Code		Description
	N25Q	MT25Q	
QUAD INPUT/OUTPUT WORD READ	N/A	E7h	–
EXTENDED QUAD INPUT FAST PROGRAM	12h/38h	38h	N25Q the command code 38h is valid only for the line items that enable the dedicated RESET# pin (MPNs: N25QxxxA8xGxxxxx), otherwise, code 12h is valid; MT25Q only command code 38h is valid
4-BYTE FAST READ (DTR mode)	N/A	0Eh	–
4-BYTE DUAL INPUT/OUTPUT FAST READ (DTR mode)	N/A	BEh	–
4-BYTE QUAD INPUT/OUTPUT FAST READ (DTR mode)	N/A	EEh	–
4-BYTE QUAD INPUT EXTENDED FAST PROGRAM	N/A	3Eh	–
32KB SUBSECTOR ERASE	N/A	52h	–
BULK ERASE	C7h	C7h/60h	Applies only to monolithic devices (see the Stacked Devices Part Numbers and Densities table).
DIE ERASE	C4h	C4h	Applies only to stacked devices.
ENTER DEEP POWER DOWN	B9h	B9h	Commands available for MT25Q 3V and 1.8V devices and for N25Q 1.8V devices.
RELEASE FROM DEEP POWER DOWN	ABh	ABh	
READ SECTOR PROTECTION	N/A	2Dh	–
PROGRAM SECTOR PROTECTION	N/A	2Ch	–
4-BYTE READ VOLATILE LOCK BITS	N/A	E0h	–
4-BYTE WRITE VOLATILE LOCK BITS	N/A	E1h	–
READ NONVOLATILE LOCK BITS	N/A	E2h	–
WRITE NONVOLATILE LOCK BITS	N/A	E3h	–
ERASE NONVOLATILE LOCK BITS	N/A	E4h	–
READ GLOBAL FREEZE BIT	N/A	A7h	–
WRITE GLOBAL FREEZE BIT	N/A	A6h	–
READ PASSWORD	N/A	27h	–
WRITE PASSWORD	N/A	28h	–
UNLOCK PASSWORD	N/A	29h	–
CYCLIC REDUNDANCY CHECK	N/A	9Bh/27h	–

Table 6: N25Q and MT25Q Addressing, Transfer Rate, and Protocol Differences

STR/DTR	Protocol	Reading Pattern	Devices		Description
			N25Q	MT25Q	
STR	Extended SPI	READ, FASTREAD, DUAL OUTPUT FAST READ, DUAL INPUT/OUTPUT FAST READ, QUAD OUTPUT FAST READ, QUAD INPUT/OUTPUT FAST READ,	Yes	Yes	–
	Dual input/ output SPI	All dual input/output commands	Yes	Yes	–
	Quad input/ output SPI	All quad input/output commands	Yes	Yes	–
DTR	Extended SPI	DUAL OUTPUT FAST READ, DUAL INPUT/OUTPUT FAST READ, QUAD OUTPUT FAST READ, QUAD INPUT/OUTPUT FAST READ,	Yes	Yes	N25Q 128Mb: DTR operations are not supported. N25Q 256Mb and higher dedicated DTR commands are available allowing read operations working in DTR mode MT25Q dedicated DTR commands are available and, in addition, full DTR protocols are available to be enabled by relevant volatile or nonvolatile registers
	Dual input/ output SPI	All dual input/output commands	Yes	Yes	
	Quad input/ output SPI	All quad input/output commands	Yes	Yes	

Dummy Clock Reads

Table 7: Default Dummy Clocks – 1.8V and 3.0V

SPI Protocol	STR/DTR	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
		N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q
Extended	STR	8	8	8	8	8	8	8	8	8	10
Extended	DTR	6	6	6	6	6	6	6	6	8	8
Dual	STR	8	8	8	8	8	8	–	–	–	–
Dual	DTR	6	6	6	6	6	6	–	–	–	–
Quad	STR	10	10	–	–	–	–	10	10	10	10
Quad	DTR	8	8	–	–	–	–	8	8	8	8

Note: 1. DTR is not supported on the N25Q 128Mb device.

Table 8: STR Dummy Clock Cycles per Frequency – 1.8V

Number of Dummy Clock Cycles	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q
1	90	94	80	79	50	60	43	44	30	39
2	100	112	90	97	70	77	60	61	40	48
3	108	129	100	106	80	86	75	78	50	58
4	108	146	105	115	90	97	90	97	60	69
5	108	162	108	125	100	106	100	106	70	78
6	108	166	108	134	105	115	105	115	80	86
7	108	166	108	143	108	125	108	125	86	97
8	108	166	108	152	108	134	108	134	95	106
9	108	166	108	162	108	143	108	143	105	115
10	108	166	108	166	108	152	108	152	108	125
11	108	166	108	166	108	162	108	162	108	134
12	108	166	108	166	108	166	108	166	108	143
13	108	166	108	166	108	166	108	166	108	156
14	108	166	108	166	108	166	108	166	108	166

Table 9: STR Dummy Clock Cycles per Frequency – 3.0V

Number of Dummy Clock Cycles	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q
1	90	94	80	79	50	60	43	44	30	39
2	100	112	90	97	70	77	60	61	40	48
3	108	129	100	106	80	86	75	78	50	58
4	108	133	105	115	90	97	90	97	60	69
5	108	133	108	125	100	106	100	106	70	78
6	108	133	108	133	105	115	105	115	80	86
7	108	133	108	133	108	125	108	125	86	97
8	108	133	108	133	108	133	108	133	95	106
9	108	133	108	133	108	133	108	133	105	115
10	108	133	108	133	108	133	108	133	108	125
11:14	108	133	108	133	108	133	108	133	108	133

Table 10: DTR Dummy Clock Cycles per Frequency – 1.8V and 3.0V

Number of Dummy Clock Cycles	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q	N25Q	MT25Q
1	45	59	40	45	25	40	30	26	15	20
2	50	73	45	59	35	49	38	40	20	30
3	54	82	50	68	40	59	45	59	25	39
4	54	90	53	76	45	65	47	65	30	49
5	54	90	54	83	50	75	50	75	35	58
6	54	90	54	90	53	83	53	83	40	68
7	54	90	54	90	54	90	54	90	43	78
8	54	90	54	90	54	90	54	90	48	85
9	54	90	54	90	54	90	54	90	53	90
10:14	54	90	54	90	54	90	54	90	54	90

Serial Flash Discovery Parameter Table Differences

The following table shows only the differences between N25Q and MT25Q device SFDP information. For complete informaiton, see the N25Q and MT25Q datasheets.

Table 11: SFDP Table Differences

Description	Byte Address	Bits	N25Q	MT25Q
Parameter ID	08h:16h	7:0	FFh	Used
Sector type 3 size	50h	7:0	00h	0Fh
Sector type 3 opcode	51h	7:0	00h	52h
Flash Basic Properties	54h:6Ch		FFh	Used
4-Byte Address Command	80h:87h		FFh	Used

Electrical – DC Characteristics 1.8V

Table 12: DC Characteristics 1.8V

Parameter	Symbol	Test Conditions	N25Q		MT25Q		Units
			Typ	Max	Typ	Max	
Standby Current I_{CC1}							
128Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	14	100	12	50	µA
128Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}		N/A	20	80	µA
256Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	100	15	75	µA
256Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	N/A	20	120	µA
512Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	150	55	100	µA
512Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	N/A	55	200	µA
1Gb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	200	60	160	µA
1Gb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	N/A	60	400	µA
Deep Power-Down Current (I_{CC2}): N25Q only supports deep power-down current for 1.8V; MT25Q supports deep power-down current for 1.8V and 3.0V.							
128Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	10	2	30	µA
128Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	2	50	µA
256Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	20	2	30	µA
256Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	2	80	µA
512Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	50	2	50	µA
512Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	100	µA
1Gb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	90	5	100	µA
1Gb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	140	µA
Operating Current Fast Read (I_{CC3}): Because of different frequencies in test conditions, the MT25Q device has a maximum operating current (I_{CC3}) slightly higher than the N25Q device.							
Extended I/O 1Gb MT25Q stack: I_{CC3} = 35mA	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 166 MHz, DQ1 = open	–	15	–	20	mA
Extended I/O 1Gb MT25Q stack: I_{CC3} = 15mA		C = 0.1V_{CC}/0.9V_{CC} at 54 MHz, DQ1 = open	–	6	–	8	mA
Dual I/O 1Gb MT25Q stack: I_{CC3} = 40mA	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 166 MHz, DQ1 = open	–	18	–	25	mA
Quad I/O 1Gb MT25Q stack: I_{CC3} = 50mA	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 166 MHz STR or 80Mhz DTR, DQ1 = open	–	20	–	28	mA
Quad I/O 1Gb MT25Q stack: I_{CC3} = 55mA	I_{CC3}	MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 90Mhz DTR, DQ1 = open	–	-	–	31	mA

Table 12: DC Characteristics 1.8V (Continued)

Parameter	Symbol	Test Conditions	N25Q		MT25Q		Units
			Typ	Max	Typ	Max	
Operating Current (I_{CC4}, I_{CC5}, I_{CC6})							
Page Program	I_{CC4}	S# = V_{CC}	–	20	–	35	mA
Write Status Register	I_{CC5}	S# = V_{CC}	–	20	–	35	mA
Erase	I_{CC6}	S# = V_{CC}	–	20	–	35	mA

Electrical – DC Characteristics 3.0V

Table 13: DC Characteristics 3.0V

Parameter	Symbol	Test Conditions	N25Q		MT25Q		Units
			Typ	Max	Typ	Max	
Standby Current (I_{CC1})							
128Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	14	100	15	50	µA
128Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	14	150	30	80	µA
256Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	100	30	75	µA
256Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	250	30	120	µA
512Mb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	150	30	100	µA
512Mb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	500	30	200	µA
1Gb	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	200	60	160	µA
1Gb (automotive)	I_{CC1}	S# = V_{CC}, V_{in} = V_{SS} or V_{CC}	–	N/A	60	400	µA
Deep Power-Down Current (I_{CC2}): N25Q only supports deep power-down current for 1.8V; MT25Q supports deep power-down current for 1.8V and 3.0V.							
128Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	30	µA
128Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	50	µA
256Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	35	µA
256Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	80	µA
512Mb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	50	µA
512Mb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	100	µA
1Gb	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	100	µA
1Gb (automotive)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	N/A	5	140	µA
Operating Current Fast Read (I_{CC3}): Because of different frequencies in test conditions, the MT25Q device has a maximum operating current (I_{CC3}) slightly higher than the N25Q device.							
Extended I/O 1Gb MT25Q stack: I_{CC3} = 35mA	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 133 MHz, DQ1 = open	–	15	–	20	mA
Extended I/O 1Gb MT25Q stack: I_{CC3} = 20mA		C = 0.1V_{CC}/0.9V_{CC} at 54 MHz, DQ1 = open	–	6	–	8	mA

Table 13: DC Characteristics 3.0V (Continued)

Parameter	Symbol	Test Conditions	N25Q		MT25Q		Units
			Typ	Max	Typ	Max	
Dual I/O 1Gb MT25Q stack: I_{CC3} = 35mA	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 133 MHz, DQ1 = open	–	18	–	25	mA
Quad I/O 1Gb MT25Q stack: I_{CC3} = 45mA	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 133 MHz STR DQ1 = open	–	20	–	22	mA
Quad I/O 1Gb MT25Q stack: I_{CC3} = 50mA	I_{CC3}	N25Q: C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 80Mhz DTR, DQ1 = open	–	20	–	28	mA
Quad I/O 1Gb MT25Q stack: I_{CC3} = 55mA	I_{CC3}	MT25Q: C = 0.1V_{CC}/ 0.9V_{CC} at 90Mhz DTR, DQ1 = open	–	20	–	28	mA
Operating Current (I_{CC4}, I_{CC5}, I_{CC6})							
Page Program	I_{CC4}	S# = V_{CC}	–	20	–	35	mA
Write Status Register	I_{CC5}	S# = V_{CC}	–	20	–	35	mA
Erase	I_{CC6}	S# = V_{CC}	–	20	–	35	mA

Electrical – AC Characteristics 1.8V

Table 14: AC Specifications 1.8V

Parameter	Symbol	Transfer Rate	N25Q		MT25Q		Units
			Min	Max	Min	Max	
Clock frequency for all commands other than READ (extended-SPI, DIO-SPI, and QIO-SPI protocols)	^{f}C	STR	DC	108	DC	166	MHz
		DTR	DC	54	DC	90	MHz
Clock frequency for READ commands	^{f}R	STR	DC	54	DC	54	MHz
		DTR	DC	27	DC	27	MHz
Clock HIGH time	^{t}CH	STR	4	–	2.7	–	ns
		DTR	4	–	5	–	ns
Clock LOW time	^{t}CL	STR	4	–	2.7	–	ns
		DTR	4	–	5	–	ns
S# active setup time	$^{t}SLCH$	STR/DTR	4	–	2.7	–	ns
S# not active hold time (relative to clock)	$^{t}CHSL$	STR/DTR	4	–	2.7	–	ns
Data in setup time	$^{t}DVCH$	STR/DTR	2	–	1.75	–	ns
	$^{t}DVCL$	DTR only	-	–	1.75	–	ns

Table 14: AC Specifications 1.8V (Continued)

Parameter	Symbol	Transfer Rate	N25Q		MT25Q		Units
			Min	Max	Min	Max	
Data in hold time	^{t}CHDX	STR/DTR	3	–	2	–	ns
	^{t}CLDX	DTR only	3	–	2.75	–	ns
S# active hold time (relative to clock)	^{t}CHSH	STR	4	–	2.7	–	ns
		DTR	4	–	5	–	ns
S# active hold time (relative to clock LOW) Only for writes in DTR	^{t}CLSH	DTR only	4	–	3.375	–	ns
S# not active setup time (relative to clock)	^{t}SHCH	STR	4	–	2.7	–	ns
		DTR	4	–	5	–	ns
Output disable time	^{t}SHQZ	STR/DTR	–	8	–	6	ns
Clock low to output valid (under 30pF)	^{t}CLQV	STR/DTR	–	7	–	6	ns
Clock low to output valid (under 30pF)	^{t}CHQV	DTR only	–	8	–	6	ns
Output hold time (clock LOW)	^{t}CLQX	STR/DTR	1	-	1	-	ns
Output hold time (clock HIGH)	^{t}CHQX	DTR only	1	-	1	-	ns
HOLD setup time (relative to clock)	^{t}HLCH	STR/DTR	4	–	2.7	–	ns
HOLD hold time (relative to clock)	^{t}CHHH	STR/DTR	4	–	2.7	–	ns
HOLD setup time (relative to clock)	^{t}HHCH	STR/DTR	4	–	2.7	–	ns
HOLD hold time (relative to clock)	^{t}CHHL	STR/DTR	4	–	2.7	–	ns
HOLD to output Low-Z	^{t}HHQX	STR/DTR	-	8	-	5	ns
HOLD to output High-Z	^{t}HLQZ	STR/DTR	-	8	-	5	ns
Write protect setup time	^{t}WHSL	STR/DTR	20	–	20	–	ns
Write protect hold time	^{t}SHWL	STR/DTR	100	–	100	–	ns
Enhanced V_{PPH} HIGH to S# LOW for extended and dual I/O page program	^{t}VPPHS		200	–	–	–	ns
S# HIGH to deep power-down	^{t}DP		–	–	3	–	µs
S# HIGH to standby mode (DPD exit time)	^{t}RDP		–	–	30	–	µs

Electrical – AC Characteristics 3.0V

Table 15: AC Specifications 3.0V

Parameter	Symbol	Transfer Rate	N25Q		MT25Q		Units
			Min	Max	Min	Max	
Clock frequency for all commands other than READ (extended-SPI, DIO-SPI, and QIO-SPI protocols)	^{f}C	STR	DC	108	DC	133	MHz
		DTR	DC	54	DC	90	MHz
Clock frequency for READ commands	^{f}R	STR	DC	54	DC	54	MHz
		DTR	DC	27	DC	27	MHz
Clock HIGH time	^{t}CH	STR	4	–	3.375	–	ns
		DTR	4	–	5	–	ns
Clock LOW time	^{t}CL	STR	4	–	3.375	–	ns
		DTR	4	–	5	–	ns
S# active setup time	$^{t}SLCH$	STR/DTR	4	–	3.375	–	ns
S# not active hold time (relative to clock)	$^{t}CHSL$	STR/DTR	4	–	3.375	–	ns
Data in setup time	$^{t}DVCH$	STR	2	–	1.75	–	ns
		DTR	2	–	1.5	–	ns
	$^{t}DVCL$	DTR only	-	–	1.5	–	ns
Data in hold time	$^{t}CHDX$	STR/DTR	3	–	2.3	–	ns
	$^{t}CLDX$	DTR only	3	–	2.3	–	ns
S# active hold time (relative to clock)	$^{t}CHSH$	STR	4	–	3.375	–	ns
		DTR	4	–	5	–	ns
S# active hold time (relative to clock LOW) Only for writes in DTR	$^{t}CLSH$	DTR only	4	–	3.375	–	ns
S# not active setup time (relative to clock)	$^{t}SHCH$	STR	4	–	3.375	–	ns
		DTR	4	–	5	–	ns
Output disable time	$^{t}SHQZ$	STR/DTR	–	8	–	7	ns
Clock low to output valid (under 30pF)	$^{t}CLQV$	STR/DTR	–	7	–	6	ns
Clock low to output valid (under 30pF)	$^{t}CHQV$	DTR only	–	8	–	6	ns
Output hold time (clock LOW)	$^{t}CLQX$	STR/DTR	1	-	1.5	-	ns
Output hold time (clock HIGH)	$^{t}CHQX$	DTR only	1	-	1.5	-	ns
HOLD setup time (relative to clock)	$^{t}HLCH$	STR/DTR	4	–	3.375	–	ns
HOLD hold time (relative to clock)	$^{t}CHHH$	STR/DTR	4	–	3.375	–	ns
HOLD setup time (relative to clock)	$^{t}HHCH$	STR/DTR	4	–	3.375	–	ns
HOLD hold time (relative to clock)	$^{t}CHHL$	STR/DTR	4	–	3.375	–	ns
HOLD to output Low-Z	$^{t}HHQX$	STR/DTR	-	8	-	8	ns
HOLD to output High-Z	$^{t}HLQZ$	STR/DTR	-	8	-	8	ns
Write protect setup time	$^{t}WHSL$	STR/DTR	20	–	20	–	ns

Table 15: AC Specifications 3.0V (Continued)

Parameter	Symbol	Transfer Rate	N25Q		MT25Q		Units
			Min	Max	Min	Max	
Write protect hold time	tSHWL	STR/DTR	100	–	100	–	ns
Enhanced V_{PPH} HIGH to S# LOW for extended and dual I/O page program	tVPPHS		200	–	–	–	ns
S# HIGH to deep power-down	tDP		–	–	3	–	µs
S# HIGH to standby mode (DPD exit time)	tRDP		–	–	30	–	µs

Electrical – Write, Program, and Erase

Table 16: WRITE Cycle, PROGRAM, ERASE Times

Parameter	Symbol	N25Q		MT25Q		Units
		Typ	Max	Typ	Max	
WRITE STATUS REGISTER cycle time	tW	1.3	8	1.3	8	ms
WRITE NONVOLATILE CONFIGURATION REGISTER cycle time	tWNVCR	0.2	3	0.2	1	s
CLEAR FLAG STATUS REGISTER cycle time	tCFSR	40	–	–	–	ns
WRITE VOLATILE CONFIGURATION REGISTER cycle time	tWVCR	40	–	–	–	ns
WRITE VOLATILE ENHANCED CONFIGURATION REGISTER cycle time	tWRVECR	40	–	–	–	ns
WRITE EXTENDED ADDRESS REGISTER cycle time	tWREAR	40	–	–	–	ns
NONVOLATILE SECTOR LOCK	tPPBP	–	–	0.1	2.8	ms
PROGRAM ASP REGISTER	tASPP	–	–	0.1	0.5	ms
PROGRAM PASSWORD	tPASSP	–	–	0.2	0.8	ms
ERASE NONVOLATILE SECTOR LOCK ARRAY	tPPBE	–	–	0.2	1	s
PAGE PROGRAM (256 bytes)	tPP	0.4	5	0.2	2.8	ms
PROGRAM OTP (64 bytes)	tPOTP	0.2	–	0.12	0.8	ms
64KB SECTOR ERASE	tSE	0.6	3	0.15	1	s
4KB SECTOR ERASE	tSSE	0.25	0.8	0.05	0.4	s
32KB SUBSECTOR ERASE	tSSE	–	–	0.1	1	s
128Mb BULK ERASE	tBE	120	240	38	114	s
256Mb BULK ERASE	tBE	240	480	77	231	s
512Mb BULK ERASE DIE ERASE (N25Q, two stack device)	tBE	240	480	153	460	s

Part Numbers

Table 17: Cross-Reference Part Numbers 128Mb

N25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Description
N/A	MT25QL128ABA1ESE-MSIT	SO8 Wide	2.7V-3.6V	No	Monotonic Counter
N25Q128A13ESE40x	MT25QL128ABA1ESE-0SIT	SO8 Wide	2.7V-3.6V	No	–
N25Q128A13ESEH0E	N/A	SO8 Wide	2.7V-3.6V	Yes	–
N25Q128A13ESEA0E	N/A	SO8 Wide	2.7V-3.6V	Yes	–
N25Q128A11ESE40x	MT25QU128ABA1ESE-0SIT	SO8 Wide	1.7V-2.0V	No	–
N/A	MT25QU128ABA1ESE-MSIT	SO8 Wide	1.7V-2.0V	No	Monotonic Counter
N25Q128A13ESF40x	MT25QL128ABA8ESF-0SIT	SO16 Wide	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q)
N25Q128A13ESFH0x	MT25QL128ABA8ESF-0AAT	SO16 Wide	2.7V-3.6V	Yes	
N25Q128A13ESFA0F		SO16 Wide	2.7V-3.6V	Yes	
N25Q128A11ESF40x	MT25QU128ABA8ESF-0SIT	SO16 Wide	1.7V-2.0V	No	
N/A	MT25QU128ABA8ESF-0AAT	SO16 Wide	1.7V-2.0V	Yes	–
N25Q128A13E1240x	MT25QL128ABA8E12-0SIT	T-PBGA	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q)
N25Q128A13E1241x	MT25QL128ABA8E12-1SIT	T-PBGA	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q); Advanced security version
N25Q128A13E12A0F	MT25QL128ABA8E12-0AAT	T-PBGA	2.7V-3.6V	Yes	#RESET pin with internal pull up (MT25Q)
N/A	MT25QL128ABA8E14-0SIT	T-PBGA	2.7V-3.6V	No	–
N/A	MT25QL128ABA8E14-1SIT	T-PBGA	2.7V-3.6V	No	Advanced security version
N25Q128A11E1240x	MT25QU128ABA8E12-0SIT	T-PBGA	1.7V-2.0V	No	#RESET pin with internal pull up (MT25Q)
N25Q128A11E1241E	MT25QU128ABA8E12-1SIT	T-PBGA	1.7V-2.0V	No	#RESET pin with internal pull up (MT25Q); Advanced security version
N/A	MT25QU128ABA8E12-0AAT	T-PBGA	1.7V-2.0V	Yes	–
N/A	MT25QU128ABA8E14-0SIT	T-PBGA	1.7V-2.0V	No	–
N/A	MT25QU128ABA8E14-1SIT	T-PBGA	1.7V-2.0V	No	Advanced security version
N25Q128A13EF740x	MT25QL128ABA1EW7-0SIT	DFN-8	2.7V-3.6V	No	N25Q DFN/6x5 Sawn
N25Q128A13EF840x	MT25QL128ABA1EW9-0SIT	DFN-8	2.7V-3.6V	No	–
N25Q128A13EF8A0F	N/A	DFN-8	2.7V-3.6V	Yes	–
N/A	MT25QL128ABA1EW7-MSIT	DFN-8	2.7V-3.6V	No	Monotonic Counter
N/A	MT25QU128ABA1EW7-MSIT	DFN-8	1.7V-2.0V	No	Monotonic Counter
N25Q128A11EF740x	MT25QU128ABA1EW7-0SIT	DFN-8	1.7V-2.0V	No	N25Q DFN/6x5 Sawn
N25Q128A11EF840x	MT25QU128ABA1EW9-0SIT	DFN-8	1.7V-2.0V	No	–
N/A	MT25QU128ABA8E54-0SIT	XFWLBGA 0.5P	1.7V-2.0V	No	–

Table 18: Cross-Reference Part Numbers 256Mb

N25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Description
N25Q256A13ESF40x	MT25QL256ABA8ESF-0SIT	SO16 Wide	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q)
N25Q256A83ESF40x		SO16 Wide	2.7V-3.6V	No	–
N25Q256A73ESF40x	N/A	SO16 Wide	2.7V-3.6V	No	–
N/A	MT25QL256ABA8ESF-MSIT	SO16 Wide	2.7V-3.6V	No	Monotonic Counter
N25Q256A83ESFH0F	MT25QL256ABA8ESF-0AAT	SO16 Wide	2.7V-3.6V	Yes	–
N25Q256A83ESFA0F		SO16 Wide	2.7V-3.6V	Yes	–
N25Q256A11ESF40x	MT25QU256ABA8ESF-0SIT	SO16 Wide	1.7V-2.0V	No	#RESET pin with internal pull up (MT25Q)
N25Q256A81ESF40x		SO16 Wide	1.7V-2.0V	No	–
N/A	MT25QU256ABA8ESF-0AAT	SO16 Wide	1.7V-2.0V	Yes	–
N/A	MT25QU256ABA8ESF-MSIT	SO16 Wide	1.7V-2.0V	No	Monotonic Counter
N25Q256A13E1240x	MT25QL256ABA8E12-1SIT	T-PBGA	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q); Advanced security version
N25Q256A83E1240x		T-PBGA	2.7V-3.6V	No	Advanced security version
N25Q256A13E1241x		T-PBGA	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q); Advanced security version
N/A	MT25QL256ABA8E14-1SIT	T-PBGA	2.7V-3.6V	No	Advanced security version
N25Q256A13E12A0F	MT25QL256ABA8E12-0AAT	T-PBGA	2.7V-3.6V	Yes	
N25Q256A11E1240x	MT25QU256ABA8E12-1SIT	T-PBGA	1.7V-2.0V	No	Advanced security version3
N/A	MT25QU256ABA8E14-1SIT	T-PBGA	1.7V-2.0V	No	
N/A	MT25QU256ABA8E12-0AAT	T-PBGA	1.7V-2.0V	Yes	–
N25Q256A13EF840x	MT25QL256ABA1EW9-0SIT	DFN-8	2.7V-3.6V	No	–
N/A	MT25QL256ABA1EW7-0SIT	DFN-8	2.7V-3.6V	No	–
N25Q256A13EF8A0F	MT25QL256ABA1EW9-0AAT	DFN-8	2.7V-3.6V	Yes	–
N25Q256A11EF840x	MT25QU256ABA1EW9-0SIT	DFN-8	1.7V-2.0V	No	–
N/A	MT25QU256ABA1EW7-0SIT	DFN-8	1.7V-2.0V	No	–
N/A	MT25QU256ABA8E55-0SIT	XFWLBGA 0.5P	1.7V-2.0V	No	–

Table 19: Cross-Reference Part Numbers 512Mb

N25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Description
N25Q512A13GSF40x	MT25QL512ABB8ESF-0SIT	SO16 Wide	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q)
N25Q512A83GSF40x		SO16 Wide	2.7V-3.6V	No	–
N25Q512A13GSFA0F	MT25QL512ABB8ESF-0AAT	SO16 Wide	2.7V-3.6V	Yes	#RESET pin with internal pull up (MT25Q)
N25Q512A13GSFH0E		SO16 Wide	2.7V-3.6V	Yes	
N25Q512A83GSFA0F		SO16 Wide	2.7V-3.6V	Yes	–
N25Q512A11GSF40x	MT25QU512ABB8ESF-0SIT	SO16 Wide	1.7V-2.0V	No	#RESET pin with internal pull up (MT25Q)
N25Q512A81GSF40x		SO16 Wide	1.7V-2.0V	No	–
N/A	MT25QU512ABB8ESF-0AAT	SO16 Wide	1.7V-2.0V	Yes	–
N25Q512A13G1240x	MT25QL512ABB8E12-0SIT	T-PBGA	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q)
N25Q512A83G1240x		T-PBGA	2.7V-3.6V	No	–
N25Q512A13G12A0F	MT25QL512ABB8E12-0AAT	T-PBGA	2.7V-3.6V	Yes	#RESET pin with internal pull up (MT25Q)
N25Q512A13G12H0F		T-PBGA	2.7V-3.6V	Yes	
N25Q512A11G1240x	MT25QU512ABB8E12-0SIT	T-PBGA	1.7V-2.0V	No	
N/A	MT25QU512ABB8E12-0AAT	T-PBGA	1.7V-2.0V	Yes	–
N25Q512A13GF840x	MT25QL512ABB1EW9-0SIT	DFN-8	2.7V-3.6V	No	–
N/A	MT25QU512ABB1EW9-0SIT	DFN-8	1.7V-2.0V	No	–
N/A	MT25QU512ABB8E56-0SIT	XFWLBGA 0.5P	1.7V-2.0V	No	–

Table 20: Cross-Reference Part Numbers 1Gb

N25Q Part Number	MT25Q Part Number	Package	Voltage	Auto	Description
N25Q00AA13GSF40x	MT25QL01GBBB8ESF-0SIT	SO16 Wide	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q)
N/A	MT25QL01GBBB8ESF-0AAT	SO16 Wide	2.7V-3.6V	Yes	–
N25Q00AA11GSF40x	MT25QU01GBBB8ESF-0SIT	SO16 Wide	1.7V-2.0V	No	#RESET pin with internal pull up (MT25Q)
N/A	MT25QU01GBBB8ESF-0AAT	SO16 Wide	1.7V-2.0V	Yes	–
N25Q00AA13G1240x	MT25QL01GBBB8E12-0SIT	T-PBGA	2.7V-3.6V	No	#RESET pin with internal pull up (MT25Q)
N/A	MT25QL01GBBB8E12-1SIT	T-PBGA	2.7V-3.6V	No	Advanced security version
N/A	MT25QL01GBBB8E12-0AAT	T-PBGA	2.7V-3.6V	Yes	–
N25Q00AA11G1240x	MT25QU01GBBB8E12-0SIT	T-PBGA	1.7V-2.0V	No	#RESET pin with internal pull up (MT25Q)
N/A	MT25QL01GBBB1EW9-0SIT	DFN-8	2.7V-3.6V	No	–
N/A	MT25QU01GBBB1EW9-0SIT	DFN-8	1.7V-2.0V	No	–

Revision History

Rev. E – 11/17

- Added commands and notes to tables under Protocols, Commands, Addressing, and Transfer Rate heading
- Reformatted to adhere more closely to Micron style and format

Rev. D – 05/17

- Review command table
- Adjust table Write Cycle, PROGRAM, ERASE Times

Rev. C – 09/16

- Fixed a table column spacing inconsistency

Rev. B – 08/16

- Correct tables: STR: Minimum Number of Dummy Cycles Required per Each Frequency, DTR: Minimum Number of Dummy Cycles Required per Each Frequency, and DC Characteristics
- Review registers consideration
- Review command and SFDP table (only differences)
- Updated Max DTR frequency to 90MHz for MT25Q
- Updated Part Numbers tables

Rev. A – 06/13

- Initial release

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