Technical Note

Migrating from Micron M29EW Devices to MT28EW NOR Flash Devices

Introduction

This technical note describes the process for converting a system design from the Micron® M29EW devices to MT28EW single-level cell NOR Flash devices, including 128Mb, 256Mb, 512Mb, and 1Gb densities. The MT28EW higher reliability and performance are ensured through the advanced technology and product design improvements. MT28EW features a large buffer size up to 512 words for advanced program performance. Erase performance is largely improved to meet all variable system design considerations. Moreover, MT28EW supports both x8 and x16 data bus for legacy controllers compatibility. This document was written based on device information available at publication time. In case of inconsistency, information contained in the relevant MT28EW data sheet supersedes the information in this technical note.

This technical note does not provide detailed device information. The standard density-specific device data sheet provides a complete description of device functionality, operating modes, and specifications.

Comparative Overview

The MT28EW is compatible with the M29EW 128Mb, 256Mb, 512Mb, and 1Gb devices, but features superior program and erase performance.

Table 1: Part Number Comparison

Density	Package Type	Part Number	
		MT28EW	M29EW
1Gb	56-pin TSOP (14mm x 20mm)	MT28EW01GABA1HJS-0SIT	JS28F00AM29EWHA
			JS28F00AM29EWHB
			JS28F00AM29EWHE
		MT28EW01GABA1LJS-0SIT	JS28F00AM29EWLA
	64-ball LBGA (11mm x 13mm)	MT28EW01GABA1HPC-0SIT	PC28F00AM29EWHA
			PC28F00AM29EWHB
		MT28EW01GABA1LPC-0SIT	PC28F00AM29EWLA
		MT28EW01GABA1LPC-1SIT	PC28F00AM29EWLD
			PC28F00AM29EWLE
512Mb	56-pin TSOP (14mm x 20mm)	MT28EW512ABA1HJS-0SIT	JS28F512M29EWHA
			JS28F512M29EWHB
		MT28EW512ABA1LJS-0SIT	JS28F512M29EWLA
			JS28F512M29EWLB
			JS28F512M29EWLD
	64-ball LBGA (11mm x 13mm)	MT28EW512ABA1HPC-0SIT	PC28F512M29EWHD
			PC28F512M29EWHB
			PC28F512M29EWHG
		MT28EW512ABA1HPC-1SIT	PC28F512M29EWHA
			PC28F512M29EWHE
		MT28EW512ABA1LPC-0SIT	PC28F512M29EWLA
			PC28F512M29EWLB
256Mb	56-pin TSOP (14mm x 20mm)	MT28EW256ABA1HJS-0SIT	JS28F256M29EWHA
			JS28F256M29EWHB
			JS28F256M29EWHD
		MT28EW256ABA1LJS-0SIT	JS28F256M29EWLA
			JS28F256M29EWLB
	64-ball LBGA (11mm x 13mm)	MT28EW256ABA1HPC-0SIT	PC28F256M29EWHA
		MT28EW256ABA1HPC-1SIT	PC28F256M29EWHD
		MT28EW256ABA1LPC-0SIT	PC28F256M29EWLB

Table 1: Part Number Comparison (Continued)

Density	Package Type	Part Number	
		MT28EW	M29EW
128Mb	56-pin TSOP (14mm x 20mm)	MT28EW128ABA1HJS-0SIT	JS28F128M29EWHF
		MT28EW128ABA1LJS-0SIT	JS28F128M29EWLA
	64-ball LBGA (11mm x 13mm)	MT28EW128ABA1HPC-0SIT	PC28F128M29EWHF
		MT28EW128ABA1HPC-1SIT	PC28F128M29EWHX
		MT28EW128ABA1LPC-0SIT	PC28F128M29EWLA
		MT28EW128ABA1LPC-1SIT	PC28F128M29EWLX

Notes:
1. For valid combination details, refer to www.micron.com/products, or contact Micron sales representatives.
2. Unlike M29EW, packing types, including tray, and tape and reel, are not indicated in Micron's MT28EW MPN. Contact Micron sales representatives for detail information.

Table 2: Features Comparison

Feature	MT28EW	M29EW	Notes
Process technology	45nm single-level cell (SLC) floating gate	65nm multi-level cell (MLC) floating gate	1
Density	128Mb 256Mb 512Mb 1Gb –	128Mb 256Mb 512Mb 1Gb 2Gb (stacked)	
Package	64-ball LBGA (11mm x 13mm), 56-pin TSOP (14mm x 20mm)	64-ball LBGA (11mm x 13mm), 56-pin TSOP (14mm x 20mm)	2
Block architecture	Uniform 128KB	Uniform 128KB	
Data bus	x8/x16	x8/x16	
Page read size	16 words	16 words	3
Extended memory block	128 words (8 + 120)	128 words (8 + 120)	
Program write buffer size	256-byte (x8 mode) 512-word (x16 mode)	256-byte (x8 mode) 512-word (x16 mode)	4
V_{CC} range	2.7V to 3.6V	2.7V to 3.6V	
V_{CCQ} range	1.65~V_{CC}	1.65~V_{CC}	
V_{PP} accelerated (TYP)	9V	12V	
CFI version	1.3	1.3	
High voltage auto select (A9)	No	No	5
Individual block write protection	Yes	Yes	
Permanent block locking (OTP block)	Yes	Yes	
Hardware protection	Yes	Yes	
Unlock bypass	Yes	Yes	
Chip erase	Yes	Yes	
RY/BY# pin	Yes	Yes	
Blank check	Yes	Yes	6
Multiblock erase	Yes	Yes	
Data polling	Yes	Yes	
EFI CRC	Yes	No	

Notes:
1. MT28EW SLC floating-gate technology provides improved performance and optimized quality and reliability. M29EW 128M is also processed with SLC technology.
2. MT28EW package is RoHS-compliant and halogen-free. For the M29EW 2Gb density, only the 64-ball BGA package is available.
3. On M29EW 128Mb device, the read page size is 8 words or 16 bytes.
4. To configure MT28EW device software, query CFI word address 2Ah (×16)/54h (×8) on the buffer size option, in either ×8 or ×16 mode. However, M29EW supports query CFI

2Ah in ×16 mode only. To configure M29EW under ×8 mode, refer to TN-13-07 for detail patch.

On M29EW 128Mb device, the maximum buffer programming size is 256 words (×16) or 256 bytes (×8).

5. To prevent damaging the device, designs applying V_{PP}/WP# voltages higher than 9.5V (MAX) should be modified. V_{PP}/WP# should not remain at V_{PPH} for more than 80 hours cumulative.
6. Refer to the data sheet for detailed BLANK CHECK command sets.

Hardware and Mechanical Considerations

Packages and Ballouts

The MT28EW device is available in 56-pin TSOP and 64-ball LBGA packages, both lead-free. The pin and ball assignments and the physical dimensions are compatible with the M29EW.

On the M29EW 64-ball LBGA package, ball B1 (labeled A26) is used to access the 1Gb/1Gb stacked die. MT28EW is not available for 2G device. On the 56-pin TSOP package, pin 28 is reserved for addressing in future 2Gb devices.

Signals

Table 3: Signal Comparison

MT28EW and M29EW	Type	Description	Notes
A[MAX:0]	Input	Address inputs	
BYTE#	Input	Byte/Word organization select cannot be floated	
CE#	Input	Chip enable	
OE#	Input	Output enable	
RST#	Input	Reset	
WE#	Input	Write enable	
V_{PP}/WP#	Input	Acceleration power/write protect input	1
DQ15/A-1	I/O or Input	Data input/output or address input	
DQ[14:8]	I/O	Data inputs/outputs	
DQ[7:0]	I/O	Data inputs/outputs	
RY/BY#	Output	Ready/Busy	
V_{CC}	Supply	Supply voltage	
V_{CCQ}	Supply	Input/Output buffer supply voltage	
V_{SS}	–	Ground	
NC	–	No connect	

Note: 1. V_{PP}/WP# could be tied to V_{CCQ} or left floating on MT28EW device if it is not used on system design.

Input/Output Capacitance

Table 4: Input/Output Capacitance Comparison

Parameter	MT28EW		M29EW		Unit
	Min	Max	Min	Max	
C_{IN}	3	11	4	9	pF
C_{OUT}	3	7	3	6	pF

Note: 1. This is a comparison table taking an example of 1Gb density.

Power Supply Decoupling

Flash memory devices require careful power supply decoupling to prevent external transient noise from affecting device operations, and to prevent internally generated transient noise from affecting other devices in the system.

Ceramic chip capacitors of 0.01µF to 0.1µF should be used between each V_{CC}, V_{CCQ}, and V_{PP} supply connection or system ground pin. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the device package, or on the opposite side of the printed circuit board close to the center of the device package footprint.

Larger electrolytic or tantulum bulk capacitors (4.7µF to 33.0µF) should also be distributed as needed throughout the system to compensate for voltage sags and surges caused by circuit trace inductance.

Transient current magnitudes depend on the capacitive and inductive loading on the device's outputs. For best signal integrity and device performance, high-speed design rules should be used when designing the printed-circuit board. Final signal reflections (overshoot and undershoot) may vary by each system.

Software Considerations

Command Set

The MT28EW command set is fully compatible with M29EW; therefore, no command change in the software is required. MT28EW provides some unique commands to support enhanced features such as EFI CRC functions.

Manufacturer ID and Auto Select Comparison

The auto select information of MT28EW is fully compatible with M29EW. There should be no any software modification on the system design.

To obtain the device ID of the secure version of MT28EW and M29EW devices, contact your local Micron sales offices for the Security Addendum.

Table 5: Auto Select Comparison – Word Mode

Address	Description	MT28EW	M29EW
(Base) + 00h	**Manufacturer ID**		
	–	0089h	0089h
(Base) + 01h	**Device ID (cycle 1)**		
	–	227Eh	227Eh
(Base) + 0Eh	**Device ID (cycle 2)**		
	128Mb	2221h	2221h
	256Mb	2222h	2222h
	512Mb	2223h	2223h
	1Gb	2228h	2228h
	2Gb	–	2248h
(Base) + 0Fh	**Device ID (cycle 3)**		
	–	2201h	2201h
(Base) + 03h	**Protection register indicator – V_{PP}/WP# locks highest block**		
	Factory locked	0099h	0099h
	Factory unlocked	0019h	0019h
	Protection register indicator – V_{PP}/WP# locks lowest block		
	Factory locked	0089h	0089h
	Factory unlocked	0009h	0009h
(Base) + 02h	**Block protection**		
	Protected	0001h	0001h
	Unprotected	0000h	0000h

CFI Comparison

M29EW and MT28EW CFI differences exist because of the different device performance characteristics. MT28EW supports asynchronous single-word and page mode READ operations while M29EW supports only asynchronous single-word mode on CFI storage area.

Table 6: CFI Comparison

Address (x16)	Description	MT28EW	MT29EW		Notes
		128Mb–1Gb	256Mb–2Gb	128Mb	
1Dh	**V_{PPH} (programming) supply minimum**				
	Bits[7:4] hex value in volts	0085	00B5	00B5	–
	Bits[3:0] BCD value in 100mV				
1Eh	**V_{PPH} (programming) supply maximum PROGRAM/ERASE voltage**				
	Bits[7:4] hex value in volts	0095	00C5	00C5	–
	Bits[3:0] BCD value in 100mV				
1Fh	**Typical timeout for single byte/word PROGRAM = 2^nµs**				
	–	0005	0009	0004	–
20h	**Typical timeout for maximum size BUFFER PROGRAM = 2^nµs**				
	–	0009	000A	0009	–
21h	**Typical timeout for individual BLOCK ERASE = 2^nms**				
	–	0008	000A	0009	–
22h	**Typical timeout for full-chip ERASE = 2^nms**				
	128Mb	000F	–	0011	–
	256Mb	0010	0012	–	
	512Mb	0011	0013	–	
	1Gb	0012	0014	–	
	2Gb	–	0015	–	
23h	**Maximum timeout for byte/word PROGRAM = 2^n times typical timeout**				
	–	0003	0001	0004	–
24h	**Maximum timeout for BUFFER PROGRAM = 2^n times typical timeout**				
	–	0002	0002	0002	–
25h	**Maximum timeout per individual BLOCK ERASE = 2^n times typical timeout**				
	–	0003	0002	0003	–
26h	**Maximum timeout for chip ERASE = 2^n times typical timeout**				
	–	0003	0002	0002	–
2Ah	**Maximum number of bytes in multiple-byte write = 2^n**				
	x8 mode	08	000A	0008	1
	x16 mode	000A			
45h	**Address-sensitive unlock (bits[1:0])**				
	0 = required, 1 = not required	0018	0018	0018	–
	Silicon revision number (bits[7:2])				
4Ch	**Page mode**				
	00 = not supported	0003	0003	0002	–
	01 = 4-word page				
	02 = 8-word page				
	03 = 16-word page				

Table 6: CFI Comparison (Continued)

Address (x16)	Description	MT28EW	MT29EW		Notes
		128Mb–1Gb	256Mb–2Gb	128Mb	
4Dh	**V_{PPH} supply minimum PROGRAM/ERASE voltage**				
	Bits[7:4] hex value in volts	0085h	00B5h	00B5h	–
	Bits[3:0] BCD value in 100mV				
4Eh	**V_{PPH} supply maximum PROGRAM/ERASE voltage**				
	Bits[7:4] hex value in volts	0095h	00C5h	00C5h	–
	Bits[3:0] BCD value in 100mV				

Note: 1. On MT28EW, the query result from 2Ah is modulated by BYTE# status for x8 and x16 modes, and designs can query the address to get the proper maximum buffer size. On M29EW (256Mb–2Gb), designs must port a software patch to get the correct buffer size for x8 mode. Refer to TN-13-07 for detail patch.

Performance Comparison

The MT28EW features significantly improved program and erase performance.

Table 7: Program and Erase Performance Comparison (Word Mode)

Parameter	MT28EW		M29EW				Unit
			256Mb–2Gb		128Mb		
	Typ	Max	Typ	Max	Typ	Max	
Block Erase							
Block erase	200	1100	500	3500	500	4000	ms
Chip Erase							
Accelerated chip erase (512Mb)	95	–	–	–	–	–	s
128Mb	26	–	–	–	25	–	
256Mb	52	–	128	–	–	–	
512Mb	104	–	256	–	–	–	
1Gb	208	–	512	–	–	–	
Program/Erase Suspend							
Erase suspend latency time	–	20	–	32	–	20	µs
Program suspend latency time	–	15	–	32	–	25	
Erase/Program or suspend to next resume (^{t}RES *1)	100	–	500	–	500	–	
Program, x16							

Table 7: Program and Erase Performance Comparison (Word Mode) (Continued)

Parameter	MT28EW		M29EW				Unit
			256Mb–2Gb		128Mb		
	Typ	Max	Typ	Max	Typ	Max	
Single word	25	200	210	456	15	175	µs
Write-to-buffer (32 words)	92 (0.7 MB/s)	460	270 (0.2 MB/s)	716	85 (0.8 MB/s)	200	
Write-to-buffer (64 words)	117 (1.1 MB/s)	600	310 (0.4 MB/s)	900	107 (1.2 MB/s)	450	
Write-to-buffer (128 words)	171 (1.5 MB/s)	900	375 (0.7 MB/s)	1140	160 (1.6 MB/s)	710	
Write-to-buffer (256 words)	285 (1.8 MB/s)	1500	505 (1.0 MB/s)	1690	284 (1.8 MB/s)	1280	
Write-to-buffer (512 words)	512 (2.0 MB/s)	2000	900 (1.1 MB/s)	3016	–	–	
Accelerated full buffered program	410 (2.5 MB/s)	–	–	–	–	–	
Set Nonvolatile Protection Bit Time							
Set nonvolatile protection bit time	25	200	150	456	50	60	µs
Clear nonvolatile protection bit time	80	1100	800	4000	500	1000	ms
Blank Check							
Blank check: main block	3.2	–	3.2	–	3.2	–	ms

Note: 1. This typical value allows an ERASE operation to progress to completion. It is important to note that the algorithm might never finish if the ERASE operation is always suspended less than this specification.

Table 8: Read AC Performance Comparison – 3V

Parameter	Symbol		MT28EW		M29EW				Unit	Notes
					256Mb–2Gb		128Mb			
	Legacy	JEDEC	Min	Max	Min	Max	Min	Max		
Address valid to output valid	^{t}ACC	^{t}AVQV	–	95/70	–	100–110	–	60/70	ns	1
Page address access	^{t}APA	–	–	20	–	25	–	25	ns	
OE# LOW to output valid	^{t}OE	^{t}GLQV	–	25	–	25	–	25	ns	

Note: 1. For MT28EW, 70ns spec is available only for 128Mb/256Mb.

Table 9: Power Consumption Comparison

Parameter		Symbol	MT28EW		M29EW				Unit
					256Mb–2Gb		128Mb		
			Typ	Max	Typ	Max	Typ	Max	
Read									
V_{CC} random read current		I_{CC1}	26	31	26	31	20	25	mA
V_{CC} page read curent		I_{CC1}	12	16	12	16	12	16	
Standby									
V_{CC} standby current	1Gb	I_{CC2}	70	150	75	240	–	–	µA
	512Mb		65	136	70	225	–	–	
	256Mb		50	120	65	210	–	–	
	128Mb		–	–	–	–	50	120	
Program/Erase									
V_{CC} erase current		I_{CC3}	35	50	35	50	35	50	mA
V_{CC} program current		I_{CC3}	35	50	35	50	35	50	

Power-on and Reset Timings

Because many of the more common processors support the MT28EW timings, there should be no adverse effect from timing differences.

Table 10: Reset Timing Comparison

Condition/Parameter	Symbol		MT28EW		M29EW				Unit
					256Mb–2Gb		128Mb		
	Legacy	JEDEC	Min	Max	Min	Max	Min	Max	
V_{CC} power valid to RST# HIGH	^{t}VCS	^{t}VCHPH	300	–	300	–	60	–	µs
RST# LOW to read mode during program or erase	^{t}READY	^{t}PLRH	–	25	–	32	–	25	µs
RST# pulse width	^{t}RP	^{t}PLPH	100	–	100	–	100	–	ns
RST# HIGH to CE# LOW, OE# LOW	^{t}RH	^{t}PHEL, ^{t}PHGL	50	–	50	–	50	–	ns
RY/BY# HIGH to CE# LOW, OE# LOW	^{t}RB	^{t}RHEL, ^{t}RHGL	0	–	0	–	0	–	ns
RST# HIGH to WE# LOW	–	^{t}PHWL	–	–	150	–	150	–	ns
Low V_{CC} lock-out voltage	V_{LKO}	–	2.0	–	2.3	–	2.3	–	V

Note: 1. During power-down or voltage drops below V_{CC}_min on the M29EW device, V_{CC} and V_{CCQ} must drop below the V_{IL} voltage to initialize correctly when V_{CC} and V_{IO} rise again to their operating ranges. Otherwise, M29EW may require longer ^{t}VCS for the first access operation when power supply is recovered. A complete initialization (^{t}VCS) is needed on MT28EW device when the device is powered up from a voltage below the normal operating range.

System Validation

Because Linux is a widely used operating system in the embedded application, system-level validations have been performed with the following environment on Micron MT28EW 128Mb, 256Mb, 512Mb, and 1Gb devices.

- ARM9, 3.3V, x16 I/O, CPU: 202.8 MHz
- Memory bus clock: 101.4 MHz
- Linux version: 2.6.22 and 3.11.6, HZ = 200
- File system: JFFS2 and UBIFS

MTD Validation

The basic functions and stress tests applied by Linux MTD driver have been performed with Linux test project (LTD) utility. It demonstrates robust compatibility and good performance.

Table 11: Typical Write Speed Comparison

Size	MT28EW	M29EW	Unit
10KB	1.9	1.0	MB/s
100KB	2.3	1.1	
1MB	2.4	1.1	
4MB	2.4	1.1	

Notes:
1. It is measured through the function that time dd if=/dev/zero of=/dev/mtd0 bs=1k count=10/100/1000/4000 conv=sync. The performance is subject to change by different system application.
2. The typical data is measured on limited samples. MTD driver includes a typical delay time probed from CFI 1Fh (x16) after the Flash WRITE operation kicks off.

Table 12: Typical Format Speed

Format		Size	MT28EW	M29EW	Unit
JFFS2	Blank Flash	16MB	17.3	66.6	s
		32MB	34.6	133.2	
	100% Dirty Flash	16MB	19.6	100.9	
		32MB	37.1	197.4	
UBIFS	Blank Flash	16MB	17.9	67.3	
		32MB	34.7	134.1	
	100% Dirty Flash	16MB	19.8	104.6	
		32MB	37.3	202.8	

Notes:
1. It is measured through the function that time flash_eraseall –jq /dev/mtd0;time ubiformat –yq /dev/mtd0. The system performance is subject to change by different system application.
2. The typical data is measured on limited samples. MTD driver includes a typical delay time after the Flash ERASE operation kicks off; namely half of the time-value probed from CFI 21h (x16). It mediates the performance advantage of MT28EW on blank Flash formatting.

File System Validation

All file operations including READ, WRITE, DELETE, and partitions, including FORMAT, MOUNT, and UNMOUNT have been validated on both the JFFS2 and the UBIFS file system.

Stress Tests

Stress reliability test is performed to validate the power loss cycling more than 40,000 times on both chip level and system level. ERASE SUSPEND operation is stressed up to 40,000 cycles. All subsequent READ, WORD PROGRAM, and BUFFER PROGRAM operations after an ERASE SUSPEND command could work successfully.

Related Information

Table 13: Document List

Document/Tool
Parallel NOR Flash Embedded Memory MT28EW datasheet (all densities)
TN-13-12: Software Driver for M29EW NOR Flash Memory
Application Note 309046: Power Loss Recovery for NOR Flash Memory
TN-13-30: System Design Considerations with Micron Flash Memory
TN-13-07: Patching the Linux Kernel and U-Boot for Micron M29 Flash Memory

Notes:
1. Contact your local Micron or distribution sales office to request additional documentation.
2. Visit www.micron.com for technical documentation.

Revision History

Rev. A – 9/14

- Initial release

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