Technical Note

Design Considerations when using NOR Flash on PCBs

Introduction and Definitions

Table 1: Definitions

Term	Definition
Power vias and thermals	Power vias accommodate high current connections to ground or power planes. Compared to signal vias, power vias have a larger diameter, and use more metal for the power or ground connection. Power vias use thermals, and as shown in the figure below, a mask isolates portions of the via from the plane, preventing excessive heat dissipation during soldering.
Equivalent series resistance (ESR)	Equivalent series resistance (ESR) is the high frequency component of the resistance that appears in the capacitor. ESR is not pure resistance and decreases with increasing frequency.
Stripline	A stripline is a trace embedded in a dielectric material, sandwiched between two reference planes.
Via	A small hole drilled in a printed circuit board used to connect layers. Traces are connected to the via.

Figure 1: Thermal

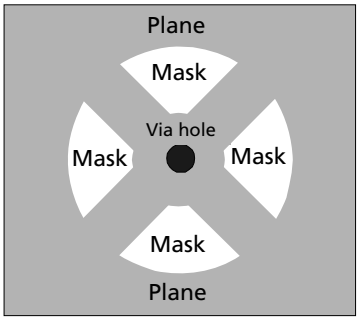
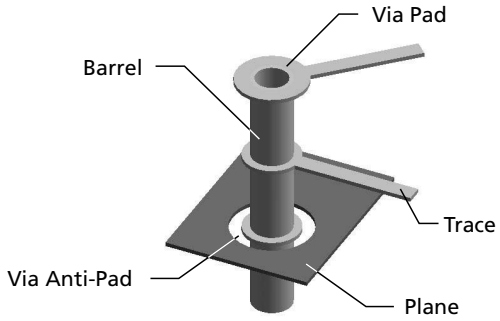


Figure 2: Via



PCB Layout

The PCB layout must be designed to accommodate the package's electrical characteristics.

Power/Ground Planes and Routing

Power and ground interconnect considerations are particularly significant. When possible, power and ground planes should be in a plane layer underneath the package, even if this requires breaking up the plane with vias. Such a configuration is superior to routing power and ground directly to the device through signal traces.

Typically, the ball or lead is connected to the plane through a trace and via, as shown in the Trace Connection to Ball Pad figure. The trace connecting the ball and via pads should be at least as wide as the ball pad, as shown in the Wide Trace Connection to Ball Pad figure.

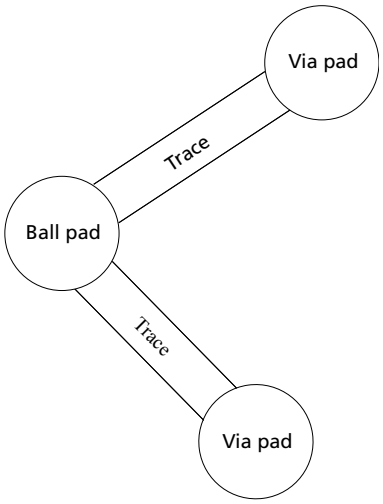
To provide sufficient space for wide or multiple traces, most power and ground balls should be placed on the outside perimeter of the ball-grid array package. The trace should then via to the plane in the shortest distance possible using a power via. The power via should be larger than the signal via and should be connected to the plane with a thermal.

Figure 3: Trace Connection to Ball Pad

Figure 4: Wide Trace Connection to Ball Pad

The Multiple Traces from Ball Pad to Via Pad figure shows multiple traces and vias when there is insufficient space to route a wide trace from the ball to via pads. When possible, the vias should be placed directly in the ball pad.

Figure 5: Multiple Traces from Ball Pad to Via Pad



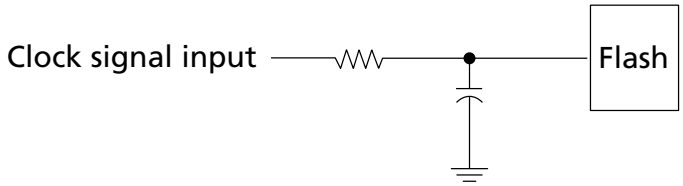
Power Supply Placement and Routing

The power supply ball or leads should be connected to the plane or trace using one or more power vias with thermals.

Clock Signals

In synchronous Flash memory products, the clock signal must be routed to provide impedance control. Otherwise, even at comparatively low clock speeds (such as 33 MHz with fast edge rates) signal integrity problems will occur. A uniform trace impedance prevents reflections and signal integrity problems. The ideal impedance value should match the clock output buffer's impedance. If system and buffer impedances are not ideal, an RC circuit should be placed as close as possible to the clock input to clean up the clock signal.

Figure 6: Clock Signal RC Circuit



Other routing considerations include minimizing distance, routing directly on one layer using strip line, eliminating stubs, and matching one clock output buffer with one clock input.

Control Signals

Similar impedance control and routing measures must be taken with control signals (CE#, WE#, OE#, and WAIT#). Longer setting times help, but impedance control measures are still critical. For example, without them, signal corruption could cause the de-

vice to interpret the falling edge of a WRITE-ERASE signal incorrectly as the rising edge. Then the device would latch in invalid data. Although the subsequent rising edge would latch in valid data, the device might already be executing the wrong program or be in an unexpected state.

Address and Data Signals

Impedance control is less critical for address and data lines since they have more time to settle. However, an exception is during a page mode access operation, when lower address lines are toggling within a page. In such cases, impedance control measures similar to those discussed above should be implemented.

Bypass Capacitors

Bypass capacitors filter electrical noise ("ripple"). For existing devices, the ratio of I/O lines to power and ground connections is typically 8:1—that is, eight I/O lines for every V_{SSQ} and V_{CCQ} line. With this relatively high ratio, bypass capacitance must be sufficient to prevent ground bounce and excessive I/O ripple during I/O line switching. –

Recommended Capacitor Values for Power Supply Lines

Micron recommends using two bypass capacitors to widen the effective decoupling bandwidth. Recommended ceramic capacitor values are 0.1µF and 0.01µF.

Recommended Capacitor Distance from Ball or Lead

The capacitor should be placed as close as possible to the device's ball or lead. Micron's simulations show that a distance of 5mm provides acceptable ripple on I/O lines. In most applications, amplitude is not materially affected by increased distance between the capacitor and device. As with any complex system, this general rule may not apply because of variations in PCB layouts, voltage supplies, package types, and I/O voltage levels. Note that some systems can withstand higher ripple levels than others.

Techniques and Considerations for Bypass Capacitor Placement

If the bypass capacitor cannot be placed next to the device, place the bypass capacitor on the opposite side of the PCB and provide a via to the power plane trace.

The bypass capacitor should be placed close to the ground (V_{SSQ}) and power (V_{CCQ}) connections. Because ground planes are typically directly underneath the device, a via to the plane will satisfy distance requirements.

Before/After Waveforms Showing Bypass Capacitor Effect on I/O Current

Figure 7: Current (I_{CCQ}) Trace Without Bypass Capacitor

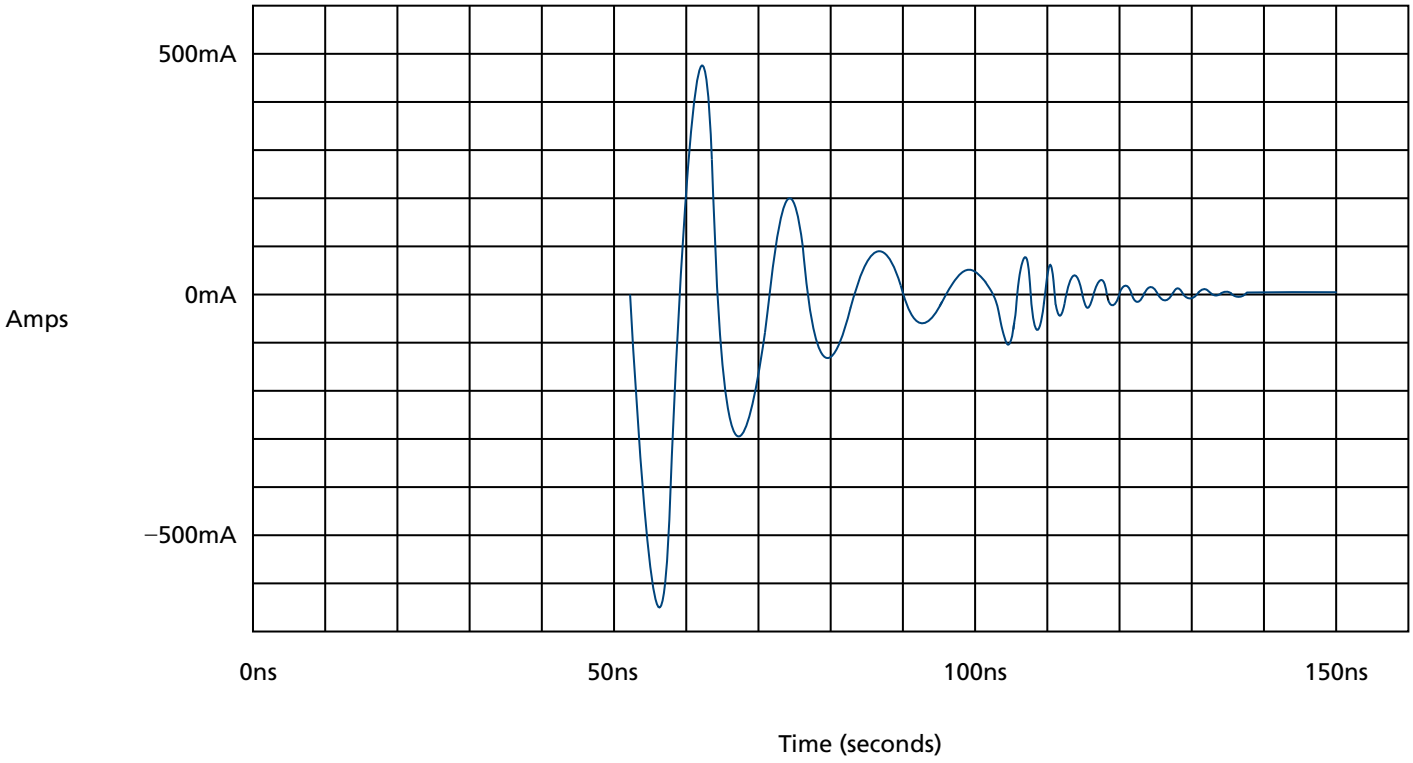


Figure 8: Current (I_{CCQ})Trace with 0.1µF Capacitor

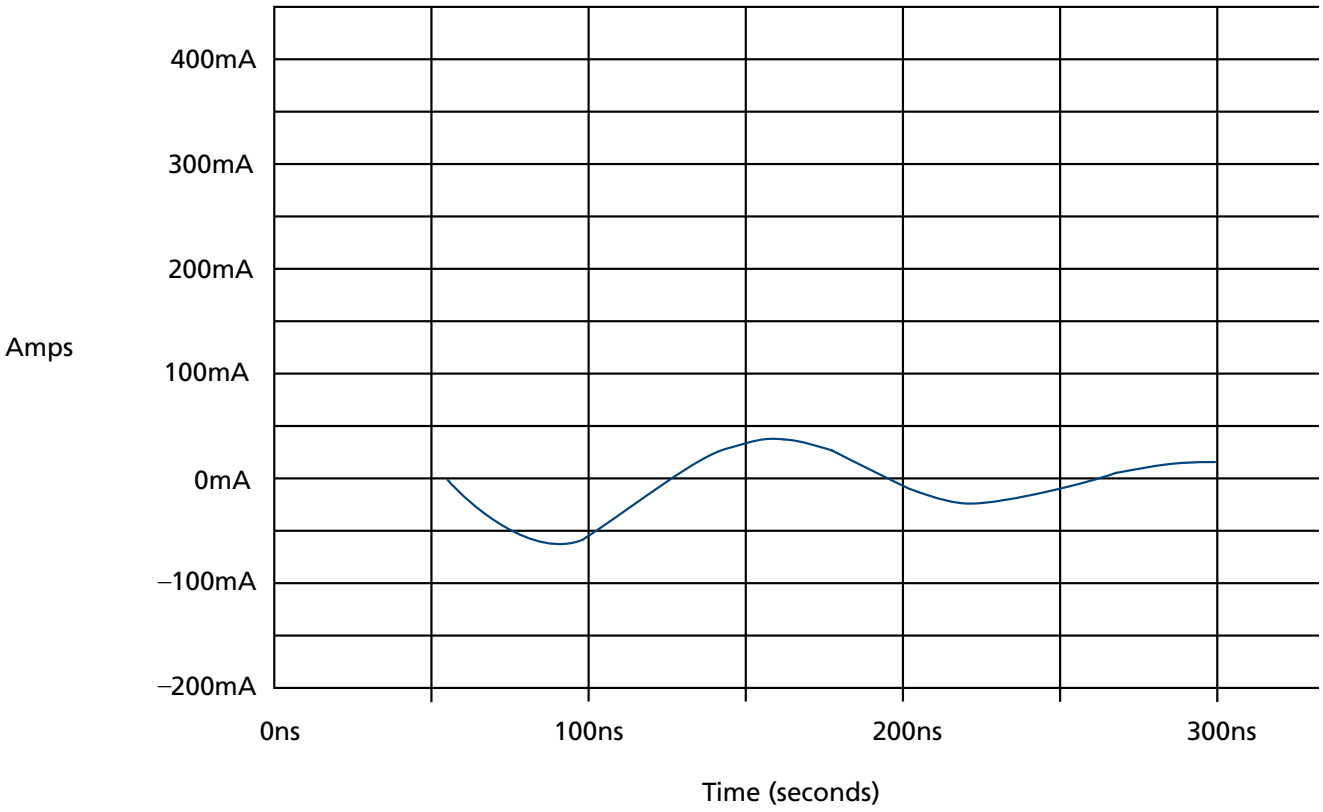


Figure 9: I/O Ripple Trace – Bypass Capacitor 5mm from Device

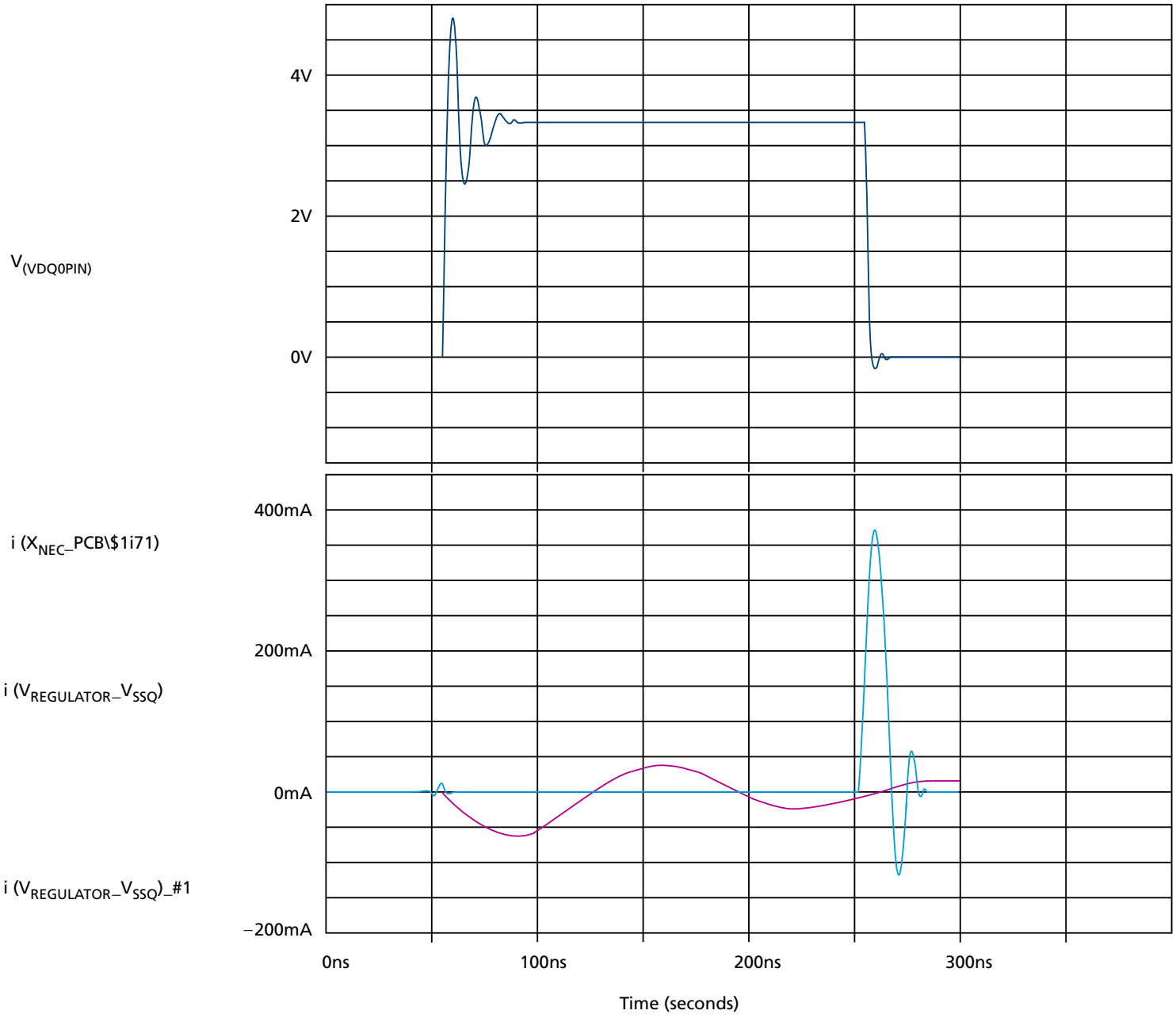
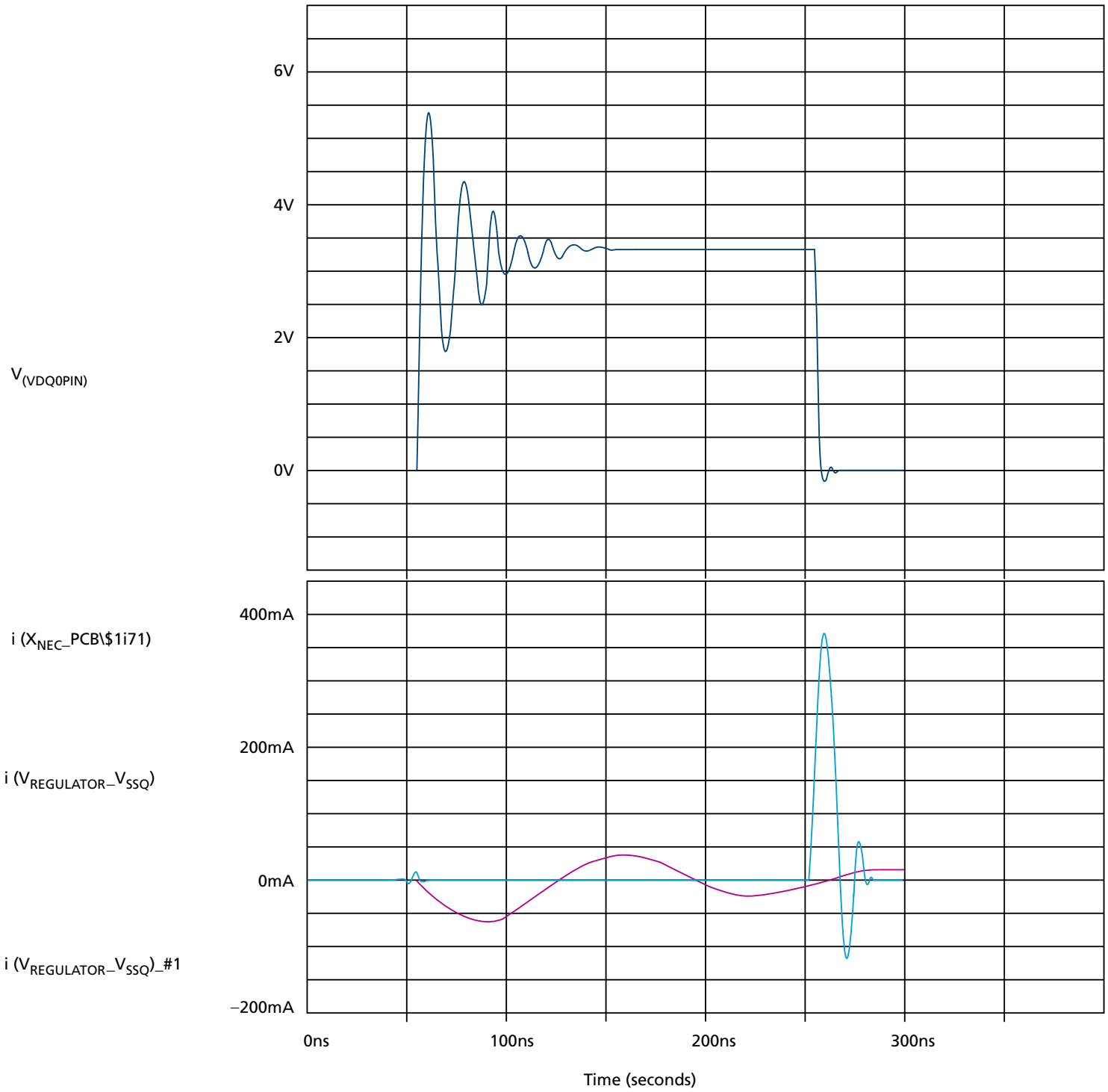


Figure 10: I/O Output Ripple – Bypass Capacitor 30mm from Device



Packaging Considerations

Available packages include EZBGA, FBGA (fine ball grid array), mBGA (mini-ball grid array), SCSP (stacked, chip-scale package), and TSOP (thin, small-outline package). For most applications, variations in electrical characteristics among package types are not significant.

No-Connect Balls

To maintain compatibility with potential future devices, no-connect balls should generally not be electrically connected. An exception is support balls on an SCSP package, which may be connected to the ground plane to increase stability and to facilitate manufacturing.

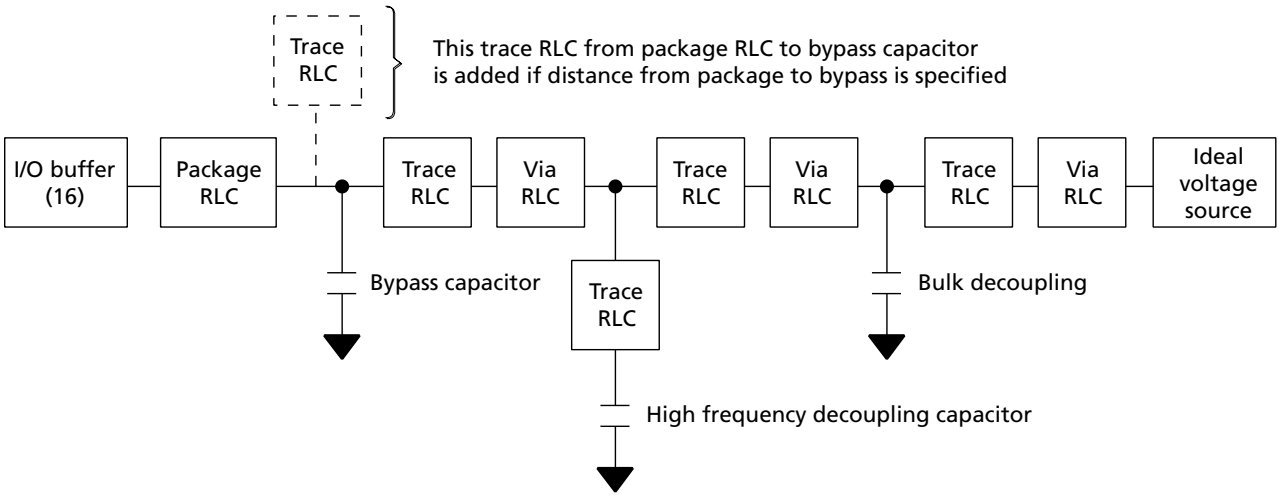
Non-Standard Methods

When the power supply is undersized or the layout is otherwise sub-optimal, resistors can be placed in the V_{CCQ} to limit the current during I/O buffer switching. Resistors are small enough to place two to three in parallel.

Simulation Model Description

The figure below shows the circuit that was used to perform the SPICE simulations for determining capacitance value and distance. Micron wireless Flash memory 1.8V I/O buffers were used using worst-case temperature and voltages. SCSP package RLC (parasitics) were used.

Figure 11: Simulation Block Diagram



Revision History

Rev. A – 11/14

- Initial release with Micron brand

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www.micron.com/products/support Sales inquiries: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.