Technical Note

Migrating from Spansion's S25FL128S to Micron's N25Q 128Mb Flash Device

Introduction

This technical note compares the features of the Micron® N25Q (128Mb) and Spansion S25FL128S Flash memory devices. Features compared include memory organization, package options, signal descriptions, software command set, electrical specifications, and device identification.

Memory Array Architecture

Table 1: Device Comparison

N25Q Features	S25FL128S Features	Notes
Program 1 to 256 bytes	Program 1 to 256 bytes	1
Uniform sector erase (64KB)	Uniform sector erase (64KB)	1
Uniform subsector erase (4KB)	Uniform 4KB granularity available on boot sectors only (top or bottom)	2
Cycling endurance 100,000	Cycling endurance 100,000	
Data retention 20 years	Data retention 20 years	

Notes:
1. For the S25FL128S device, program 512K and uniform sector erase 256KB supported on specific part numbers.
2. On the S25FL128S device, the granularity at 4KB is available for top and bottom sectors only; the remaining sectors must erase at 64KB.

Package Configurations

Table 2: Package Configurations

Package (JEDEC code)	N25Q	S25FL128S
V-PDFN8 (8mm x 6mm)	Yes	Yes
V-PDFN8 (6mm x 5mm) "SAWN"	Yes	No
SOP2-8/208 mils	Yes	No
SOP2-16/300 mils	Yes	Yes
T-PBGA-24b05 (6mm x 8mm, 5 x 5 ball)	Yes	Yes
T-PBGA-24b05 (8mm x 6mm, 4 x 6 ball)	Yes	Yes
KGD	Yes	Yes

Signal Descriptions

Table 3: Signal Descriptions

N25Q	S25FL128S	Type	Description	Notes
C	SCLK	Input	Serial clock	
S#	CS#	Input	Chip select	
–	RESET#	Input	Hardware reset	1
DQ0	SI/IO0	Input or I/O	Serial data input or I/O	
HOLD#/DQ3	HOLD#/SIO3	Input or I/O	HOLD or I/O	2
W#/V_{PP}/DQ2	WP#/IO2	Input or I/O	Write protect/enhanced program supply voltage or I/O	3
DQ1	SO/IO1	Output or I/O	Serial data output or I/O	
V_{CC}	V_{CC}	Power	Supply voltage	
–	V_{IO}	Power	Versatile I/O power supply	
V_{SS}	GND	Ground	Ground	

Notes:
1. RESET functionality is available on Spansion devices with a dedicated part number.
2. RESET functionality is available on devices with a dedicated part number. For the N25Q device, RESET# takes the place of HOLD#.
3. V_{PP} is not available on the S25FL128S device.

Commands

Table 4: Command Set

Command	N25Q Command Code	S25FL128S Command Code	Notes
RESET Operations			
RESET ENABLE	66h	N/A	
RESET MEMORY	99h	F0h	
PERFORMANCE ENHANCE MODE RESET		FFh	1
IDENTIFICATION Operations			
READ ID	9E/9Fh	9Fh	
MULTIPLE I/O READ ID	AFh	N/A	
READ ELECTRONICS SIGNATURE	N/A	ABh	
READ MAN and DEV ID	N/A	90h	
READ SERIAL FLASH DISCOVERY PARAMETER	5Ah	N/A	
READ Operations			
READ	03h	03h	
FAST READ	0Bh	0Bh	
DUAL OUTPUT FAST READ	3Bh	3Bh/3C	
DUAL INPUT/OUTPUT FAST READ	BBh	BBh	
QUAD OUTPUT FAST READ	6Bh	6Bh	
QUAD INPUT/OUTPUT FAST READ	EBh	EBh	
WRITE Operations			
WRITE ENABLE	06h	06h	
WRITE DISABLE	04h	04h	
REGISTER Operations			
READ STATUS REGISTER	05h	05h	
READ STATUS REGISTER 2	N/A	07h	
WRITE STATUS REGISTER	01h	01h	
READ LOCK REGISTER	E8h	E0h	2
WRITE LOCK REGISTER	E5h	E1h	3
READ FLAG STATUS REGISTER	70h	N/A	4
CLEAR FLAG STATUS REGISTER	50h	30h	5
READ NONVOLATILE CONFIGURATION REGISTER	B5h	N/A	
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h	N/A	
READ VOLATILE CONFIGURATION REGISTER	85h	N/A	
WRITE VOLATILE CONFIGURATION REGISTER	81h	N/A	
READ ENHANCED VOLATILE CONFIGURATION REGISTER	65h	N/A	
WRITE ENHANCED VOLATILE CONFIGURATION REGISTER	61h	N/A	
Misc. Operations			
ASP REGISTER READ	N/A	2Bh	

Table 4: Command Set (Continued)

Command	N25Q Command Code	S25FL128S Command Code	Notes
ASP REGISTER WRITE	N/A	2Fh	
READ CONFIGURATION REGISTER	N/A	35h	
AUTOBOOT REGISTER READ	N/A	14h	
AUTOBOOT REGISTER WRITE	N/A	15h	
PPB LOCK BIT WRITE	N/A	A6h	
PPB LOCK BIT READ	N/A	A7h	
PPB READ	N/A	E2h	
PPB PROGRAM	N/A	E3h	
PPB ERASE	N/A	E4h	
PASSWORD READ	N/A	E7h	
PASSWORD PROGRAM	N/A	E8h	
PASSWORD UNLOCK	N/A	E9h	
READ DATA LEARNING PATTERN	N/A	41h	
PROGRAM NV DATA LEARNING REGISTER	N/A	43h	
WRITE VOLATILE DATA LEARNING REGISTER	N/A	4Ah	
PROGRAM Operations			
PAGE PROGRAM	02h	02h	
DUAL INPUT FAST PROGRAM	A2h	N/A	
EXTENDED DUAL INPUT FAST PROGRAM	D2h	N/A	
QUAD INPUT FAST PROGRAM	32h	32h/38h	
EXTENDED QUAD INPUT FAST PROGRAM	12h	N/A	
ERASE Operations			
BULK ERASE	C7h	C7h/60h	
SECTOR ERASE – 64KB	D8h	D8h	
SUB-SECTOR ERASE – 4KB	20h	20h	
PROGRAM/ERASE SUSPEND	75h	85h/75h	
PROGRAM/ERASE RESUME	7Ah	8Ah/7Ah	
ONE-TIME PROGRAMMABLE (OTP) Operations			
READ OTP ARRAY	4Bh	4Bh	
PROGRAM OTP ARRAY	42h	42h	
DEEP POWER-DOWN			
DEEP POWER-DOWN	B9h	N/A	
RELEASE FROM DEEP POWER-DOWN	ABh	N/A	

Notes:
1. Execution in place (XIP) device reset; see the Execute in Place (XIP) section for more details.
2. The name of this command in the S25FL128S data sheet is DYB READ.
3. The name of this command in the S25FL128S data sheet is DYB WRITE.
4. The S25FL128S configuration register is not compatible with the N25Q device.

5. Program/erase error bits are cleared by CLEAR FLAG STATUS REGISTER on the N25Q device. The S25FL128S device performs the same in status register 1.

Table 5: Different Commands Sharing Same Command Code

Command Code	N25Q 128Mb Command	S25F12835F Command
ABh	RELEASE FROM DEEP POWER-DOWN	READ ELECTRONIC SIGNATURE
B9h	DEEP POWER-DOWN	BANK REGISTER ACCESS
E8h	READ LOCK REGISTER	PASSWORD PROGRAM
85h	READ VOLATILE CONFIGURATION REGISTER	PROGRAM/ERASE SUSPEND

READ Commands

The READ command set for the N25Q and S25FL128S devices is identical. Both devices follow the standard three address byte protocol.

Both devices have configurable dummy cycles. The S25FL128S device dummy cycles can be configured by configuration register bits 7 and 8; the N25Q device dummy cycles can be configured by nonvolatile configuration register bits 12–15 or by volatile configuration register bits 7–4.

Table 6: Minimum Number of Dummy Cycles Required per Each Frequency

Frequency	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
MHz	N25Q	S25FL	N25Q	S25FL	N25Q	S25FL	N25Q	S25FL	N25Q	S25FL
≤50	1	0	1	0	1	4	2	0	3	1
≤80	1	8	1	8	3	4	4	8	6	4
≤90	1	8	2	8	4	5	4	8	8	4
≤104	3	8	4	8	6	6	6	8	9	5
≤133	–	8	–	–	–	–	–	–	–	–

Note: 1. The S25FL128S device has one additional clock for mode bits in QUAD I/O FAST READ only.

The S25FL128S device requires a nonvolatile quad bit in the configuration register to enable QUAD I/O functionality. When this bit is set, HOLD# and WP# are disabled.

VECR or NVCR bits enable the QSPI protocol. See the product data sheet for more information.

QUAD commands are available without any register setting. When VECR or NVCR bits are set, W# and HOLD# remain functional. With NVCR set (bit 3 = 0), the device can be powered up or down with QUAD I/O functionality. No additional commands are required for the N25Q device to use QUAD or DUAL I/O functionality.

The manufacturer ID, memory type, and memory capacity for both devices can be read by issuing the 9Fh command. Additionally, the N25Q outputs this data when the 9Eh command is issued. The S25FL128S device has a command that outputs the device ID (ABh) and a command that outputs the manufacturer ID and device ID (90h).

Execute in Place (XIP)

The N25Q device enters and exits XIP mode via volatile and nonvolatile configuration register settings. The nonvolatile configuration register sets XIP mode at device power on. After it is enabled, XIP management in the N25Q device is identical to that of the S25FL128S device. The S25FL128S device uses one nibble (code Ah) to enter or exit XIP mode. This solution is compatible with the N25Q methodology of entering and exiting XIP mode because other bits are "Don't Care".

Table 7: XIP Mode

Mode	N25Q	S25FL128S
Fast read	Yes	N/A
Dual output fast read	Yes	N/A
Dual I/O fast read	Yes	YES
Quad output fast read	Yes	N/A
Quad I/O fast read	Yes	Yes

Figure 1: XIP Timing Configuration

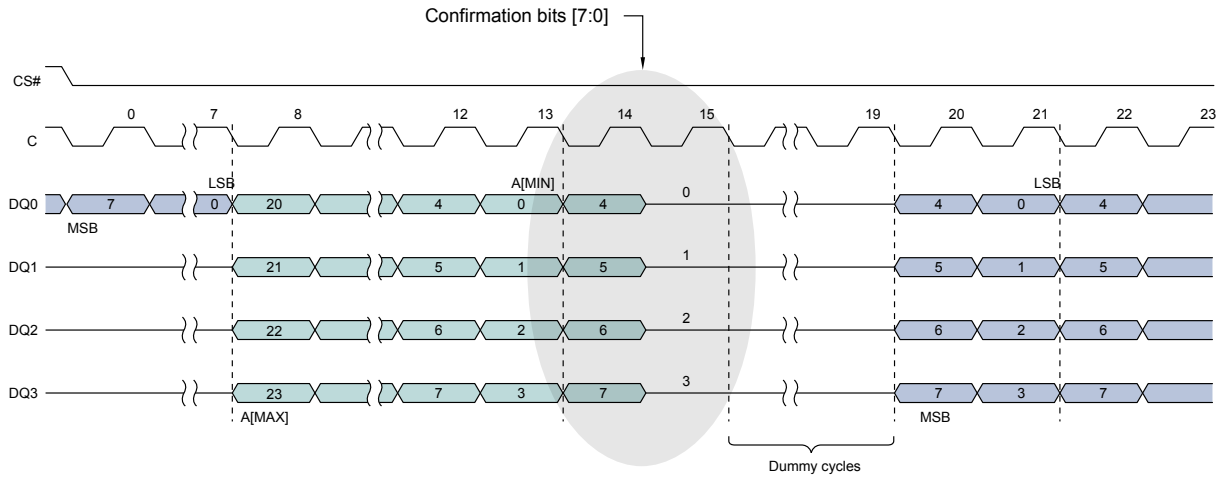


Table 8: XIP Confirmation Bit Software Commands

XIP Confirmation Bit	N25Q	S25FL128S
Enter/confirm XIP mode	B4 = 0 (B7:B5 and B3:B0 = "Don't Care")	Mode bits = Ah; B7 = 1; B6 = 0; B5 = 1; B4 = 0
Exit XIP mode	B4 = 1 (B7:B5 and B3:B0 = "Don't Care")	Mode bit ≠ Ah

XIP and Protocol Exiting Algorithm

To reset XIP mode on the S25FL128S device, using command FFh for N25Q, follow the procedure below.

Note: This sequence is required when power loss occurs because the device may start in an undetermined state (XIP or unnecessary protocol).

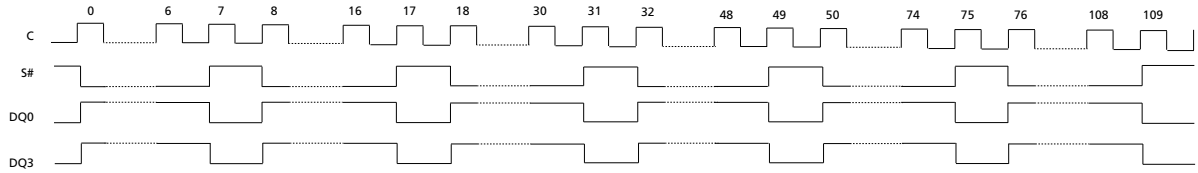
1. Perform the XIP exit sequence.
2. Perform the dual SPI protocol exit sequence.

Note: During the execution of the WRITE NONVOLATILE CONFIGURATION REGISTER command, ^{t}SHSL2 must be at least 50ns.

XIP Exiting Sequence

Below is the reset sequence for all possible XIP configurations (quad I/O, dual I/O, and fast read).

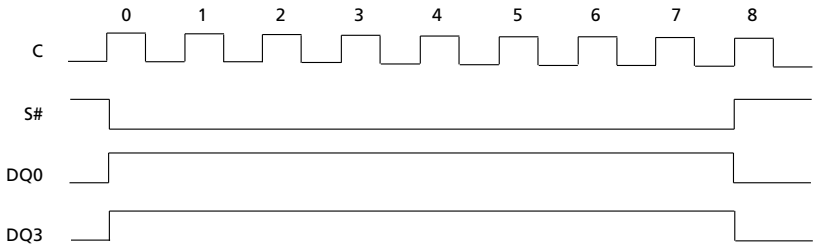
Figure 2: XIP Exiting Sequence



Dual SPI Protocol Exiting Sequence

Exit from dual (DIO-SPI) or quad (QIO-SPI) protocol using the following FFh sequence.

Figure 3: Dual SPI Protocol Exiting Sequence



Electrical Characteristics

Table 9: DC Current Characteristics

Parameter	Symbol	N25Q		S25FL128S		Unit	Notes
		Min	Max	Min	Max		
Standby current	I_{CC1}	–	100	–	100	µA	1
Operating current (fast read quad I/O)	I_{CC3}	–	20	–	61	mA	
Operating current (page program)	I_{CC4}	–	20	–	100	mA	
Operating current (write status register)	I_{CC5}	–	20	–	100	mA	
Operating current (erase)	I_{CC6}	–	20	–	100	mA	

Note: 1. Standby current for the S25FL automotive device is 300µA.

Table 10: DC Voltage Specifications

Parameter	Symbol	N25Q		S25FL128S		Unit
		Min	Max	Min	Max	
Input low voltage	V_{iL}	–0.5	0.3 V_{CC}	–0.5	0.2 V_{CC}	V
Input high voltage	V_{iH}	0.7 V_{CC}	V_{CC} + 0.4	0.7 V_{CC}	V_{CC} + 0.4	V
Output low voltage	V_{OL}	–	0.4	–	0.15 V_{CC}	V
Output high voltage	V_{OH}	V_{CC} - 0.2	–	V_{CC} - 0.2	–	V

AC Characteristics

Table 11: AC Specifications

Parameter	Symbol	Alternate Symbol	N25Q		S25FL128S		Unit
			Min	Max	Min	Max	
Clock frequency (x1 fast read)	^{f}C	^{f}C	–	108	–	133	MHz
Clock frequency (x2, x4 fast read)	^{f}C	^{f}C	–	108	–	104	MHz
Clock frequency (read)	^{f}R	^{f}R	–	54	–	50	MHz
S# active setup time	$^{t}SLCH$	^{t}CSS	4	–	3	–	ns
Data-in setup time	$^{t}DVCH$	^{t}DSU	2	–	3	–	ns
Data-in hold time	$^{t}CHDX$	^{t}DH	3	–	2	–	ns
S# deselect time after correct read (array read to array read)	$^{t}SHSL$	^{t}CSH	50	–	50	–	ns
Output disable time (2.7–3.6V)	$^{t}SZQZ$	^{t}DIS	–	8	–	8	ns
Clock low to output valid (30pF)	$^{t}CLQV$	^{t}V	–	7	–	8	ns
Output hold time	$^{t}CLQX$	^{t}HO	1	-	0	–	ns
HOLD to output Low-Z	$^{t}HHQX$	^{t}LZ	–	8	N/A	8	ns
HOLD to output High-Z	$^{t}HLQZ$	^{t}HZ	–	8	N/A	8	ns

Note: 1. AC specifications compare the fastest versions available at the full voltage range (2.7–3.6V).

Program and Erase Specifications

Table 12: Program and Erase Specifications

Operation	N25Q		S25FL128S		Unit
	Typ	Max	Typ	Max	
PAGE PROGRAM (256 bytes)	0.5	5	0.25	0.75	ms
4KB SUBSECTOR ERASE	0.25	0.8	0.13	0.65	s
64KB SECTOR ERASE	0.7	3	0.13	0.65	s
BULK ERASE	170	250	33	165	s

Configuration and Memory Map

Table 13: Sectors and Subsectors

Sector	Subsector	Address Range	
		Start	End
255	4095	00FF F000h	00FF FFFFh
	:	:	:
	4080	00FF 0000h	00FF 0FFFh
:	:	:	:
127	2047	007F F000h	007F FFFFh
	:	:	:
	2032	007F 0000h	007F 0FFFh
:	:	:	:
63	1023	003F F000h	003F FFFFh
	:	:	:
	1008	003F 0000h	003F 0FFFh
:	:	:	:
0	15	0000 F000h	0000 FFFFh
	:	:	:
	0	0000 0000h	0000 0FFFh

Device Identification

Manufacturer identification is assigned by JEDEC. As a result, the N25Q and S25FL128S devices have a different manufacturer ID and memory type code even though their memory capacity is identical. Command 9Fh is used to read these codes in both devices.

The N25Q device has a unique ID (UID) composed of 17 read-only bytes, which contains the following data:

- The first byte is set to 10h.
- The next two bytes of extended device ID specify device configuration (top, bottom, or uniform architecture and HOLD or RESET functionality).
- The next 14 bytes contain optional customized factory data. The customized factory data bytes are factory programmed. Refer to the N25Q 128Mb data sheet for more information.

Table 14: Read Identification Summary

Parameter	N25Q Code	S25FL128S Code
Manufacturer ID	20h	01h
Memory type	BAh	20h
Memory capacity	18h	18h

Part Numbers

Table 15: Cross Reference of Part Numbers

Micron Part Number	Spansion Part Number[1]	Package	Secure	Media	Notes
N25Q128A13E1240E	S25FL128SAGBFIA00	T-PBGA	No	Tray	
N25Q128A13E1240F	S25FL128SAGBFIA03	T-PBGA	No	Tape and Reel	
N25Q128A13E1241E	N/A	T-PBGA	Yes	Tray	2
N25Q128A13E1241F	N/A	T-PBGA	Yes	Tape and Reel	2
N25Q128A813E12A0F	S25FL128SAGBFVA00	T-PBGA	No	Tape and Reel	
N25Q128A813EF740E	S25FL128SAGBFIA13	V-PDFN-8	No	Tray	
N25Q128A13EF740F	N/A	V-PDFN-8	No	Tape and Reel	3
N25Q128A13EF840E	S25FL128SAGNFI000	V-PDFN-8	No	Tray	
N25Q128A13EF840F	S25FL128SAGNFI003	V-PDFN-8	No	Tape and Reel	
N25Q128A13EF8A0F	S25FL128SAGNFV003	V-PDFN-8	No	Tape and Reel	
N25Q128A13ESE40E	N/A	SO8 Wide	No	Tray	4
N25Q128A13ESE40F	N/A	SO8 Wide	No	Tape and Reel	
N25Q128A13ESE40G	N/A	SO8 Wide	No	Tube	
N25Q128A13ESF40E	S25FL128SAGMFI000	SO16 Wide	No	Tray	
N25Q128A13ESF40F	S25FL128SAGMFI003	SO16 Wide	No	Tape and Reel	
N25Q12813ESF40G	S25FL128SAGMFI001	SO16 Wide	No	Tube	
N25Q128A13ESFA0F	S25FL128SAGMFV000	SO16 Wide	No	Tape and Reel	
N25Q128A13ESFH0E	N/A	SO16 Wide	No	Tray	5
N25Q128A13ESFH0F	N/A	SO16 Wide	No	Tape and Reel	5
N25Q128A13EV740		KGD	Yes		6

Notes:
1. All Spansion part numbers include 64KB UNIFORM SECTOR ERASE, footprint with RESET# and V_{IO}.
2. Spansion device does not support secure release.
3. Spansion device does not support SAWN package.
4. Spansion device does not support SOP2-8/208 mils package.
5. Spansion device does not support automotive ews flow.
6. Information for part number code KGD not provided in Spansion data sheet.

Conclusion

Comparing features of the Micron N25Q 128Mb and Spansion S25FL128S Flash memory devices enables users to migrate applications from the S25FL128S to the N25Q 128Mb device.

Revision History

Rev. A – 07/13

- Initial release

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