Technical Note

NOR Flash Cycling Endurance and Data Retention

Introduction

NOR Flash memory is subject to physical degradation that can lead to device failure. As a result, customers often ask how long Micron's NOR devices will retain data; this question can be answered with device testing. This technical note defines the industry standards for this testing, Micron's NOR Flash testing methodology, and the two key metrics used to measure NOR device failure: cycling endurance and data retention. It also outlines two case studies that test the different endurance and data retention requirements for applications that use Micron's NOR Flash devices.

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Cycling Endurance and Data-Retention Testing Methodology

Industry-Standard Testing Methodology

Micron uses the current JEDEC global standard for testing Flash memory devices. (The JESD47I specification was the most current version at the time of publication.)

Table 1: JESD47I Device Qualification Tests

Stress	Reference	Abbreviation	Conditions	Requirements	
				# Lots/SS per Lot	Duration/Accept
High-temperature operating life	JESD22-A108, JESD85	HTOL	$T_J \geq 125°C$, $V_{CC} \geq V_{CC,max}$	3 lots/77 devices	1000 hours/0 failures
Early-life failure rate	JESD22-A108, JESD74	ELFR	$T_J \geq 125°C$, $V_{CC} \geq V_{CC,max}$	See ELFR table	48 ≤ ^{t} ≤ 168 hours
Low-temperature operating life	JESD22-A108	LTOL	$T_J \leq 50°C$, $V_{CC} \geq V_{CC,max}$	1 lot/32 devices	1000 hours/0 failures
High-temperature storage life	JESD22-A103	HTSL	$T_A \geq 150°C$	3 lots/25 devices	1000 hours/0 failures
Latch-up	JESD78	LU	Class I or II	1 lot/3 devices	0 failures
Electrical parameter assessment	JESD86	ED	Data sheet	3 lots/10 devices	T_A per data sheet
ESD human body model	JESD22-A114	ESD-HBM	$T_A = 25°C$	3 devices	Classification
ESD-charged device model	JESD22-C101	ESD-CDM	$T_A = 25°C$	3 devices	Classification
Accelerated soft error testing	JESD89-2, JESD89-3	ASER	$T_A = 25°C$	3 devices	Classification
System soft error testing	JESD89-1	SSER	$T_A = 25°C$	Minimum of 1E+06 device hours or 10 fails	Classification
Nonvolatile memory cycling endurance	JESD22-A117	NVCE[1]	≥ 25°C and $T_J \geq 55°C$	3 lots/77 devices	Cycles per NVCE (≥ 55°C)/96 and 1000 hours/0 failures
Uncycled high-temperature data retention	JESD22-A117	UCHTDR[2]	$T_A \geq 125°C$	3 lots/77 devices	1000 hours/0 failures
Post-cycling high-temperature data retention	JESD22-A117	PCHTDR[3]	Option 1: $T_J = 100°C$	3 lots/39 devices	Cycles per NVCE (≥ 55°C)/96 and 1000 hours/0 failures
			Option 2: $T_J \geq 125°C$		Cycles per NVCE (≥ 55°C)/10 and 1000 hours/0 failures

Notes:
1. **NVCE** cycles a device and then tests it at room temperature to ensure that the part is still functional and meets all data sheet requirements.
2. **UCHTDR** checks the data retention of uncycled devices at a high temperature.
3. **PCHTDR** checks the data retention of cycled devices at a high temperature.

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Micron Testing Methodology

As shown by comparing Table 1 (page 2) and Table 2 (page 3), Micron's NOR Flash testing conditions meet JESD47I requirements without exception.

Table 2: Micron's NOR Flash Device Qualification Tests

Stress	Abbreviation	Conditions	Requirement
High-temperature operating life	HTOL	Maintain continual operation of the device with $T_J > 125°C$ and $V_{CC} > V_{CC,max}$	1000 hours with 0 failures
Early-life failure rate	ELFR	Accelerate first-year defects with $T_J > 125°C$ and $V_{CC} > V_{CC,max}$	0–168 hours
Low-temperature operating life	LTOL	Operate with $T_J < 50°C$ and $V_{CC} > V_{CC,max}$	1000 hours with 0 failures
High-temperature storage life	HTSL	Detect temperature-accelerated defects with $T_A > 150°C$	1000 hours with 0 failures
Latch-up	LU	Verify V_{CC} over voltage and I/O trigger current resistance to LU	0 failures
Electrical parameter assessment	ED	Test data sheet parameters	QV testing 85°C and –40°C
ESD Human body model	ESD-HBM	Human body model ESD resistance	Per specification
ESD-charged device model	ESD-CDM	Charged device model ESD resistance	Per specification
Accelerated soft error testing	ASER	$T_A = 25°C$	Per specification
System soft error testing	SSER	$T_A = 25°C$	Per specification
Nonvolatile memory cycling endurance	NVCE	Distributed cycling at room (25°C) and hot ($T_J > 55°C$) temperatures for 3 weeks	Room and hot-temperature cycling 1000 hours with 0 failures
Uncycled high-temperature data retention	UCHTDR	$T_A \geq 125°C$	1000 hours/0 failures
Post-cycling high-temperature data retention	PCHTDR	Option 1: $T_J = 100°C$	Cycles per NVCE (≥ 55°C)/96 and 1000 hours/0 failures
		Option 2: $T_J \geq 125°C$	Cycles per NVCE (≥ 55°C)/10 and 1000 hours/0 failures

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Cycling Endurance

In this technical note, cycling is defined as the cumulative number of PROGRAM (0s)/ ERASE operations (1s) performed on the Flash device. NOR Flash is always erased at the sector (also known as block) level. Each PROGRAM/ERASE operation can degrade the memory cell, and over time, the cumulation of cycles can prevent the device from meeting power, programming, or erasing specifications or from reading the correct data pattern.

JEDEC Cycling Testing

JESD47I-defined testing for NVCE is performed at two temperatures; half the devices are cycled at room temperature (25°C), and the other half are cycled at an elevated temperature (i.e. at 85°C, following Jedec requirement to run high temperature cycling at T >= 55°C). It is not always feasible to cycle every block on the device for the maximum number of cycles (100,000 for NOR) due to time constraints. As outlined in JESD47I, NVCE testing is capped at 500 hours, and each device must have at least one block or sector cycled to 100,000 cycles. Cycling at 1%, 10%, and 100% should be divided by the cycling time so that one-third of the cycle time is 1000, 10,000, and 100,000.

As shown in the figure below, JESD47I is used to separate a many-block device into cycled blocks of 1%, 10%, and 100% of the maximum specification. One-third of the cycling time is devoted to each of these three cycle counts, and at least one block is cycled to the maximum specification.

Figure 1: JESD47I NVCE Cycling of a Multiblock Device

1K	0K	0K	0K	0K	0K	0K	0K	0K	0K	0K
1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K
1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K
1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K
1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K
1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K
1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K
1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K
1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K
1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K
10K	10K	10K	10K	10K	10K	10K	10K	10K	10K	100K

Total cycle time = 500 hours (MAX)

Blocks not cycled

1/3 of cycle time for 1000 (1K)

1/3 of cycle time for 10,000 (10K)

1/3 of cycle time for 100,000 (100K)

Notes:
1. Cycling is performed at 25°C and 85°C.
2. At least one block is cycled to the maximum specification (100,000 cycles).

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Micron Cycling Testing

Micron's NOR product line is designed to handle 100,000 PROGRAM/ERASE cycles. The figure below shows an example of how blocks are divided into 1%, 10%, and 100% of the 100,000 maximum specification when testing Micron's NOR devices. As shown in the Total Cycles column, one-third of the cycling time is devoted to each of these three cycle counts.

Figure 2: Micron NVCE Testing – NOR Die Example

239	238	237	236	235	234	233	232	231	230	229	228	227	226	225	224		240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192		208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160		176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128		144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96		112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64		80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Periphery

	Block Cycle Count	Blocks	Total Cycles
0% of MAX	0	32	0
1% of MAX	1000	202	202,000
10% of MAX	10,000	20	200,000
100% of MAX	100,000	2	200,000
	Total	259	602,000

Note: 1. Cycling is performed at 25°C and 85°C.

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Data Retention

In this technical note, data retention is defined as retaining a given data pattern for the expected life of a NOR Flash device. Data retention tests evaluate the reliability of the device to withstand a specified number of PROGRAM/ERASE cycles. Post-cycling data retention tests evaluate the data retention capability of the device after it has been subjected to extensive PROGRAM/ERASE cycling.

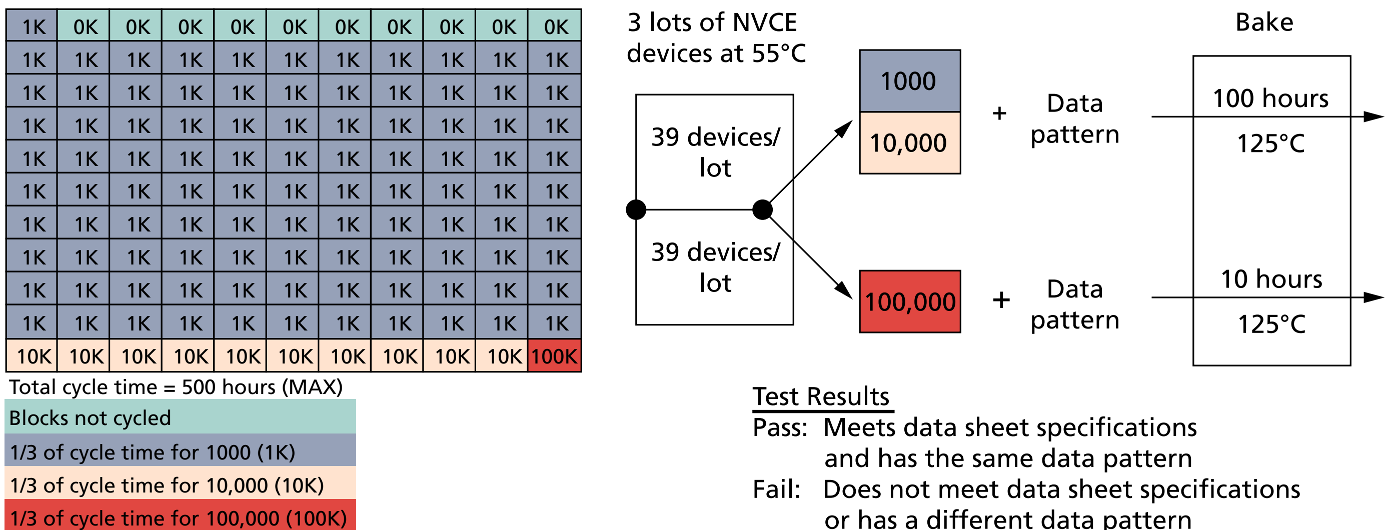
JEDEC Data Retention Tests

JESD47I requires two different tests to validate data retention:

- The uncycled high-temperature data retention (UCHTDR) test is performed on uncycled devices at 125°C. A data pattern is input, samples are submitted to high temperature storage for 1000 hours. This testing duration ensures acceptable quality in a reasonable Flash memory application.
- The post-cycling high-temperature data retention (PCHTDR) test is performed on NVCE devices, which have been cycled at 85°C, and tests them at 125°C to check for data sheet violations and data pattern integrity. The JESD47I specification defines two PCHTDR test flows:
  - *Test Flow 1:* For the blocks that were cycled at 1% and 10% of the maximum specification, a data pattern is programmed into the blocks, the blocks are baked for 100 hours at 125°C, and then they are tested.
  - *Test Flow 2:* For the blocks that were cycled at 100% of the maximum specification, a data pattern is programmed into the blocks, the blocks are baked for 10 hours at 125°C, and then they are tested.

  For both PCHTDR test flows, if the blocks meet all data sheet specifications, and the data pattern is the same, the device passes; if any data sheet violations occur, the device fails.

Figure 3: JESD47I PCHTDR Test



Note: 1. At least one block cycled to the maximum specification (100,000 cycles).

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Micron Data Retention Tests

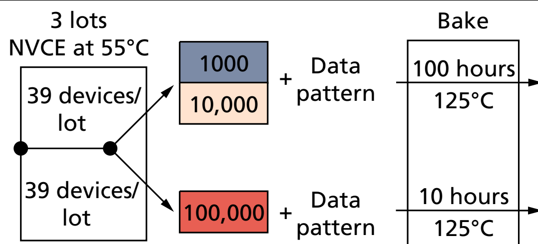
Micron performs two JESD47I-compliant data retention tests on NOR Flash devices:

- Micron's **UCHTDR** test is a high temperature (125°C) storage test aimed at evaluating the data retention capability of the Flash cell when it is fresh, that means it has been submitted to none or very few P/E cycles.. A checkerboard data pattern is used to simulate random patterns expected during actual use. Finally, all devices are tested for standard data sheet requirements.
- Micron's **PCHTDR** test evaluates the data retention capability of the Flash cell after extensive PROGRAM/ERASE cycling. As shown in the figure below, blocks cycled to 100,000 PROGRAM/ERASE cycles are baked at 125°C for 10 hours; the blocks cycled to 10,000 and 1000 are baked for 100 hours. After bake, all devices are tested for standard data sheet requirements.

Figure 4: Micron PCHTDR Test – NOR Die Example

239	238	237	236	235	234	233	232	231	230	229	228	227	226	225	224		240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192		208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160		176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128		144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96		112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64		80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Periphery



Test Results
Pass: Meets data sheet specifications and has the same data pattern
Fail: Does not meet data sheet specifications or has a different data pattern or

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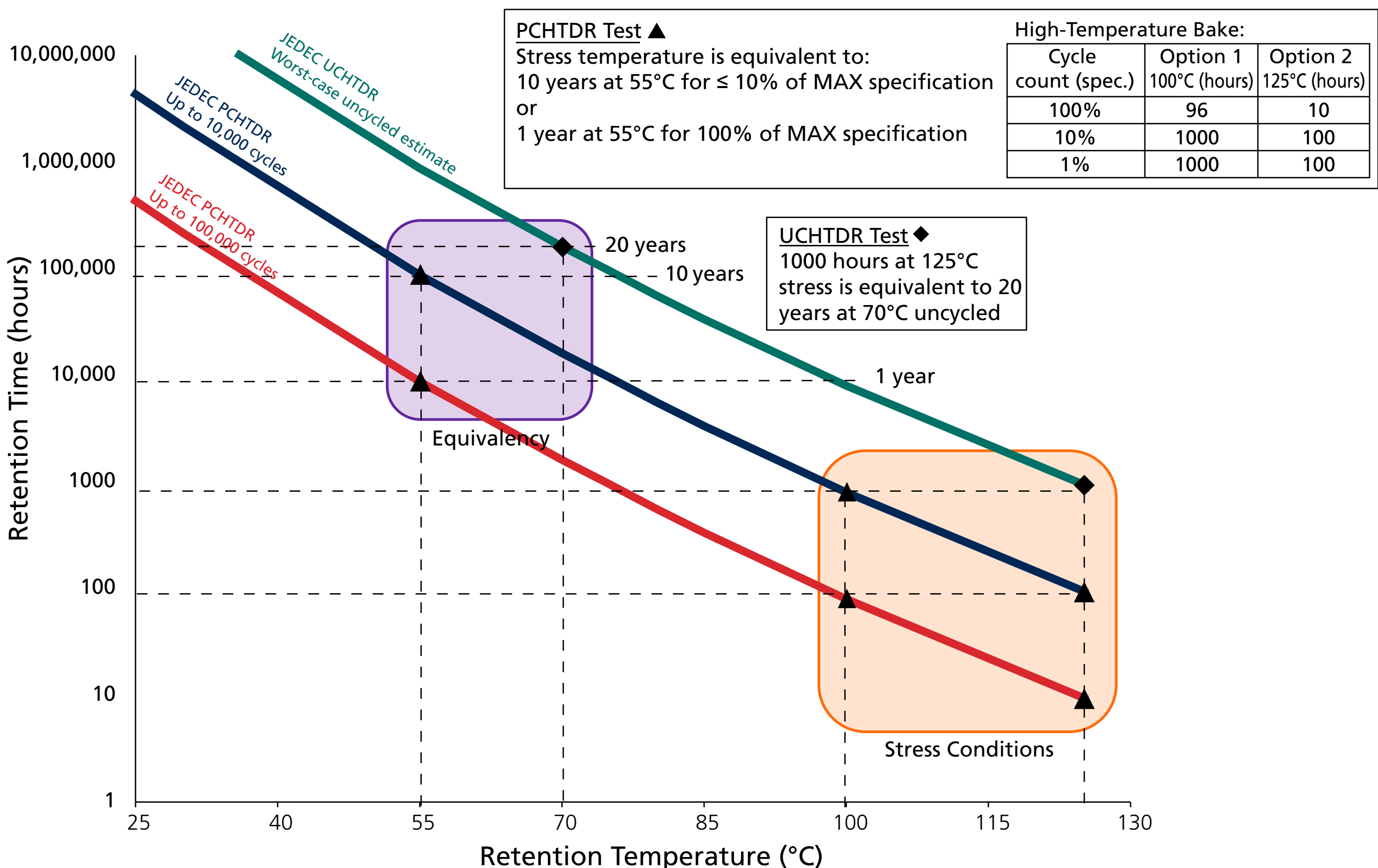
Modeling Data Retention and Cycling Endurance

The dominant wear mechanism for charge loss and gain in NOR Flash memory occurs through electron trapping in the tunnel oxide of the Flash cell. This results in leakage through the insulator, and the damage primarily occurs during the ERASE/WRITE operations of a cell.

In the figure below, the annealing of this damage is thermally modeled using an Arrhenius relationship where the activation energy of detrapping is 1.1eV (see JESD22-A117). The amount of annealing or relaxation depends on the estimated field usage time.

This model assumes that cycles are equally distributed across the usage time. In regards to uncycled stress (UCHTDR) performance, a conservative model is assumed with 1000 hours of 125°C uncycled stress and 1.1eV for detrapping. 1000 hours of stress at 125°C translates to 100 years of real-time use at 55°C. The uncycled performance is equivalent or better than this estimate.

Figure 5: Data Retention vs. Cycling Endurance Counts



Notes:
1. The data points in the orange Stress Conditions box represent the JESD47I specification's five valid conditions for the UCHTDR and PCHTDR tests.
2. The data points in the purple Equivalency box represent the JESD47I specification's equivalent life conditions for a given test.
3. Uncycled is defined as fewer than five PROGRAM/ERASE cycles for a given block.

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Application Case Studies

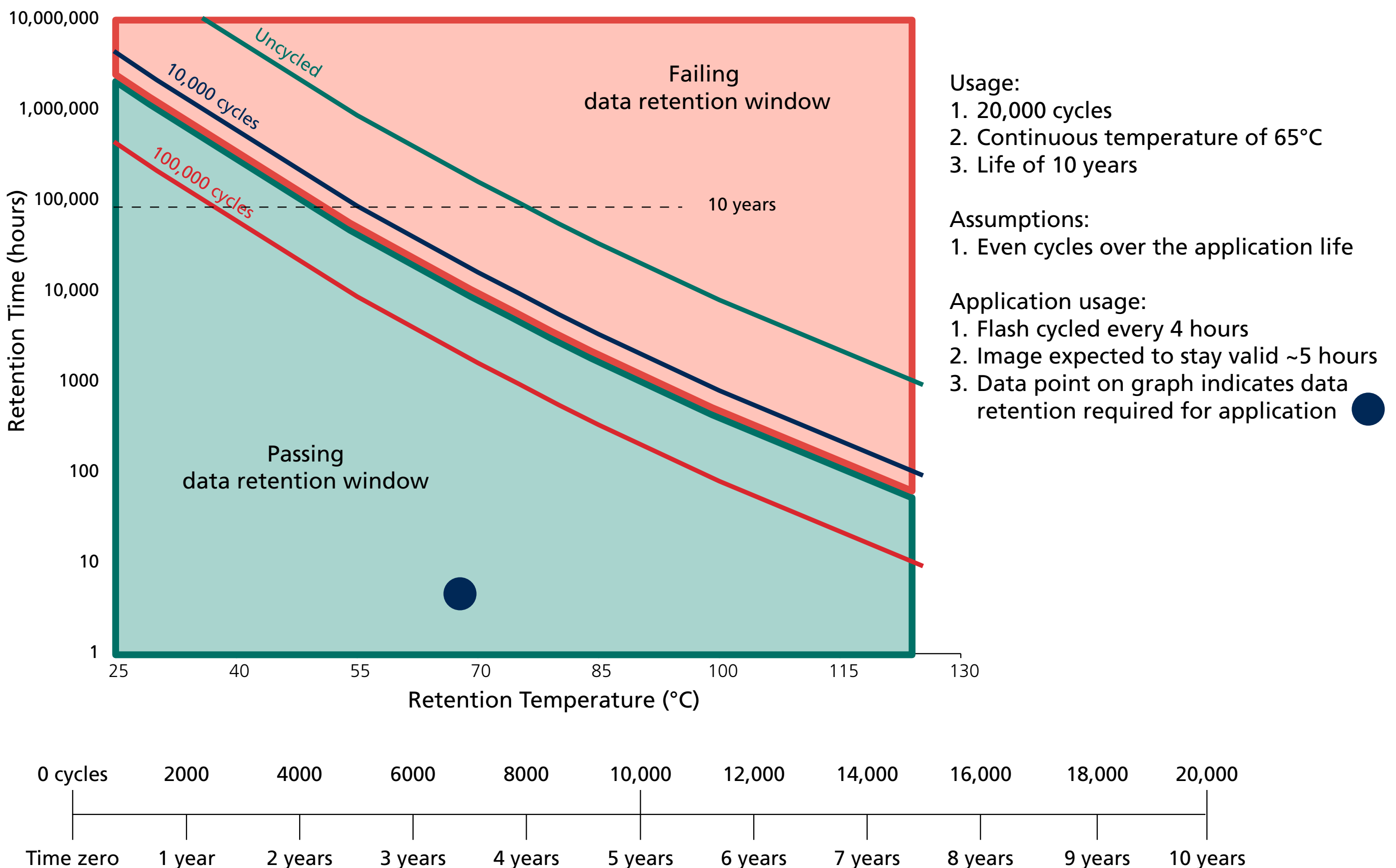
The JESD47I standard is designed for testing NOR Flash device use in reasonable conditions; it does not cover use in more extreme conditions. Therefore, Micron has performed two case studies to compare data retention for 1) NOR use within the JESD47I-specified conditions and 2) NOR use outside of those conditions. These studies help to identify any data retention issues over the life of the application using Micron's NOR Flash devices.

Case Study #1 – Conditions Within JEDEC Specifications

In the first case study, it is assumed that the application will have an expected life of 10 years with a worst-case temperature of 65°C. The data on the NOR device will be cycled 20,000 times with the cycling evenly distributed over the 10 years. For this example, the NOR device will be written to once every four hours.

As shown in the figure below, this case study demonstrates that with evenly distributed device cycling, the data will last for 10 years of application life with no risk of data retention issues.

Figure 6: Case Study #1



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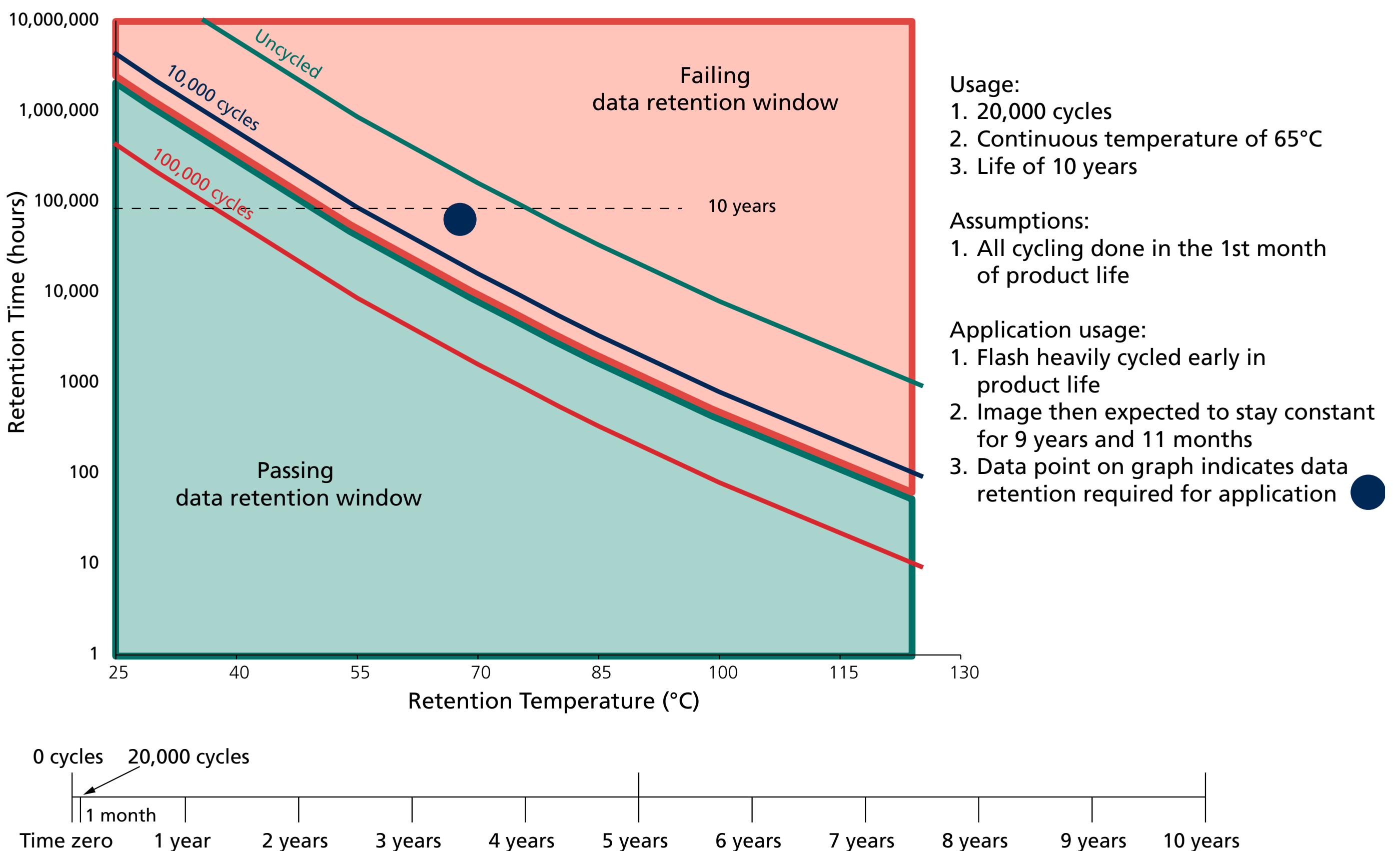
Case Study #2 – Conditions Outside JEDEC Specifications

In the second case study, the usage model is the same as in the first case study, except in regards to the cycling frequency. The expected application life is 10 years with a worst-case temperature of 65°C. Over 10 years, the data on the NOR device will be cycled 20,000 times; however, there will be heavy cycling during the first month of application life and then the data is expected to remain valid with no further cycling for 9 years and 11 months.

As shown in the figure below, this case study demonstrates that with device cycling heavily distributed early in application life (a condition outside of JEDEC specifications), there is a risk that the data will not be valid at the end of the 10-year application life.

Figure 7: Case Study #2



To minimize the risk for applications that may require data retention following heavy cycling at the start of the product life (like in Case Study #2), system software can be programmed to refresh the data in the cycled blocks once every one or two years, which would provide adequate data retention. Another option for meeting data retention requirements is to separate blocks that are heavily cycled (data images) from blocks that require long data retention (code images). For the heavily cycled blocks, wear leveling can be used to spread PROGRAM/ERASE cycles across multiple blocks.

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Conclusion

Micron's NOR Flash devices meet all JEDEC requirements for cycling endurance and data retention. Cycling endurance for Flash memory requires that at least one block be cycled to 100% of the maximum specification and that cycling must be completed within 1000 hours. Not all cycling tests are performed at 100% of the maximum specification —some are performed at 1% and 10%. Data retention stress conditions are correlated to real-world usage cases and are measured for both uncycled devices and devices that are cycled at 1% and 10% of the specification and tested at 100% of the maximum specification.

Cycling endurance and data retention are not independent of one another; they are interrelated and also a function of temperature. Application requirements for cycling and data retention can vary, and, depending on cycling count, temperature, and the time needed to retain data, industry standards may or may not provide a valid usage model.

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Revision History

Rev. B – 09/15

- UCHTDR test conditions and definition clarified

Rev. A – 07/13

- Initial release.

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