Technical Note

Migrating from EON's EN25QH256 to Micron's N25Q 256Mb Flash Device

Introduction

The purpose of this technical note is to compare features of the Micron® N25Q (256Mb) and EON EN25QH256 Flash memory devices. Features compared include memory organization, package options, signal descriptions, the software command set, electrical specifications, and device identification.

Memory Array Architecture

Table 1: Device Comparison

N25Q Features	EN25Q Features
Program 1 to 256 bytes	Program 1 to 256 bytes
Uniform sector erase (64KB)	Uniform sector erase (64KB)
Uniform subsector erase (4KB)	Uniform subsector erase (4KB)
Cycling endurance 100,000	Cycling endurance 100,000
Data retention 20 years	Data retention 20 years

Package Configurations

Table 2: Package Configurations

Package (JEDEC code)	N25Q 256Mb	EN25Q
V-PDFN8 (8mm x 6mm)	Yes	Yes
SOP2-16/300 mil	Yes	Yes
T-PBGA24b05 (6mm x 8mm, 5 x 5 ball)	Yes	Yes

Signal Descriptions

Table 3: Signal Descriptions

N25Q Signal	EN25Q Signal	Type	Description	Notes
C	CLK	Input	Serial clock	
DQ0	DI	Input or I/O	Serial data input or I/O	
DQ1	DO	Output or I/O	Serial data output or I/O	
S#	CS#	Input	Chip select	
W#/V_{PP}/DQ2	WP#/DQ2	Input or I/O	Write protect/enhanced program supply voltage or I/O	1
HOLD#/DQ3	HOLD#/DQ3	Input or I/O	HOLD or I/O	
V_{CC}	V_{CC}	Input	Supply voltage	
V_{SS}	V_{SS}	Input	Ground	

Note: 1. V_{PP} is not available on the EN25Q device.

Commands

Table 4: Command Set

Command	Command Code N25Q	Command Code EN25Q	Notes
RESET Operations			
READ ENABLE	66h	66h	
RESET MEMORY	99h	99h	
RESET QUAD I/O	N/A	FFh	1
IDENTIFICATION Operations			
READ ID	9E/9Fh	90h/9Fh	
MULTIPLE I/O READ ID	AFh	N/A	2
READ DEVICE ID	N/A	ABh	
READ SERIAL FLASH DISCOVERY PARAMETER	5Ah	5Ah	
READ Operations			
READ	03h	03h	
FAST READ	0Bh	0Bh	
DUAL OUTPUT FAST READ	3Bh	3Bh	
DUAL INPUT/OUTPUT FAST READ	BBh	BBh	
QUAD OUTPUT FAST READ	6Bh	N/A	
QUAD INPUT/OUTPUT FAST READ	EBh	EBh	
FAST_READ.DTR	0Dh	N/A	3
DUAL OUTPUT FAST READ DTR	3Dh	N/A	3
DUAL INPUT/OUTPUT FAST READ DTR	BDh	N/A	3
QUAD OUTPUT FAST READ DTR	6Dh	N/A	3
QUAD INPUT/OUTPUT FAST READ DTR	EDh	N/A	3
4-BYTE ADDRESS MODE Operations			
ENTER 4-BYTE ADDRESSING	B7h	B7h	
EXIT 4-BYTE ADDRESSING	E9h	E9h	
4-BYTE READ	13h	N/A	4
4-BYTE FAST_READ	0Ch	N/A	
4-BYTE DUAL OUTPUT FAST READ	3Ch	N/A	
4-BYTE DUAL INPUT/OUTPUT FAST READ	BCh	N/A	
4-BYTE QUAD OUTPUT FAST READ	6Ch	N/A	
4-BYTE QUAD INPUT/OUTPUT FAST READ	ECh	N/A	
4-BYTE Page Program	02h	N/A	
4 BYTE Quad Page Program	32h	N/A	
4-BYTE Sector Erase – 64KB	D8h	N/A	
4-BYTE Sub-Sector Erase – 4KB	20h	N/A	
ENTER HIGH BANK LATCH MODE	N/A	67h	5
EXIT HIGH BANK LATCH MODE	N/A	98h	5

Table 4: Command Set (Continued)

Command	Command Code N25Q	Command Code EN25Q	Notes
ENABLE QUAD PERIPHERAL INTERFACE MODE (EQPI)	N/A	38h	6
WRITE Operations			
WRITE ENABLE	06h	06h	
WRITE DISABLE	04h	04h	
REGISTER Operations			
READ STATUS REGISTER	05h	05h	
WRITE STATUS REGISTER	01h	01h	
READ INFORMATION REGISTER	N/A	2Bh	7
READ LOCK REGISTER	E8h	N/A	
WRITE LOCK REGISTER	E5h	N/A	
READ FLAG STATUS REGISTER	70h	N/A	
CLEAR FLAG STATUS REGISTER	50h	N/A	
READ NONVOLATILE CONFIGURATION REGISTER	B5h	N/A	
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h	N/A	
READ VOLATILE CONFIGURATION REGISTER	85h	N/A	
WRITE VOLATILE CONFIGURATION REGISTER	81h	N/A	
READ ENHANCED VOLATILE CONFIGURATION REGISTER	65h	N/A	
WRITE ENHANCED VOLATILE CONFIGURATION REGISTER	61h	N/A	
READ EXTENDED ADDRESS REGISTER	C8h	N/A	5
WRITE EXTENDED ADDRESS REGISTER	C5h	N/A	5
PROGRAM Operations			
PAGE PROGRAM	02h	02h	
QUAD INPUT FAST PROGRAM	32h	N/A	
QUAD INPUT/OUTPUT FAST PROGRAM	12h	N/A	
OTP PROGRAM	42h	N/A	
DUAL INPUT FAST PROGRAM	A2h	N/A	
DUAL INPUT/OUTPUT FAST PROGRAM	D2h	N/A	
ERASE Operations			
BULK ERASE	C7h	60h or C7h	
SECTOR ERASE – 64KB	D8h	D8h	
SUB-SECTOR ERASE – 4KB	20h	20h	
PROGRAM/ERASE SUSPEND	75h	N/A	
PROGRAM/ERASE RESUME	7Ah	N/A	
ONE-TIME PROGRAMMABLE (OTP) Operations			
READ OTP ARRAY	4Bh	N/A	
PROGRAM OTP ARRAY	42h	N/A	
DEEP POWER-DOWN			

Table 4: Command Set (Continued)

Command	Command Code N25Q	Command Code EN25Q	Notes
DEEP POWER-DOWN	B9h	B9h	8
RELEASE FROM DEEP POWER-DOWN	ABh	ABh	

Notes:
1. EON RESET ENABLE QUAD PERIPHERAL INTERFACE (EQPI) protocol.
2. The EN25Q device uses the same command (STD and MULTIPLY I/O) to read information for ID identification.
3. The EN25Q device does not support DTR mode.
4. The N25Q device features dedicated opcodes working in 4-byte address mode regardless of the current addressing mode (3, 4 bytes).
5. For the N25Q device, access to the upper and lower 128Mb segments is done by extended address register setting. Access to these segments in the EN25Q device is done by a command.
6. For the N25Q device, set this protocol by volatile register (VECR bity 7) or nonvolatile register (NVCR bit 3).
7. For the EN25Q device, this register contains multifunctional information (see the EN25Q data sheet for more information).
8. The DEEP POWER DOWN operation is available in N25Q 1.8V devices only.

Table 5: Different Commands Sharing Same Command Code

Command	N25Q 256Mb Command	EN25Q 256Mb Command
ABh	RELEASE FROM DEEP POWER-DOWN	RELEASE FROM DEEP POWER-DOWN and READ ELECTRONIC SIGATURE

READ Commands

The READ/FAST READ command set for the N25Q and EN25Q devices is identical. However, the EN25Q device does not have the QUAD OUTPUT FAST READ command.

Execute-in-Place (XIP)

The N25Q device enters and exits XIP via volatile and nonvolatile configuration register settings. The nonvolatile configuration register sets XIP mode at power-on of the device. Once enabled, XIP management in the N25Q matches that of the EON XIP usage mode. EON uses two confirmation nibbles to enter or exit XIP mode. The solution is fully compatible with the N25Q XIP methodology; other bits are don't care. The table below compares XIP read configuration at power-on for both devices.

Table 6: XIP Mode at Power-On

Read Configuration	N25Q	EN25Q
FAST READ	Yes	N/A
DUAL OUTPUT FAST READ	Yes	N/A
DUAL I/O FAST READ	Yes	N/A
QUAD OUTPUT FAST READ	Yes	N/A
QUAD I/O FAST READ	Yes	Yes

Figure 1: XIP Timing Configuration

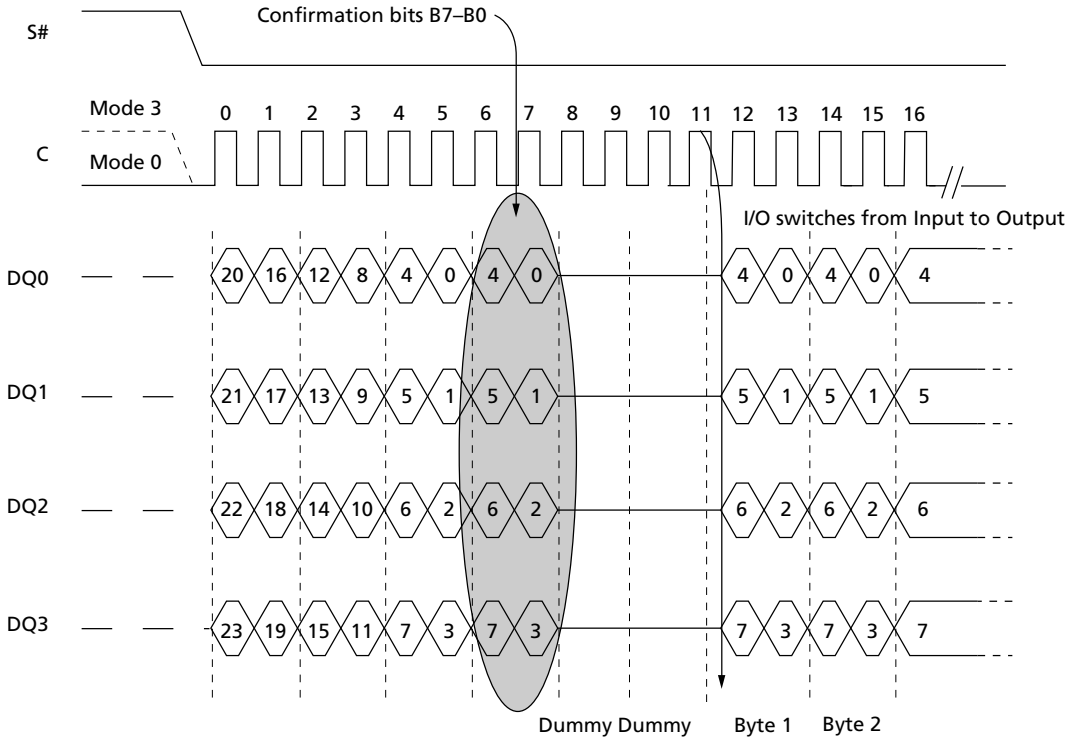


Table 7: XIP Confirmation Bit Software Commands

XIP Confirmation Bit	N25Q	EN25Q
Enter/confirm XIP mode	B4 = 0 (B7–B5 and B3–B0 = "Don't Care")	B7 ≠ B3 and B6 ≠ B2 and B5 ≠ B1 and B4 ≠ B0
Exit XIP mode	B4 = 1 (B7–B5 and B3–B0 = "Don't Care")	B7 = B3 or B6 = B2 or B5 = B1 or B4 = B0

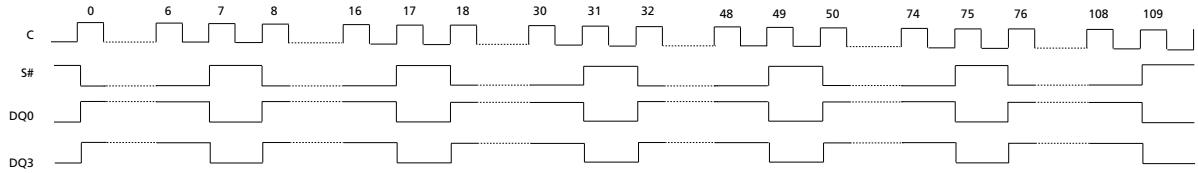
Reset Algorithm

The N25Q device can be reset using the following procedure, which must be completed in the order described: Reset XIP and Reset Dual SPI. (This procedure is necessary because when power loss occurs, the device may start in an undertermined state [XIP or an unnecessary protocol].) During the entire sequence, ^{t}SHSL2 must be at least 50ns.

Reset XIP

Below is the RESET sequence for all possible XIP configurations (QUAD I/O, DUAL I/O, and FAST READ).

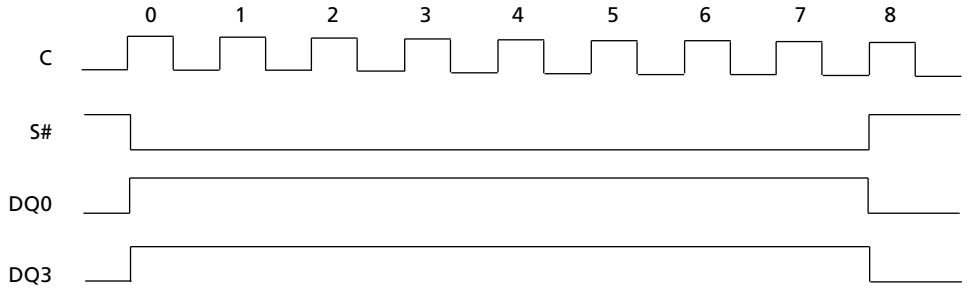
Figure 2: Reset XIP



Reset Dual SPI

Exit from DUAL or QUAD SPI protocol using the following FFh sequence.

Figure 3: Reset DUAL SPI



Electrical Characteristics

Table 8: DC Current Characteristics

Parameter	Symbol	N25Q		EN25Q		Unit
		Min	Max	Min	Max	
Standby current	I_{CC1}	–	100	–	20	µA
Operating current (FAST READ QUAD I/O)	I_{CC3}	–	20	–	20	mA
Operating current (PAGE PROGRAM)	I_{CC4}	–	20	–	28	mA
Operating current (WRITE STATUS REGISTER)	I_{CC5}	–	20	–	18	mA
Operating current (ERASE)	I_{CC6}	–	20	–	25	mA

Table 9: DC Voltage Specifications

Parameter	Symbol	N25Q		EN25Q		Unit
		Min	Max	Min	Max	
Input low voltage	V_{iL}	-0.5	0.3 V_{CC}	-0.5	0.2 V_{CC}	V
Input high voltage	V_{iH}	0.7 V_{CC}	V_{CC} + 0.4	0.7 V_{CC}	V_{CC} +0.4	V
Output low voltage	V_{OL}	–	0.4	–	0.4	V
Output high voltage	V_{OH}	V_{CC} -0.2	–	V_{CC} -0.2	–	V

AC Characteristics

Table 10: AC Specifications

AC specifications compare the fastest versions available at the full voltage range (2.7-3.6V).

Parameter	Symbol	Alternate Symbol	N25Q		EN25Q		Unit
			Min	Max	Min	Max	
Clock frequency (x1 FAST READ)	^{f}C	^{f}C	–	108	–	80	MHz
Clock frequency (x2, x4 FAST READ)	^{f}C	^{f}C	–	108	–	80	MHz
Clock frequency (READ)	^{f}R	^{f}R	–	54	–	50	MHz
S# active setup time	$^{t}SLCH$	^{t}CSS	4	–	5	–	ns
Data-in setup time	$^{t}DVCH$	^{t}DSU	2	–	2	–	ns
Data-in hold time	$^{t}CHDX$	^{t}DH	3	–	5	–	ns
S# deselect time after correct READ (ARRAY READ to ARRAY READ)	$^{t}SHSL$	^{t}CSH	50	–	50	–	ns
Output disable time (2.7–3.6V)	$^{t}SZQZ$	^{t}DIS	–	8	–	6	ns
Clock low to output valid (30pF)	$^{t}CLQV$	^{t}V	–	7	–	10	ns
Output hold time	$^{t}CLQX$	^{t}HO	1	-	0	–	ns
HOLD to output Low-Z	$^{t}HHQZ$	^{t}LZ	–	8	–	6	ns
HOLD to output High-Z	$^{t}HLQZ$	^{t}HZ	–	8	–	6	ns

Program and Erase Specifications

Table 11: Program and Erase Specifications

Operation	N25Q		EN25Q		Unit
	Typ	Max	Typ	Max	
PAGE PROGRAM (256 bytes)	0.5	5	0.8	5	ms
4KB SUBSECTOR ERASE	0.3	1.5	0.05	0.3	s
64KB SECTOR ERASE	0.7	3	0.4	2	s
BULK ERASE	240	480	100	280	s

Configuration and Memory Map

Table 12: Sectors and Subsectors

Sector	Subsector	Address Range	
		Start	End
511	8191	01FF F000h	01FF FFFFh
	:	:	:
	8176	01FF 0000h	01FF 0FFFh
:	:	:	:
255	4095	00FF F000h	00FF FFFFh
	:	:	:
	4080	00FF 0000h	00FF 0FFFh
:	:	:	:
127	2047	007F 0000h	007F 0FFFh
	:	:	:
	2032	007F 0000h	007F 0FFFh
:	:	:	:
63	1023	003F F000h	003F FFFh
	:	:	:
	1008	003F 0000h	003F 0FFFh
:	:	:	:
0	15	0000 F000h	0000 FFFFh
	:	:	:
	0	0000 0000h	0000 0FFFh

Device Identification

Manufacturer identification is assigned by JEDEC. As a result, the N25Q and EN25Q devices have a different manufacturer ID, memory type code, and method for reading information.

N25Q has a unique ID (UID) composed of 17 read-only bytes, which contain the following data:

- The first byte is set to 10h.
- The next two bytes of extended device ID specify device configuration (top, bottom, or uniform architecture and hold or reset functionality).
- The next 14 bytes contain optional customized factory data. The customized factory data bytes are factory programmed. Refer to the N25Q 256Mb data sheet for more information.

For the EN25Q device, you can access information using one of the following codes: ABh, 90h, or 9Fh. Code 9Fh provides complete information.

Table 13: Read Identification Summary

Parameter	N25Q Code	EN25Q Code
Manufacturer ID	20h	12h
Memory type	BAh	70h
Memory capacity	19h	19h

Conclusion

Comparing features of the Micron N25Q 256Mb and EN25Q Flash memory devices enables users to migrate applications from the EN25Q to the N25Q 256Mb device.

Revision History

Rev. A – 8/12

- Initial release

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