How to migrate to Numonyx® Axcell™ M29EW (MLC) from Spansion flash (S29GL 256-Mbit, 512-Mbit, 1-Gbit and S70GL 2-Gbit)

Application Note - 108109

Jun 2010

Revision History

Date of Revision	Revision	Description
Jul 2008	Rev00	Initial Release
Aug 2008	Rev01	Added *Section 2.2.5 Incompatibility of stacked 512Mbit M29EW device* Added Device ID for 512M and 1G density in *Table 8: Autoselect Information Comparison (16-bit mode)*
Oct 2008	Rev02	Added compatibility information of the conversion from S29GL-N to M29EW in all sections Re-organized the document structure Removed *Section 2.2.5 Incompatibility of stacked 512Mbit M29EW device* Added $I_{CCR}/I_{CCW}/I_{CCE}$ comparison
Feb 2009	Rev03	Added Axcell™ brand name Added 1-Gbit and 512-Mbit device information
Jun 2010	Rev04	Added Typical Single Word Program, Typical Block Erase Time and Available densities in *Table 1: Major Feature Comparison* Updated Typical Program Speed with full buffer information in *Table 1: Major Feature Comparison* Added *Figure 1: M29EW (MLC) 64-Ball Fortified BGA Ball Layout (top and bottom views)* and *Figure 2: M29EW (MLC) 56-Lead TSOP Pin Layout* Added *Section 3.1: Signal Description Difference* Added *Section 3.2: Mechanical Comparison* Added 2-Gbit information in *Table 4: ICC Comparison* Added *Section 3.5: Device Capacitance Difference* Updated Typical Program Speed with Full Buffer information in *Table 6: Write Performance Comparison* Added a note to state 15µs delay after Error bit (DQ5) set to issue Read/Reset command (F0h). Added NVPBs Clear Time, Erase to Suspend, Erase and Program Suspend Latency information in *Table 6: Write Performance Comparison* Updated some timings in *Table 7: Power-on and Reset Timing Comparison* Added Device ID for 2G density in *Table 8: Autoselect Information Comparison (16-bit mode)* Added *Section 5.3: CFI Difference* Added *Section 5.5: Power-Loss Recovery* Updated Order Number and Document/Tool in *Section Appendix A: Additional Information*

1 Introduction

This application note describes how to convert a system design from Spansion S29GL (including P series and N series) and S70GL-P Flash to Numonyx® Axcell™ M29EW (MLC) Flash.

This document was written based on device information available at the time. The 256-Mbit, 512-Mbit, 1-Gbit and 2-Gbit MLC M29EW Datasheet may override this application note if there is a different description for the same items in the datasheet.

Note: MLC in this document refers to Multi-Level Cell.

Spansion 2-Gbit Flash is S70GL-P, which is S29GL-P 1-Gbit/1-Gbit stack, so 2-Gbit is still put under S29GL-P in this document.

2 Brief Comparison

The M29EW (MLC) flash memory device is manufactured on leading 65nm process lithography and is compatible to the S29GL flash memory device. *Table 1* is a major feature comparison between the three devices.

Table 1. Major Feature Comparison

Features	M29EW (MLC)	S29GL-P	S29GL-N
Process Technology	65nm MLC	90nm Mirror-bit	110nm Mirror-bit
Available densities(1)	256-Mbit 512-Mbit 1-Gbit 2-Gbit	256-Mbit 512-Mbit 1-Gbit 2-Gbit	256-Mbit 512-Mbit
Package	64-Ball Fortified BGA 56-Lead TSOP	64-Ball Fortified BGA 56-Lead TSOP	64-Ball Fortified BGA 56-Lead TSOP
Block Architecture	Uniform 128KB	Uniform 128KB	Uniform 128KB
Page Read Size	16-Word	8-Word	8-Word
Program Buffer Size (maximum)	512-Word	32-Word	16-Word
Single Word Program (typical)	210µs per Word	60µs per Word	60µs per Word
Program Speed with full buffer (typical)	1.76µs per Word	15µs per Word	15µs per Word
Random Access Time(2)	1.8V V_{CCQ}: 100ns 3.0V V_{CCQ}: 95ns	1.8V V_{CCQ}: 130ns (2-Gbit), 110ns (others) 3.0V V_{CCQ}: 120ns (2-Gbit), 100ns (others)	1.8V V_{CCQ}: 110ns 3.0V V_{CCQ}: 100ns
Block Erase Time (typical)	0.8s	0.5s	0.5s
Extended Memory Block	128 Words	128 Words	128 Words
Support for Common Flash Interface	Yes	Yes	Yes
Hardware Protection of Highest or Lowest Block	Yes	Yes	Yes
Software Protection and Password Protect	Yes	Yes	Yes
Password Access	Yes	No	No

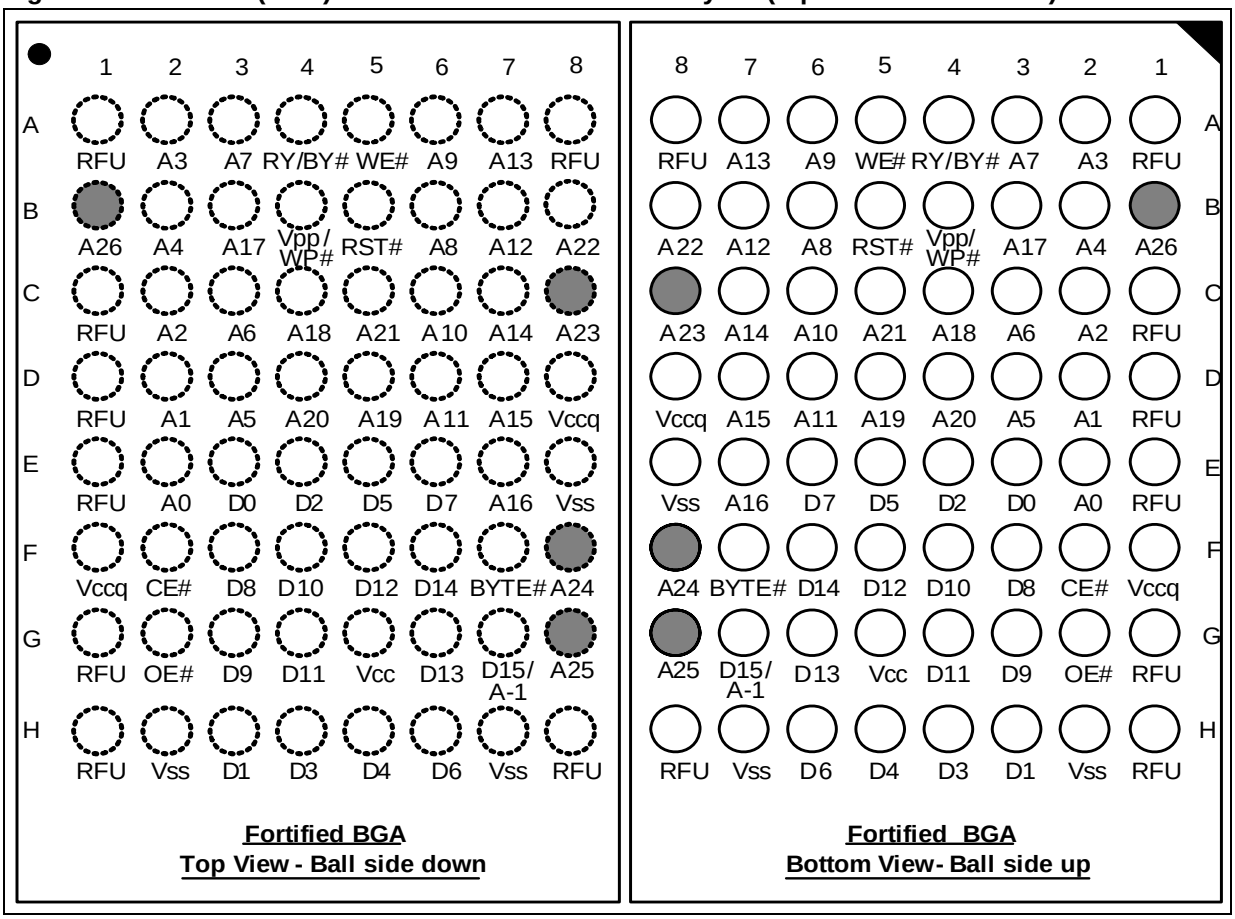
1. Only BGA package is available for 2-Gbit density.
2. The random access time of M29EW device varies according to package: BGA (3V: 95ns and 1.8V: 100ns) and TSOP (3V: 105ns and 1.8V: 110ns).

3 Hardware Considerations

The M29EW device is available in two packages, 56-TSOP and 64-Fortified BGA. For compatibility, the Pin/Ball layouts and physical dimensions are equivalent to the S29GL Flash devices.

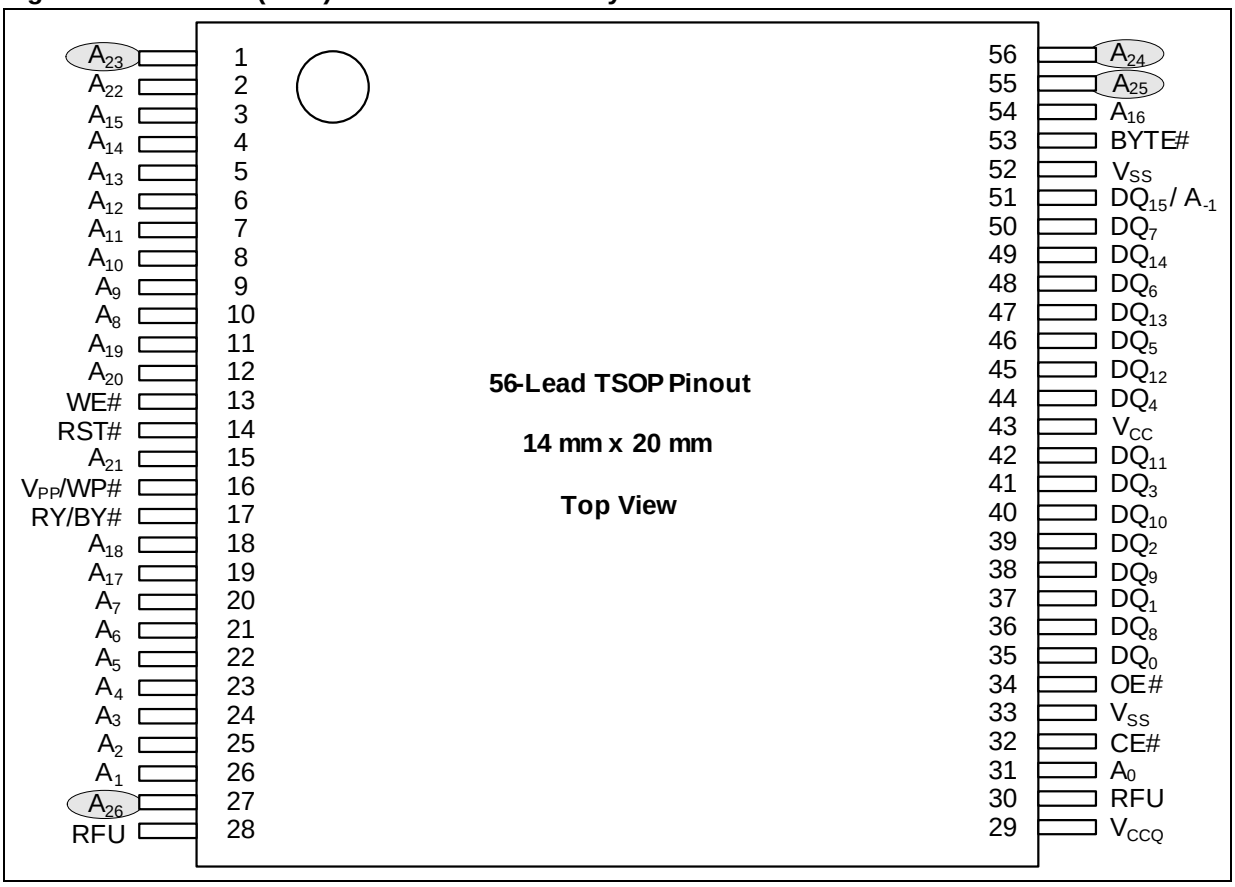
Figure 1, *Figure 2* show the ball/pin details of all packages.

Figure 1. M29EW (MLC) 64-Ball Fortified BGA Ball Layout (top and bottom views)



1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256-Mbit density and above; otherwise, it is RFU.
3. A24 is valid for 512-Mbit density and above; otherwise, it is RFU.
4. A25 is valid for 1-Gbit density and above; otherwise, it is RFU.
5. A26 is valid for 2-Gbit (1-Gbit/1-Gbit stack) density only; otherwise it is RFU.
6. RFU = Reserved for Future Use. These locations can be treated as NC (no connect).

Figure 2. M29EW (MLC) 56-Lead TSOP Pin Layout



1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256-Mbit density and above; otherwise, it is RFU.
3. A24 is valid for 512-Mbit density and above; otherwise, it is RFU.
4. A25 is valid for 1-Gbit density and above; otherwise, it is RFU.
5. A26 is reserved for 2-Gbit.
6. RFU = Reserved for Future Use. These locations can be treated as NC (no connect).

3.1 Signal Description Difference

Table 2 compares between the M29EW (MLC) and S29GL signals. On both devices, V_{PP} allows the use of an external high voltage to improve programming time. The Write Protect (WP#) function provides a hardware method of protecting the highest or lowest blocks.

The highest or lowest block of M29EW (MLC) and S29GL are protected when V_{PP} /WP# is V_{IL}.

When V_{PP} /WP# is V_{IH}, the memory reverts to its previous status of the highest or lowest block protected.

The M29EW (MLC) and S29GL devices automatically enter Unlock Bypass mode when V_{PP} /WP# is raised to V_{PPH}.

Table 2. Signal Description Comparison

Name		Description	Direction
M29EW (MLC)	**S29GL**		
A[max:0]		Address inputs	Input
DQ[7:0]		Data inputs/outputs	I/O
DQ[14:8]		Data inputs/outputs	I/O
DQ15/A-1		Data input/output or address input	I/O or input
CE#		Chip Enable	Input
OE#		Output Enable	Input
WE#		Write Enable	Input
RST#	RESET#	Reset	Input
RY/BY#		Ready/Busy	Output
BYTE#		Byte/word organization select	Input
V_{CCQ}	V_{IO}	Input/output buffer supply voltage	Supply
V_{CC}		Supply voltage	Supply
V_{PP}/WP#	WP#/ACC	Acceleration Input/Write Protect	Input
V_{SS}		Ground	-
NC		No connect	-

3.2 Mechanical Comparison

The M29EW (MLC) and S29GL 56-Lead TSOP packages have the same mechanical dimensions.

The M29EW (MLC) and S29GL 64-Ball Fortified BGA packages have the same mechanical dimensions.

3.3 Autoselect Entry Comparison

M29EW (MLC) does not support V_{HH} on address A9. Instead, use command sequence (AAh/55h/90h) to enter Autoselect mode. Applying 12V on A9 may damage the M29EW (MLC) device. S29GL devices support both methods to enter Autoselect mode.

Table 3. Autoselect Entry Comparison

Autoselect Entry Method	M29EW (MLC)	S29GL-P	S29GL-N
12V on A9 input	No	Yes	Yes
Entry Command (90h)	Yes	Yes	Yes

3.4 I_{CC} Difference

Table 4 compares the I_{CC} values for the M29EW (MLC) and S29GL devices. The higher I_{CCS} of M29EW (MLC) is offset by its lower I_{CCR}, I_{CCW} and I_{CCE} specs.

Table 4. I_{CC} Comparison

Symbol	M29EW (MLC)				S29GL-P		S29GL-N		Unit
	Density	Test condition	Typ	Max	Typ	Max	Typ	Max	
ICCS	256-Mbit	CE# = VCCQ = ± 0.2 V RST# = VCCQ = ± 0.2 V	65	210	1	5	1	5	µA
	512-Mbit		70	225					
	1-Gbit		75	240			-	-	
	2-Gbit		150	480	2	10			
ICCR	All	Random read, f = 5MHz	26	31	30	55	30	50	mA
ICCW ICCE	All	VPP/WP# = V_{IL} or V_{IH}	35	50	50	90	50	90	
		VPP/WP# = V_{PPH}	35	50	50	80	50	90	

3.5 Device Capacitance Difference

Table 5 compares the input/output capacitance differences between M29EW (MLC) and S29GL.

Table 5. Capacitance Comparison

Symbol	Parameter	Test Condition			M29EW(MLC)		S29GL-P		S29GL-N		Unit
					Min	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0V	256-, 512-Mbit	TSOP	3	8	6	10	6.0	7.5	pF
			1-Gbit		4	9			-	-	
			2-Gbit		-	-	-	-			
			256-, 512-Mbit	BGA	3	8	6	10	4.2	5.0	
			1-Gbit		4	9			-	-	
			2-Gbit		8	18	12	20			
C_{OUT}	Output Capacitance	V_{OUT} = 0V	256-, 512-Mbit 1-Gbit	TSOP	2	5	10	12	8.5	12.0	
			2-Gbit		-	-	-	-	-	-	
			256-, 512-Mbit 1-Gbit	BGA	2	5	10	12	5.4	6.5	
			2-Gbit				20	24	-	-	

4 Performance Differences

The M29EW (MLC) device has better program performance vs. S29GL devices.

4.1 Write Performance

The M29EW (MLC) has a larger program buffer than the S29GL-P and S29GL-N devices. Modifying system software will greatly improve system performance. *Table 6* compares buffer sizes and typical write performance between the three devices.

Note: A Read/Reset command (F0h) must be issued with 15µs delay after the Error bit (DQ5) is set during Program/Erase operations.

Table 6. Write Performance Comparison

Description	M29EW (MLC)	S29GL-P	S29GL-N
Program Buffer Size	512-word	32-word	16-word
Typical Program Speed with Full Buffer	1.14MB/s	0.148MB/s	0.148MB/s
NVPBs(1) Clear Time	0.8s	-	-
Erase Suspend Latency	27µs(typ)/32µs(max)	5µs(typ)/20µs(max)	5µs(typ)/20µs(max)
Program Suspend Latency	27µs(typ)/32µs(max)	5µs(typ)/15µs(max)	5µs(typ)/20µs(max)
Erase to Suspend	500µs(typ)	-	-

1. NVPB = Non-Volatile Protection Bit.

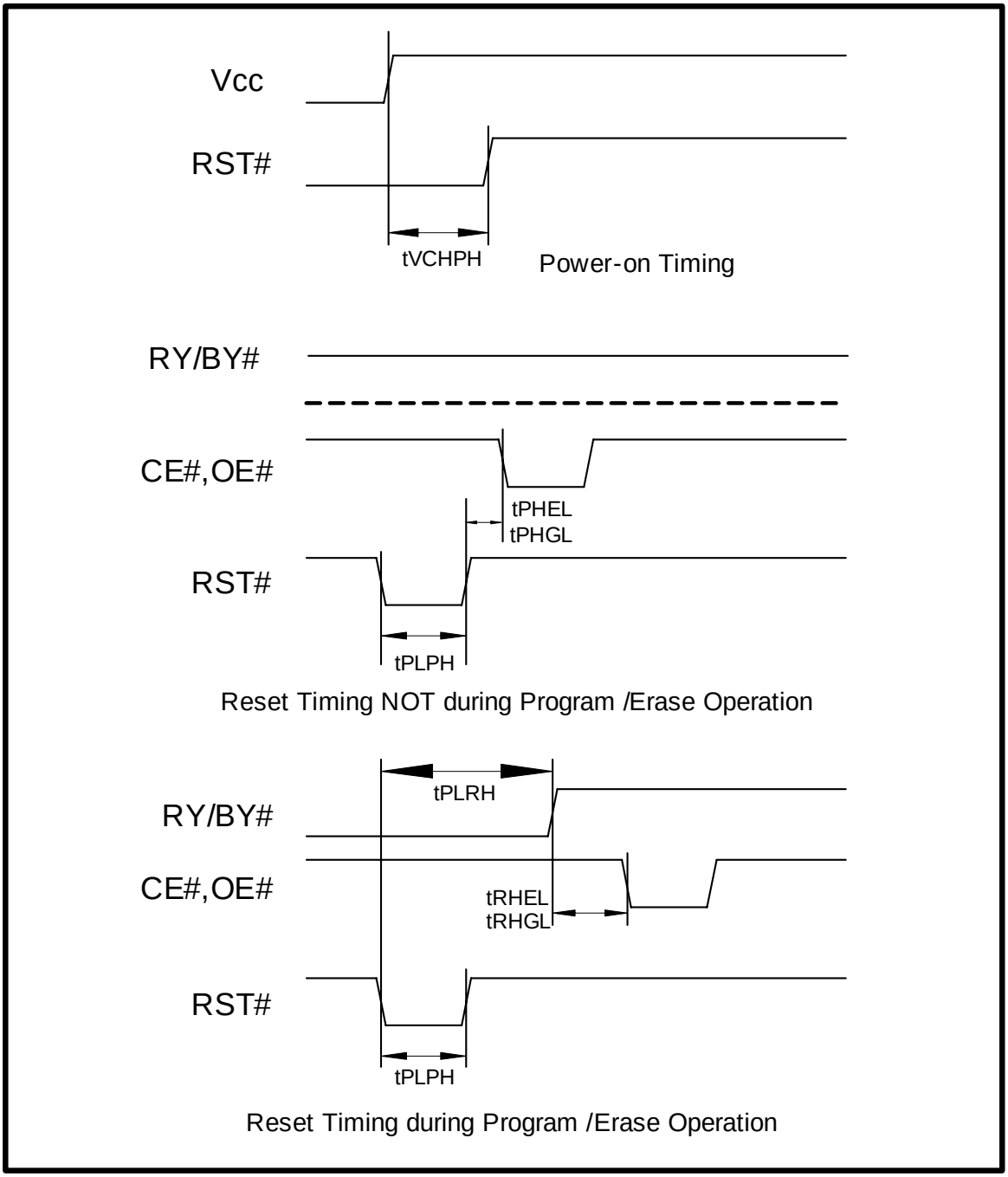
4.2 Power-on and Reset Timings

Table 7 compares the differences in power-on and reset timing specifications between M29EW (MLC) and S29GL-P, S29GL-N devices. Many of the common processors support the M29EW (MLC) timings; in those cases there should be no impact.

Table 7. Power-on and Reset Timing Comparison

Symbol	Alt.	Parameter	Min/Max	M29EW (MLC)	S29GL-P	S29GL-N
t_{VCHPH}	t_{VCS}	V_{CC} power valid to Reset# high (Min)	Min	300µs	35µs	50µs
t_{PLRH}	t_{READY}	Reset# low to read mode, during Program or Erase	Max	32µs	35µs	20µs
t_{PLPH}	t_{RP}	Reset# pulse width	Min	100ns	35µs	500ns
t_{PHEL} t_{PHGL}	t_{RH}	Reset# high to Chip Enable low, Output Enable low	Min	50ns	200ns	50ns
t_{RHEL} t_{RHGL}	t_{RB}	RY/BY# high to Chip Enable low, Output Enable low	Min	0ns	0ns	0ns

Figure 3. Power-on and Reset Timing Sequences



5 Software Considerations

The command set of M29EW (MLC) flash is fully compatible with that of S29GL-P/S29GL-N devices. Therefore, no command change in software is required to accommodate M29EW (MLC) flash.

5.1 Manufacturer ID and Other Autoselect Information

Numonyx and Spansion have different Manufacturer IDs, Protection Register Indicators, therefore, a slight modification in the software is required during migration.

Table 8 outlines the differences of Autoselect information.

Table 8. Autoselect Information Comparison (16-bit mode)

Description			Address	M29EW (MLC)	S29GL-P	S29GL-N
Manufacturer ID			(Base)+00h	0089h	0001h	0001h
Device ID Cycle 1			(Base)+01h	227Eh	227Eh	227Eh
Device ID cycle 2		256-Mbit	(Base)+0Eh	2222h	2222h	2222h
		512-Mbit		2223h	2223h	2223h
		1-Gbit		2228h	2228h	-
		2-Gbit		2248h	2248h	-
Device ID cycle 3			(Base)+0Fh	0001h	0001h	0001h
Protection Register Indicator	V_{PP}/WP # Locks Highest Block	Factory Locked	(Base)+03h	0099h	0099h	0098h
		Factory Unlocked		0019h	0019h	0018h
	V_{PP}/WP # Locks Lowest Block	Factory Locked		0089h	0089h	0088h
		Factory Unlocked		0009h	0009h	0008h
Block Protection		Unprotected	(Base)+02h	0000h	0000h	0000h
		Protected		0001h	0001h	0001h

Note: For the security device (M29EW-S), the Device ID is different from the regular part; please contact your local Numonyx or distribution sales office to request the M29EW-S Security Feature Addendum.

5.2 Unlock Bypass Mode

In Unlock Bypass mode, the use of Autoselect mode is not recommended on M29EW device. If existing software is using Autoselect Entry command (90h) to read information in Unlock Bypass mode, an additional F0h command must be issued after Autoselect read to return Unlock Bypass mode.

S29GL series devices don't have this requirement.

5.3 CFI Difference

CFI differences exist between M29EW (MLC) and S29GL-P/S29GL-N due to device features and performance characteristics.

Table 9 outlines the relevant information.

Table 9. CFI Difference Comparison

Address (HEX)	Description	M29EW (MLC) (HEX)		S29GL-P (HEX)	S29GL-N (HEX)
1D	V_{PPH} [programming] supply minimum Program / Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	00B5		0000	0000
1E	V_{PPH} [programming] supply maximum Program / Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	00C5		0000	0000
1F	Typical time-out for single byte/word program = 2^n µs	0009		0006	0007
20	Typical time-out for maximum size buffer program = 2^n µs	000A		0006	0007
21	Typical time-out for individual block erase = 2^n ms	000A		0009	000A
22	Typical time-out for full Chip Erase = 2^n ms	256M	0012	0013	0000
		512M	0013		
		1G	0014		
		2G	0015		
23	Maximum time-out for byte/word program = 2^n times typical time-out	0001		0003	0003
24	Maximum time-out for buffer program = 2^n times typical time-out	0002		0005	0005
25	Maximum time-out per individual block erase = 2^n times typical time-out	0002		0003	0004
26	Maximum time-out for Chip Erase = 2^n times typical time-out	0002		0002	0000
2A 2B	Maximum number of byte in multiple-byte write = 2^n	000A 0000		0006 0000	0005 0000
45	Address Sensitive Unlock (Bits 1 to 0) 0 = Required, 1 = Not Required Silicon revision number (Bits 7 to 2)	0018		0014	0010

5.4 Password Access

Password Access is a security enhancement offered on the M29EW (MLC) device. This feature protects information stored in the main-array blocks by preventing content alteration or reads until a valid 64-bit password is received. Password Access may be combined with Non-Volatile and/or Volatile Protection to create a multi-tiered solution.

S29GL-P and S29GL-N series devices don’t support this feature.

Please contact your Numonyx sales representatives for further details concerning Password Access feature.

5.5 Power-Loss Recovery

It is recommended that the user enable robust power-loss recovery in software system, especially during the flash write operations. Please refer to the Application Note 309046 for details.

Appendix A Additional Information

Order Number	Document / Tool
208045	Numonyx® Axcell™ M29EW 256-Mbit, 512-Mbit, 1-Gbit, 2-Gbit (x8 or x16, uniform block) 3V Supply Flash Memory Datasheet
S29GL-P_00	SPANSION® MirrorBit® S29GL-P 1-Gbit, 512-Mbit, 256-Mbit, 128-Mbit 3.0 Volt-only Page Mode Flash Memory Datasheet
S29GL-N_00	SPANSION® MirrorBit® S29GL-N 512-Mbit, 256-Mbit, 128-Mbit 3.0 Volt-only Page Mode Flash Memory Datasheet
S70GL-P_02	SPANSION® MirrorBit® S70GL-P 2-Gbit 3.0 Volt-only Page Mode Flash Memory Datasheet
309046	Application Note: Power Loss Recovery for NOR Flash Memory

Notes:
1. Contact your local Numonyx or distribution sales office to request Numonyx documentation.
2. Visit the Numonyx World Wide Web home page at http://www.Numonyx.com for further information, technical documentation and tools.

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