How to migrate to Numonyx® Axcell™ M29EW (SBC) from Spansion S29GL flash (32-, 64- and 128-Mbit)

Application Note - 309014

May 2010

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Revision History

Date of Revision	Revision	Description
Jun 2009	Rev01	Initial Release
May 2010	Rev02	Updated density to include 32M, 64M and 128M. Updated package, block Architecture information in *Table 1: General Feature Comparison*. Added 48B BGA and 48L TSOP layout information in *Section 3: Hardware Considerations*. Added Signal description comparison at *Section 3.1: Signal Description Difference*. Updated TSOP major dimension comparison in *Table 3: TSOP Dimension Comparison*. Updated I_{CC} comparison information in *Table 4: ICC Comparison*. Updated capacitance comparison information in *Table 5: Capacitance Comparison*. Added a note to state 1µs delay after Error bit (DQ5) set to issue Read/Reset command (F0h). Updated write performance information in *Table 6: Write Performance Comparison*. Updated power-on and reset timing Comparison information in *Table 7: Power-on and Reset Timing Comparison*. Update autoselect information comparison information in *Table 8: Autoselect Information Comparison (16-bit mode)*. Added Autoselect Entry Comparison at *Section 5.2: Autoselect Entry Comparison*. Updated CFI difference comparison information in *Table 10: CFI Difference Comparison*. Added order number and document/tool information in *Section Appendix A: Additional Information*. Added the power-loss recovery in *Section 5.5: Power-Loss Recovery*.

1 Introduction

This application note describes how to convert a system design from Spansion S29GL (including P series and N series) Flash to Numonyx® Axcell™ M29EW (SBC) Flash.

This document was written based on device information available at the time. The 32-, 64- and 128-Mbit SBC M29EW Datasheet may override this application note if there is a different description for the same items in the datasheet.

Note: SBC in this document refers to Single Bit per Cell.

2 Brief Comparison

The M29EW (SBC) flash memory device is manufactured on leading 65nm process lithography and is compatible to S29GL flash memory device. *Table 1* is a major feature comparison between the three devices.

Table 1. General Feature Comparison

Features	M29EW (SBC)		S29GL-P	S29GL-N	
Process Technology	65nm SBC		90nm Mirror-bit	110nm Mirror-bit	
Package	64-Ball Fortified BGA 48-Ball BGA 56-Lead TSOP 48-Lead TSOP		64-Ball Fortified BGA 56-Lead TSOP	64-Ball Fortified BGA 48-Ball BGA 56-Lead TSOP 48-Lead TSOP	
Block Architecture	128-Mbit	Uniform 128KB	Uniform 128KB (128-Mbit only)	128-Mbit	Uniform 128KB
	64-Mbit	Uniform 64KB		64-Mbit	Uniform 64K
		Boot: 64KB (main block) and 8KB (boot block)			Boot: 64KB (main block) and 8KB (boot block)
	32-Mbit	Uniform 64KB		32-Mbit	Uniform 64K
		Boot: 64KB (main block) and 8KB (boot block)			Boot: 64KB (main block) and 8KB (boot block)
Page Read Size	8-Word		8-Word	8-Word	
Max. Program Buffer Size	256-Word		32-Word	16-Word	
Typical Single Word Program	15µs per Word		60µs per Word	60µs per Word	
Typical Program Speed with full buffer	1.11µs per Word		15µs per Word	15µs per Word	
Random Access Time(1)	1.8V V_{CCQ}: 65ns 3.0V V_{CCQ}: 60ns		1.8V V_{CCQ}: 110ns 3.0V V_{CCQ}: 100ns	1.8V V_{CCQ}: 110ns 3.0V V_{CCQ}: 100ns	
Typical Block Erase Time	0.5s		0.5s	0.5s	
Extended Memory Block	128 Words		128 Words	128 Words	
Support for Common Flash Interface	Yes		Yes	Yes	
Hardware Protection of Highest/Lowest Block or Top/Bottom two Blocks	Yes		Yes	Yes	
Software Protection and Password Protect	Yes		Yes	Yes	
Password Access	Yes		No	No	

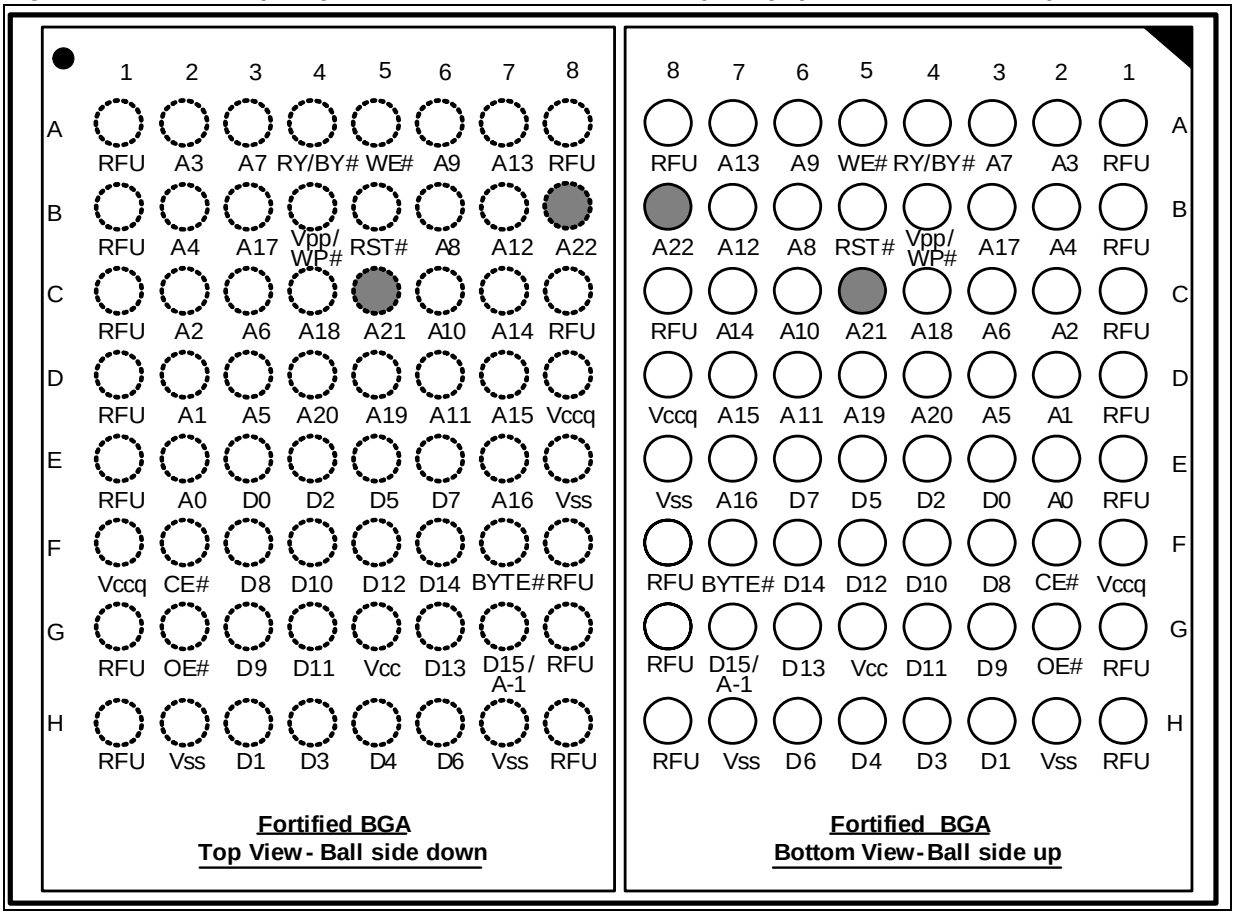
1. The random access time of M29EW device varies according to different packages: BGA (3V: 60ns and 1.8V: 65ns) and TSOP (3V: 70ns and 1.8V: 75ns).

3 Hardware Considerations

The M29EW (SBC) device is ball/pin compatible to the S29GL series flash, in the 64-Ball Fortified BGA, 48-Ball BGA, 56-Lead TSOP and 48-Lead TSOP packages.

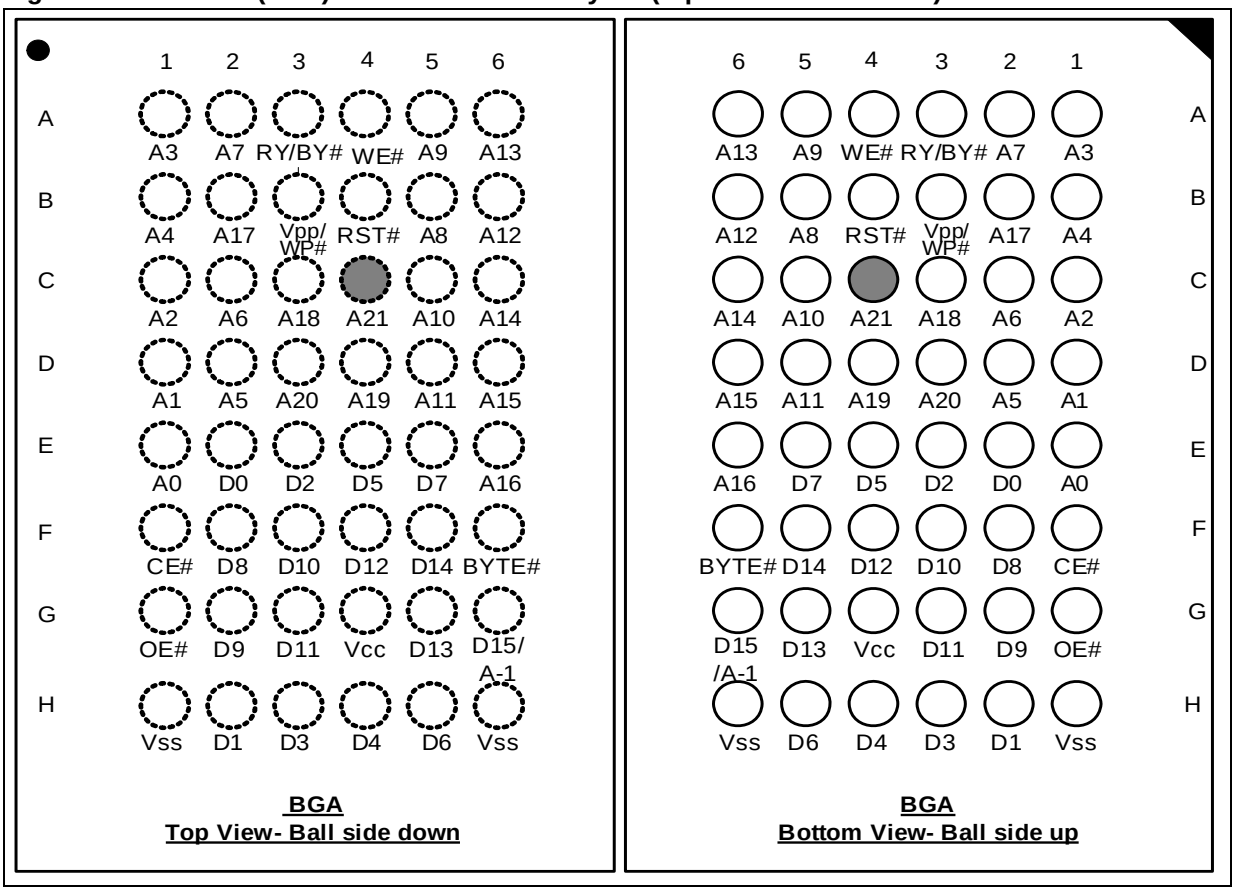
Figure 1, *Figure 2*, *Figure 3* and *Figure 4* show the ball/pin details of all packages.

Figure 1. M29EW (SBC) 64-Ball Fortified BGA Ball Layout (top and bottom views)



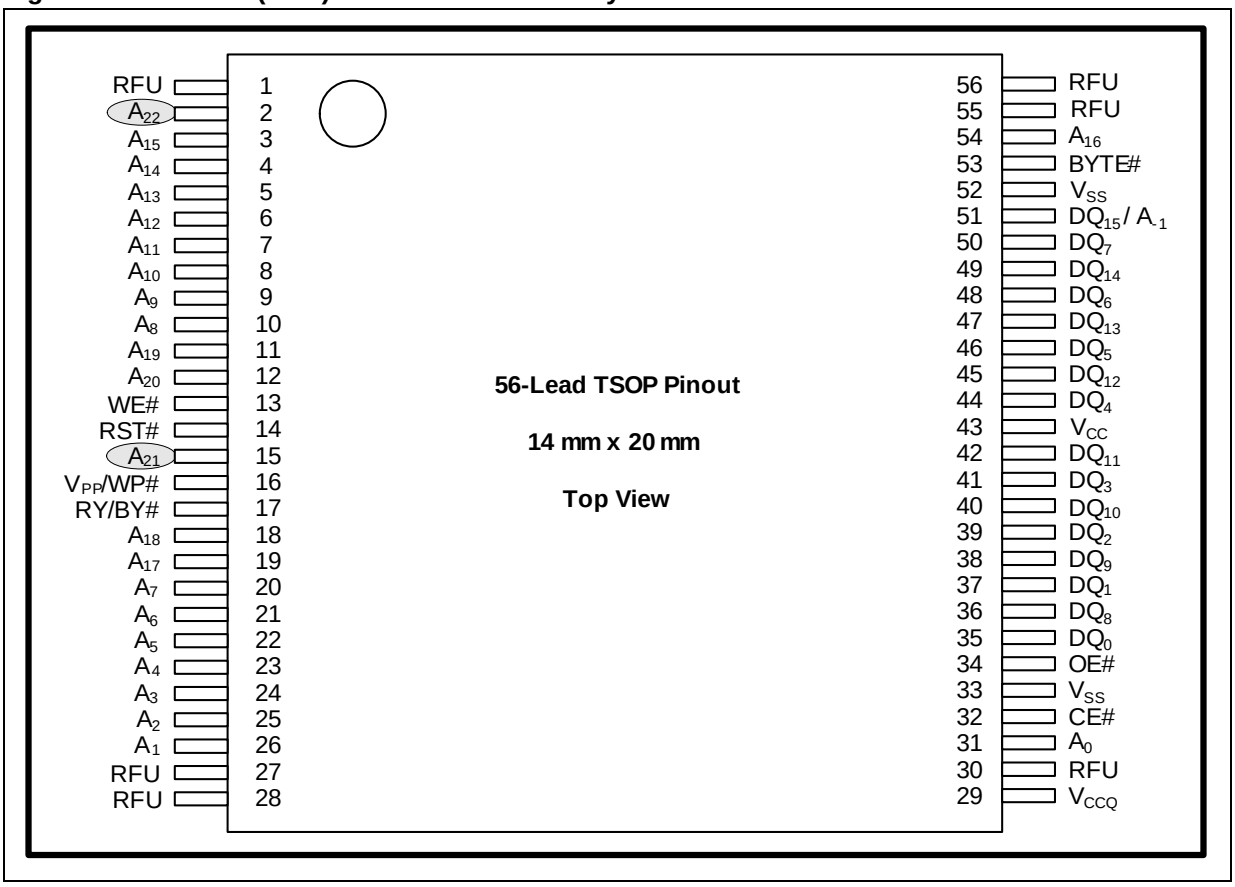
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64-Mbit density and above; otherwise, it is not connected internally but RFU.
3. A22 is valid for 128-Mbit density; otherwise, it is not connected internally but RFU.
4. RFU stands for Reserved for Future Use.

Figure 2. M29EW (SBC) 48-Ball BGA Ball Layout (top and bottom views)



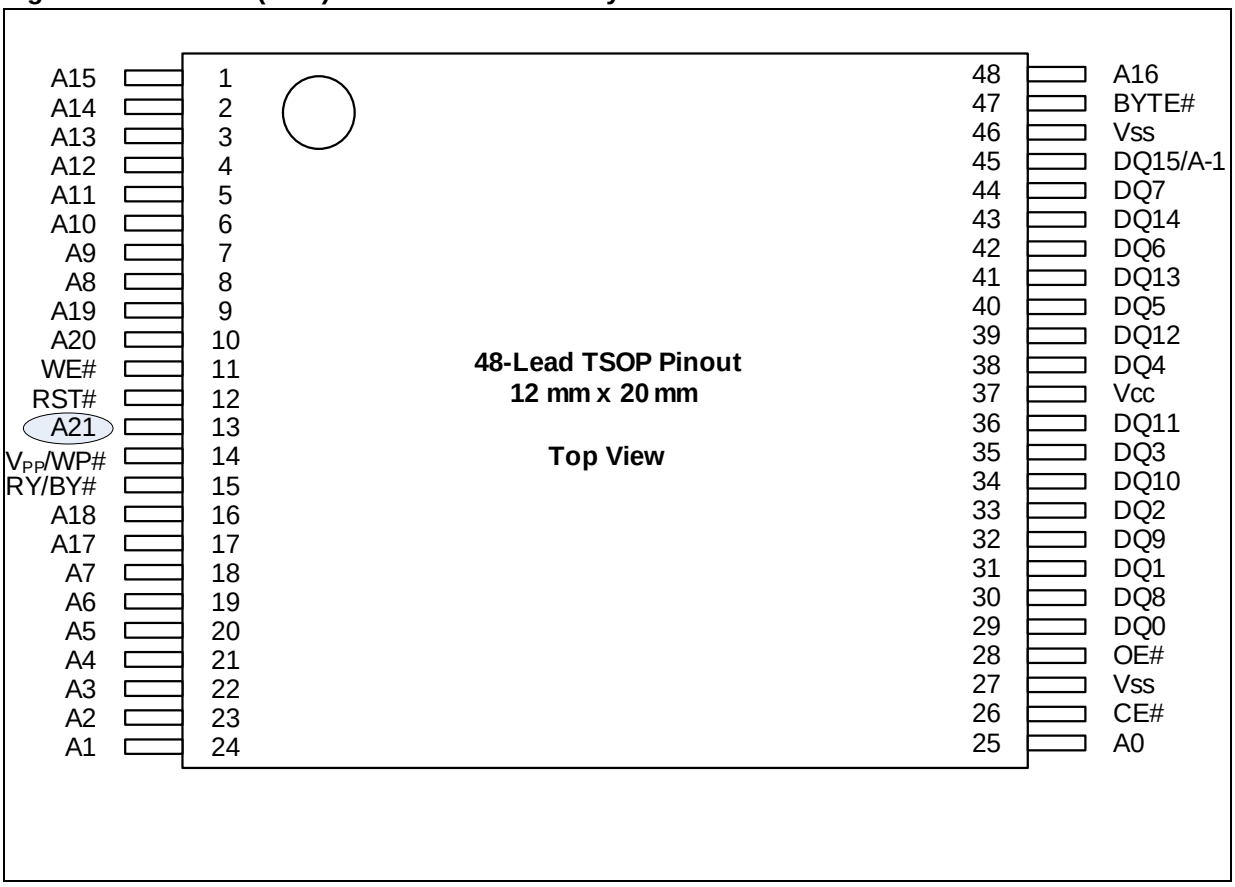
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64-Mbit density; otherwise, it is not connected internally but RFU.
3. RFU stands for Reserved for Future Use.

Figure 3. M29EW (SBC) 56-Lead TSOP Pin Layout



1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64-Mbit density and above; otherwise, it is not connected internally but RFU.
3. A22 is valid for 128-Mbit density; otherwise, it is not connected internally but RFU.
4. RFU stands for Reserved for Future Use.

Figure 4. M29EW (SBC) 48-Lead TSOP Pin Layout



1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64-Mbit density; otherwise, it is not connected internally but RFU.
3. RFU stands for Reserved for Future Use.

3.1 Signal Description Difference

Table 2 gives a comparison between the M29EW (SBC) and S29GL signals. On both devices, the V_{PP} function allows the memory to use an external high voltage power supply to reduce the time required for fast program operations. The Write Protect (WP) function provides a hardware method of protecting the highest, lowest, top two or bottom two blocks.

When V_{PP} /WP is Low, V_{IL}, the highest, lowest, top two or bottom two blocks are protected on both the M29EW (SBC) and S29GL devices.

When V_{PP} /WP is High, V_{IH}, the memory reverts to the previous protection status of the highest, lowest, top two or bottom two blocks.

When V_{PP} /WP# pin is raised to V_{PPH}, the memory automatically enters the Unlock Bypass mode for both the M29EW (SBC) and S29GL devices.

Table 2. Signal Description Comparison

Name		Description	Direction
M29EW (SBC)	S29GL		
A0-Amax(1)		Address inputs	Input
DQ0-DQ7		Data inputs/outputs	I/O
DQ8-DQ14		Data inputs/outputs	I/O
DQ15/A-1		Data input/output or address input	I/O or input
CE#		Chip Enable	Input
OE#		Output Enable	Input
WE#		Write Enable	Input
RST#	RESET#	Reset	Input
RY/BY#		Ready/Busy output	Output
BYTE#		Byte/word organization select	Input
V_{CCQ}	V_{IO}	Input/output buffer supply voltage	Supply
V_{CC}		Supply voltage	Supply
V_{PP}/WP#	WP#/ACC	Acceleration Input/Write Protect	Input
V_{SS}		Ground	-
NC		Not connected	-

1. A22, A21 and A20 are maximum address pins for 128-Mbit, 64-Mbit and 32-Mbit density respectively.

3.2 Mechanical Differences

The M29EW (SBC) 48-Lead TSOP package has the same mechanical dimensions as S29GL 48-Lead TSOP package.

The M29EW (SBC) 56-Lead TSOP package has a few mechanical dimensions that are different from S29GL 56-Lead TSOP package.

Table 3 shows the major dimension comparison between M29EW (SBC) and S29GL TSOP devices.

The M29EW (SBC) 64-Ball Fortified BGA package and 48-Ball BGA package have the same mechanical dimensions as S29GL 64-Ball Fortified BGA package and 48-Ball BGA package respectively.

Figure 5. 56-Lead TSOP and 48-Lead TSOP, package outline

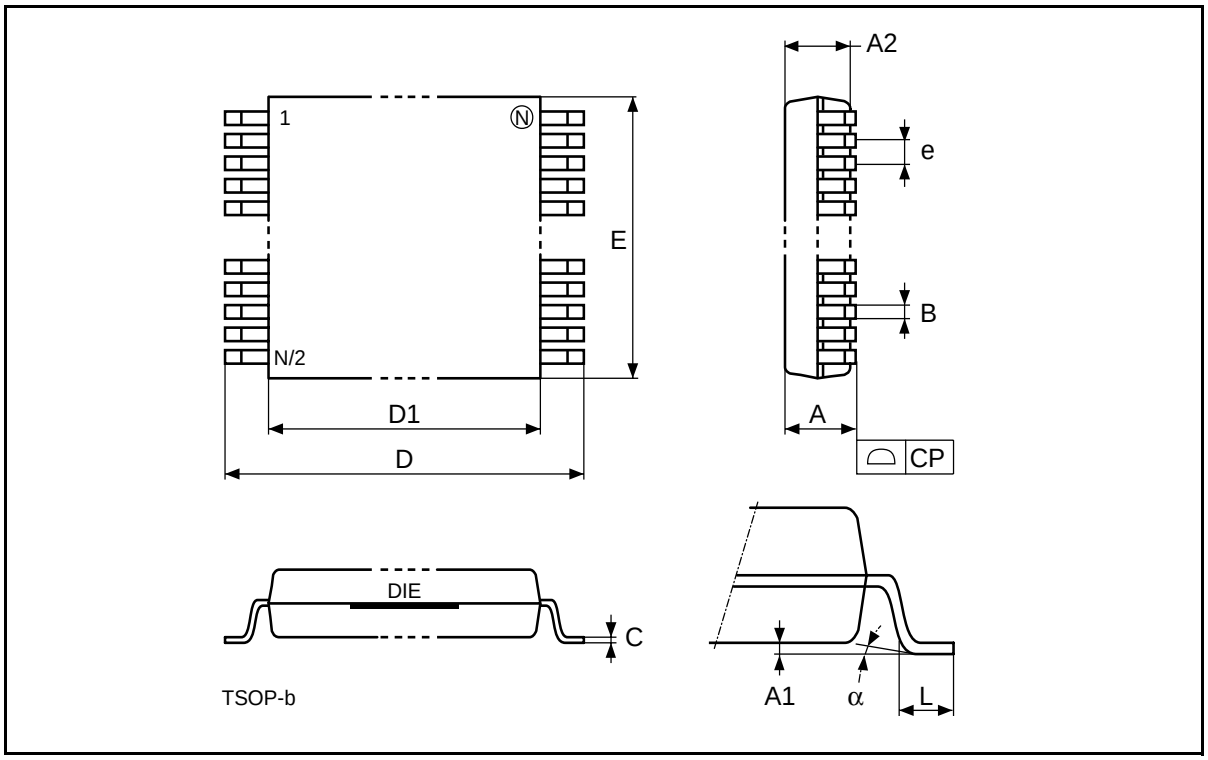


Table 3. TSOP Dimension Comparison

Symbol	M29EW (SBC) (Typical in millimeters)		S29GL-P (Typical in millimeters)		S29GL-N (Typical in millimeters)	
A2	56-Lead TSOP	0.995	56-Lead TSOP	1.00	56-Lead TSOP	1.00
	48-Lead TSOP	1.00			48-Lead TSOP	1.00
B	56-Lead TSOP	0.15	56-Lead TSOP	0.22	56-Lead TSOP	0.22
	48-Lead TSOP	0.22			48-Lead TSOP	0.22

3.3 I_{CC} Difference

Table 4 compares the I_{CC} values for the M29EW (SBC) and S29GL devices. The $I_{CCStandby}$ difference has minimal system impact because the lower I_{CCRead}, $I_{CCWrite}$, and $I_{CCErase}$ specs of M29EW (SBC) provide for better overall system power consumption.

Table 4. I_{CC} Comparison

Symbol	M29EW (SBC)				S29GL-P		S29GL-N		Unit
	Density	Test condition	Typ	Max	Typ	Max	Typ	Max	
$I_{CCStandby}$	128-Mbit	-	50	120	1	5	1	5	µA
	64-Mbit		35	120	-	-			
	32-Mbit		35	120					
I_{CCRead}	32- and 64-Mbit	Random read, f = 5MHz	20	25	-	-	25	30	mA
	128-Mbit				30	55	30	50	
$I_{CCWrite}$ $I_{CCErase}$	32- and 64-Mbit	V_{PP}/WP# = V_{IL} or V_{IH}	35	50	-	-	50	60	
	128-Mbit				50	90	50	90	
	32- and 64-Mbit	V_{PP}/WP# = V_{PPH}	26	33	-	-	50	60	
	128-Mbit				50	80	50	90	

3.4 Device Capacitance Difference

M29EW (SBC) flash has a different input/output capacitance, compared with S29GL flash. *Table 5* shows the detail comparison. The minor difference for Input/Output Capacitance won't impact customer's hardware.

Table 5. Capacitance Comparison

Symbol	Parameter	Test Condition		M29EW (SBC)		S29GL-P		S29GL-N			Unit
				Min	Max	Typ	Max	Density	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0V	TSOP	2	7	6	10	32- and 64-Mbit	6.0	10.0	pF
								128-Mbit	6.0	7.5	
			BGA					32- and 64-Mbit	TBD	TBD	
								128-Mbit	4.2	5.0	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	TSOP	2	5	10	12	32- and 64-Mbit	6.0	12.0	
								128-Mbit	8.5	12.0	
			BGA					32- and 64-Mbit	TBD	TBD	
								128-Mbit	5.4	6.5	

4 Performance Differences

The M29EW (SBC) device has better program performance vs. S29GL devices.

4.1 Write Performance

The M29EW (SBC) has a larger program buffer than the S29GL-P and S29GL-N devices. Modifying system software will greatly improve system performance. *Table 6* compares buffer sizes and typical write performance between the three devices.

Note: A Read/Reset command (F0h) must be issued with 1µs delay after the Error bit (DQ5) is set during Program/Erase operations.

Table 6. Write Performance Comparison

Description	M29EW (SBC)	S29GL-P	S29GL-N
Program Buffer Size	256-word	32-word	16-word
Typical Program Speed with Full Buffer	1.8MB/s	0.133MB/s	0.133MB/s
NVPBs Clear Time	0.5s	NA	NA
Erase Suspend Latency	20µs (typ)/25µs (max)	5µs (typ)/20µs (max)	5µs (typ)/20µs (max)
Program Suspend Latency	20µs (typ)/25µs (max)	5µs (typ)/15µs (max)	5µs (typ)/20µs (max)

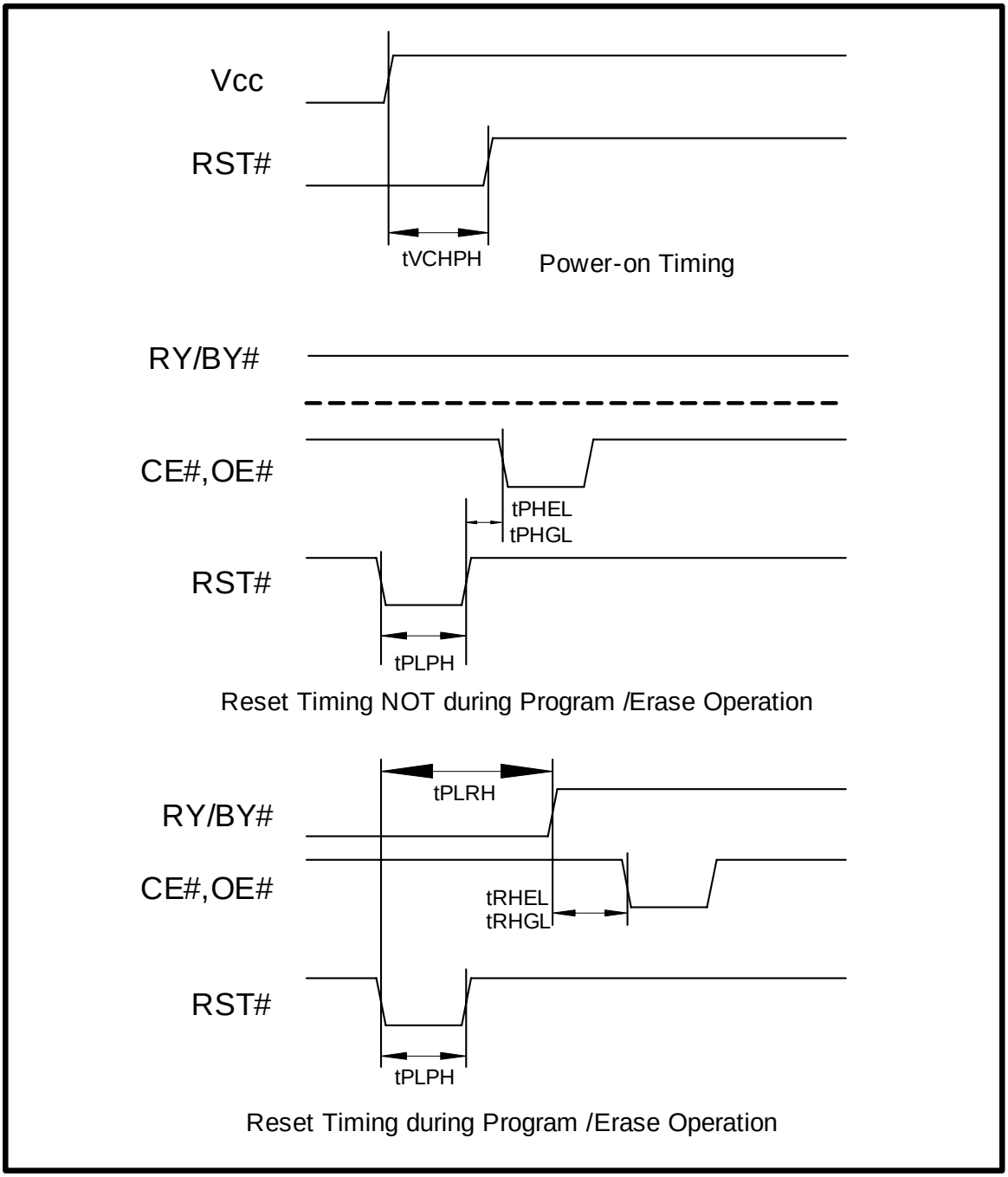
4.2 Power-on and Reset Timings

The M29EW (SBC) device has slightly different power-on and reset timing specifications, compared with the S29GL-P and S29GL-N devices. However, the difference has been proven to be of minimal impact on the customer, since many common processors support those parameters.

Table 7. Power-on and Reset Timing Comparison

Symbol	Alt.	Parameter	Min/Max	M29EW (SBC)	S29GL-P	S29GL-N
t_{VCHPH}	t_{VCS}	V_{CC} power valid to Reset# high (Min)	Min	60µs	35µs	50µs
t_{PLRH}	t_{READY}	Reset# low to read mode, during Program or Erase	Max	25µs	-	20µs
			Min	-	35µs	-
t_{PLPH}	t_{RP}	Reset# pulse width	Min	100ns	35µs	500ns
t_{PHEL} t_{PHGL}	t_{RH}	Reset# high to Chip Enable low, Output Enable low	Min	50ns	200ns	50ns
t_{RHEL} t_{RHGL}	t_{RB}	RY/BY# high to Chip Enable low, Output Enable low	Min	0ns	0ns	0ns

Figure 6. Power-on and Reset Timing Sequences



5 Software Considerations

The command set of M29EW (SBC) flash is fully compatible with that of S29GL-P/S29GL-N devices. Therefore, no command change in software is required to accommodate M29EW (SBC) flash.

5.1 Manufacturer ID and Other Autoselect Information

Numonyx and Spansion have different Manufacturer IDs, therefore, a slight modification in the software is required during migration.

Table 8 outlines the differences of Autoselect information.

Table 8. Autoselect Information Comparison (16-bit mode)

Description			Address	M29EW (SBC) (Hex)		S29 GL-P (Hex)	S29GL-N (Hex)	
Manufacturer ID			(Base)+00h	0089h		0001h	0001h	
Device ID Cycle 1			(Base)+01h	227Eh		227Eh	227Eh	
Device ID cycle 2			(Base)+0Eh	128-Mbit	2221h	2221h (128-Mbit only)	128-Mbit	2221h
				64-Mbit, boot	2210h		64-Mbit, boot	2210h
				64-Mbit, uniform	220Ch		64-Mbit, uniform	220Ch
				32-Mbit, boot	221Ah		32-Mbit, boot	221Ah
				32-Mbit, uniform	221Dh		32-Mbit, uniform	221Dh
Device ID cycle 3			(Base)+0Fh	128- and 64-Mbit uniform, 64- and 32-Mbit top	2201h	2201h (128-Mbit only)	128- and 64-Mbit uniform, 64- and 32-Mbit top	2201h
				64- and 32-Mbit bottom, 32-Mbit uniform	2200h		64- and 32-Mbit bottom, 32-Mbit uniform	2200h
Protection Register Indicator	V_{PP}/WP # Locks Highest Block (s)(1)	Factory Locked	(Base)+03h	128-Mbit	0099h	0099h	128-Mbit	0098h
				64- and 32-Mbit	009Ah	-	64- and 32-Mbit	009Ah
		Factory Unlocked		128-Mbit	0019h	0019h	128-Mbit	0018h
				64- and 32-Mbit	001Ah	-	64- and 32-Mbit	001Ah
	V_{PP}/WP # Locks Lowest Block (s)(2)	Factory Locked		128-Mbit	0089h	0089h	128-Mbit	0088h
				64- and 32-Mbit	008Ah	-	64- and 32-Mbit	008Ah
		Factory Unlocked		128-Mbit	0009h	0009h	128Mbit	0008h
				64- and 32-Mbit	000Ah	-	64- and 32-Mbit	000Ah

Table 8. Autoselect Information Comparison (16-bit mode)

Description		Address	M29EW (SBC) (Hex)	S29 GL-P (Hex)	S29GL-N (Hex)
Block Protection	Unprotected	(Base)+02h	0000h	0000h	0000h
	Protected		0001h	0001h	0001h

1. When VPP/WP# is V_{IL}, the highest (M29EWH) or top two (M29EWT) blocks are protected.
2. When VPP/WP# is V_{IL}, the lowest (M29EWL) or bottom two (M29EWB) blocks are protected.

5.2 Autoselect Entry Comparison

The M29EW device does not support 12V V_{HH} on A9 pin to enter Autoselect mode, while normal command sequence (AAh/55h/90h) can enter Autoselect mode. Applying 12V on A9 pin may damage the device. S29GL devices support both methods to enter Autoselect mode.

Table 9. Autoselect Entry Comparison

Autoselect Entry Mode	M29EW (SBC)	S29GL-P	S29GL-N
12V on A9 pin	No	Yes	Yes
Entry Command (90h)	Yes	Yes	Yes

5.3 CFI Difference

CFI differences exist between M29EW (SBC) and S29GL-P/S29GL-N due to device features and performance characteristics.

The *Table 10* outlines the relevant information.

Table 10. CFI Difference Comparison

Address (HEX)	Description	M29EW (SBC) (HEX)	S29GL-P (HEX)	S29GL-N (HEX)
1D	V_{PPH} [programming] supply minimum Program / Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	00B5	0000	0000
1E	V_{PPH} [programming] supply maximum Program / Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	00C5	0000	0000
1F	Typical time-out for single byte/word program = 2^n µs	0004	0006	0007
20	Typical time-out for maximum size buffer program = 2^n µs	0009	0006	0007
21	Typical time-out for individual block erase = 2^n ms	0009	0009	000A

Table 10. CFI Difference Comparison

Address (HEX)	Description	M29EW (SBC) (HEX)		S29GL-P (HEX)	S29GL-N (HEX)
22	Typical time-out for full Chip Erase = 2^n ms	128-Mbit	0011	0013	0000
		64-Mbit	0010		
		32-Mbit	0009		
23	Maximum time-out for byte/word program = 2^n times typical time-out	0004		0003	0003
24	Maximum time-out for buffer program = 2^n times typical time-out	0002		0005	0005
25	Maximum time-out per individual block erase = 2^n times typical time-out	0003		0003	0004
26	Maximum time-out for Chip Erase = 2^n times typical time-out	0002		0002	0000
2A 2B	Maximum number of byte in multiple-byte write = 2^n	0008 0000		0006 0000	0005 0000
45	Address Sensitive Unlock (Bits 1 to 0) 0 = Required, 1 = Not Required Silicon revision number (Bits 7 to 2)	0018		0014	0010

5.4 Password Access

Password Access is a security enhancement offered on the M29EW (SBC) device. This feature protects information stored in the main-array blocks by preventing content alteration or reads until a valid 64-bit password is received. Password Access may be combined with Non-Volatile and/or Volatile Protection to create a multi-tiered solution.

S29GL-P and S29GL-N series devices don’t support this feature.

Please contact your Numonyx sales representatives for further details concerning Password Access feature.

5.5 Power-Loss Recovery

It is recommended that the user enable robust power-loss recovery in software system, especially during the flash write operations. Please refer to the Application Note 309046 for detail information.

Appendix A Additional Information

Order Number	Document / Tool
208031	Numonyx® Axcell™ M29EW (SBC) 128-Mbit, 64-Mbit, 32-Mbit (x8 or x16, page) 3V Supply Flash Memory Datasheet
S29GL-P_00	SPANSION® MirrorBit® S29GL-P 1-Gbit, 512-Mbit, 256-Mbit, 128-Mbit 3.0 Volt-only Page Mode Flash Memory Datasheet
S29GL-N_00	SPANSION® MirrorBit® S29GL-N 512-Mbit, 256-Mbit, 128-Mbit 3.0 Volt-only Page Mode Flash Memory Datasheet
S29GL-N_01	SPANSION® MirrorBit® S29GL-N 64-Mbit, 32-Mbit 3.0 Volt-only Page Mode Flash Memory Datasheet
309046	Application Note: Power-Loss Recovery for Nor Flash Memory

Notes:
1. Contact your local Numonyx or distribution sales office to request Numonyx documentation.
2. Visit the Numonyx World Wide Web home page at http://www.Numonyx.com for further information, technical documentation and tools.