Technical Note

How to Read, Program, and Manage Small Page NAND OTP Area

Introduction

Micron single level cell NAND flash devices include a one time programmable (OTP) area that can be used to increase the security of a system. This technical note describes how to read and program the user OTP area in single level cell NAND flash memories. This document should be read in conjunction with the single level cell small page NAND data sheets. For confidentiality and licensing reasons, OTP area security is not mentioned in the device data sheets. The information in this technical note applies to the devices listed here.

Table 1: Small Page Device Part Number List

Size	Part Number
128Mb	NAND128W3A2B
	NAND128W3A0B
256Mb	NAND256W3A2B
	NAND256W3A0B
512Mb	NAND512x3A2D
	NAND512x3A2S

Reading Small Page OTP Area

To read the OTP user area, first issue the UNLOCK OTP AREA command sequence (29h, 17h, 04h, and 19h).

Only when the UNLOCK OTP AREA command sequence is completed, issue the PAGE READ command. The PAGE READ command is composed of first, a READ SETUP command (00h), followed by four address input cycles. After the last address input cycle, the device goes into BUSY state, and then, when the device is ready, subsequent READ cycles output the data.

After the OTP area is read, either a RESET (FFh) command or an EXIT OTP AREA command (06h) must be issued.

This UNLOCK OTP AREA command sequence minimizes the risk of accidental or unauthorized UNLOCK operations.

Table 2: Read OTP Area Bus Cycle

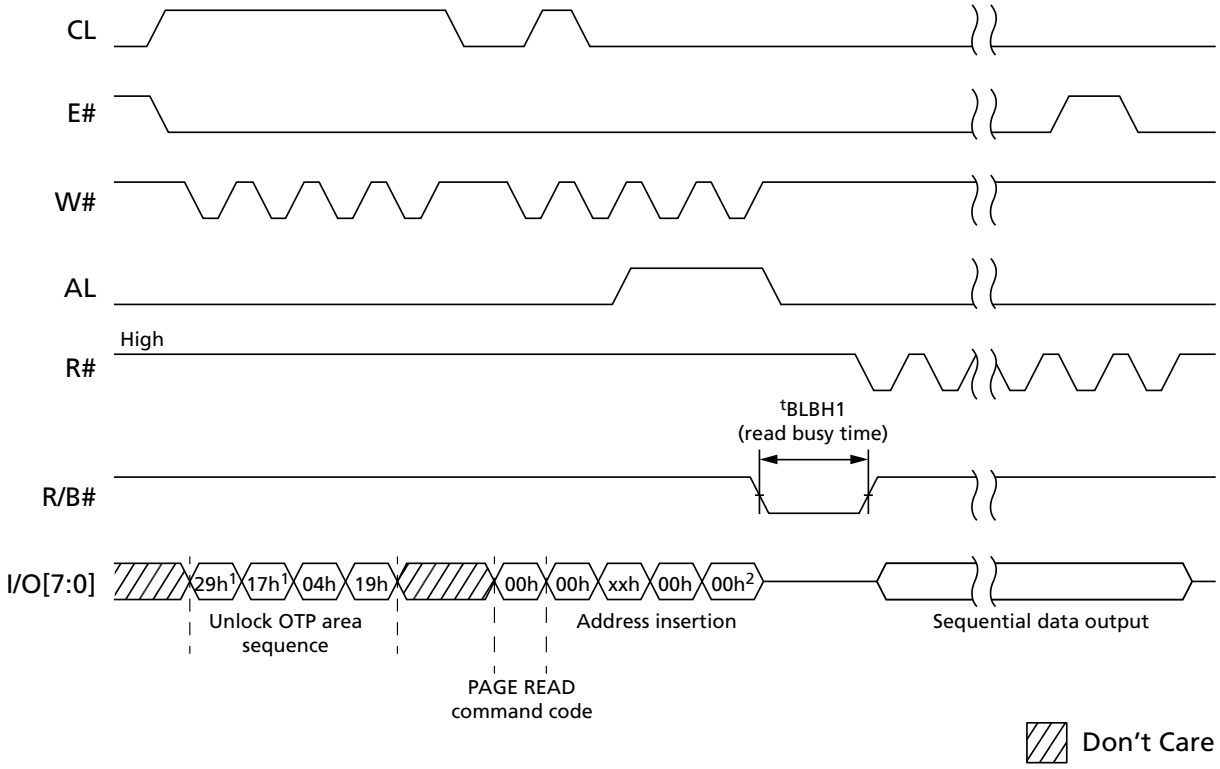
Bus Cycle	Type	Value	Notes
1	Command	29h	1
2	Command	17h	1
3	Command	04h	
4	Command	19h	

Table 2: Read OTP Area Bus Cycle (Continued)

Bus Cycle	Type	Value	Notes
5	Command	00h	
6	Address cycle 1	00h	
7	Address cycle 2	00h to 1Fh	
8	Address cycle 3	00h	
9	Address cycle 4	00h	2
10	RESET or EXIT OTP command	FFh or 06h	

Notes: 1. Required only for NAND128W3A2B and NAND256W3A2B.
2. The fourth address cycle is required only for 512Mb devices.

Figure 1: Read Small Page OTP Area Timing



Notes: 1. Required only for NAND128W3A2B and NAND256W3A2B.
2. The fourth address cycle is required only for 512Mb devices.

Programming Small Page OTP Area

To program the OTP user area, first issue the UNLOCK OTP AREA command sequence (29h, 17h, 04h, and 19h).

Only when the UNLOCK OTP AREA command sequence is completed, issue the PAGE PROGRAM command. The PAGE PROGRAM command is composed of first, a PAGE PROGRAM command (80h), followed by data input of 528 bytes (maximum) to be programmed to the OTP area. This is followed by a PAGE PROGRAM CONFIRM command (10h).

After the OTP area is programmed, either a RESET (FFh) command or an EXIT OTP AREA command (06h) must be issued to exit the OTP area and return the device to the READ mode.

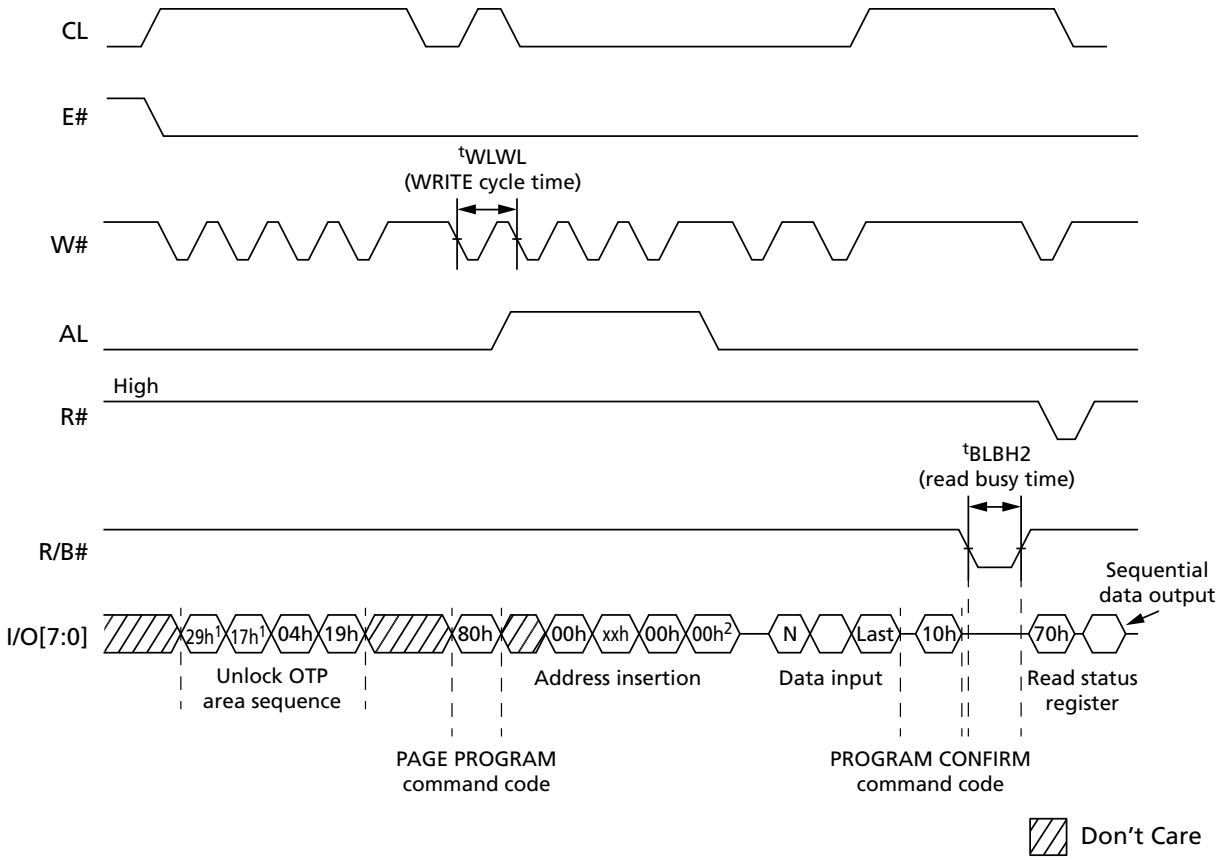
This UNLOCK OTP AREA command sequence minimizes the risk of accidental or unauthorized UNLOCK operations.

Table 3: Program OTP Area Bus Cycle

Bus Cycle	Type	Value	Notes
1	Command	29h	1
2	Command	17h	1
3	Command	04h	
4	Command	19h	
5	Command	80h	
6	Address cycle 1	00h	
7	Address cycle 2	00h to 1Fh	
8	Address cycle 3	00h	
9	Address cycle 4	00h	2
10	PROGRAM CONFIRM command	10h	
11	RESET or EXIT OTP command	FFh or 06h	

Notes:
1. Required only for NAND128W3A2B and NAND256W3A2B.
2. The fourth address cycle is required only for 512Mb devices.

Figure 2: Program Small Page OTP Area Timing



Notes: 1. Required only for NAND128W3A2B and NAND256W3A2B.
2. The fourth address cycle is required only for 512Mb devices.

Managing Small Page OTP Area

The table here shows OTP size and address cycle ranges to manage small page NAND Flash devices. This information is necessary to access and then READ or PROGRAM pages of the OTP user area. Each page is 528 bytes wide.

Table 4: Small Page NAND OTP Sizes and Addresses

Part Number	OTP Size	Column Address	Page Address
NAND128W3A2B	512 bytes (1 page)	0h to 200h (bus x8)	10h
NAND128W3A0B	512 bytes (1 page)	0h to 200h (bus x8)	10h
NAND256W3A2B	512 bytes (1 page)	0h to 200h (bus x8)	10h
NAND256W3A0B	512 bytes (1 page)	0h to 200h (bus x8)	10h
NAND512x3A2D	16 Kbytes (32 pages)	0h to 200h (bus x8) 0h to 100h (bus x16)	00h to 1Fh

Table 4: Small Page NAND OTP Sizes and Addresses (Continued)

Part Number	OTP Size	Column Address	Page Address
NAND512x3A2S	16 Kbytes (32 pages)	0h to 200h (bus x8) 0h to 100h (bus x16)	00h to 1Fh

Revision History

Rev. A – 11/2011

- Initial creation.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992