# Technical Note

## Thinning Considerations for Wafer Products

## Introduction

With increased use of wafer- and die-level products comes added logistic and process considerations. For customers who thin Micron's wafers, this document contains information helpful for determining the optimal wafer-thinning processes to meet their specific requirements.

## Micron's Recommendations

Careful qualification is required to validate alternative customer-generated wafer-thinning processes. In addition to a mechanical or physical evaluation, validation may include the examination of any potentially adverse effects on device performance, such as critical electrical timing specifications, operating currents, charge loss, and refresh. Micron cannot assume responsibility for wafer thinning that may occur after shipment.

## Process Factors for Consideration

Numerous elements of wafer thinning, including product handling issues, must be thoroughly evaluated when determining a suitable thinning process. The information below explains some of the difficulties with wafer thinning to help you identify a technique that meets your specific requirements.

### Backside Surface Damage

Surface damage to the back sides of wafers is an inherent consequence of the coarse grinding step of wafer thinning. To help counter this, fine grinding can be performed to remove the damage caused by the bulk removal of the coarse grind. Typical fine grind removals are in the range of 10µm to 20µm. Actual optimal removals can be determined with surface roughness and/or die strength evaluations.

### Backside Surface Contamination

While stress relief can be advantageous for die strength and handling, some processes, if not carefully developed, can adversely affect the electrical performance of devices. Take care to avoid possible backside surface contamination caused by some stress relief processes to protect the normal operation of Micron's semiconductor products.

### Handling of Thinned Wafers

As a general rule, excessive wafer warping can create handling issues in production and may require integrated tooling for back grinding, mounting wafers on film frames, and detaping procedures.


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## Handling of Thinned Die

The known issues with handling thin die can be further complicated by film frame transfer techniques and package assembly processes. Several aspects of film frame transfer techniques should be evaluated, including film frame tape release properties, the potential for plunge-up pin damage, and the need for a well synchronized pick-and-place process.

## Device Performance

DRAM or NAND performance is dependent on not only how the device is used, but how the device is handled prior to encapsulation; how it is thinned; its finished thickness; and the assembly process temperatures and stresses applied during handling and packaging. Each of these is an important consideration for choosing an appropriate wafer thinning process.

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## Revision History

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- Updated text under “Micron’s Recommendations.”
- Updated text under “Handling of Thinned Die.”
- Updated text under “Device Performance.”
- Updated template.

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- Initial release.



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