Technical Note

LPDDR – Thermal Implications for Die Stacks

Introduction

Mobile applications require memory to meet ever-more-stringent criteria for speed, power consumption, and package footprint. As access speeds increase, mounting the memory closer to the applications processor is key to optimizing signal quality.

Stacking memory either in the same package as the applications processor or in a package that mounts on top of the processor package has been proven to improve signal quality and reduce the overall footprint for the system.

However, application designers must be careful to ensure that all devices are fully functional and do not pose reliability risks when operated in the resulting high-temperature thermal environment.

This technical note presents a case study of a handset simulation in which an LPDRAM is stacked on an application processor (PoP) and the resulting thermal-profile modeling. This note also explains how thermal detection features included in LPDDR and LPDDR2 can be used to monitor the junction temperature of the memory, enabling the application to detect and compensate when the junction temperature exceeds the specified operating temperature.

Background

Memory is packaged in a variety of ways, including:

1. Discrete package, where only one memory device is packaged and then mounted on the application board.
2. Multichip module (MCM), where memory die are mounted on a package substrate and encapsulated with a processor or other discrete components.
3. System-in-package (SiP), where the memory is stacked with an SOC processor.
4. Multichip package (MCP), where multiple memory types are stacked in a single package that is then mounted on the application PCB.
5. Package-on-package (PoP), where multiple memory die are stacked in a discrete package designed to be placed on top of the applications processor package. The PoP could contain one or more types of memory. For example, NAND plus LPDDR, NAND plus LPDDR2, *e*·MMC™ plus LPDDR or LPDDR2, etc.

The Impact of Heat on Memory

Many factors should be considered during an application design. A key design requirement is that the memory operates within the specified temperature range, ensuring that functionality and reliability of the memory are not compromised.

The implications of violating the specified temperature range for any MOS or bipolar semiconductor product are covered in Micron® technical note TN-00-18, "Uprating Semiconductors for High-Temperature Applications," available at the Micron Web site, http:\\www.micron.com. TN-00-18 focuses specifically on temperature uprating and the significant failure mechanisms associated with operating semiconductors outside their specified temperature ranges.

Additional information about junction temperatures is available in Micron technical note TN-00-08, "Thermal Applications."

Each memory manufacturer assumes that memory will be operated within the specified temperature range. Failure to do so compromises the device functionality and can lead to reliability failures. As discussed in TN-00-08, "Thermal Applications Junction Temperature," it is sometimes difficult to determine the actual temperature of the device. Relying on case- or board-temperature measurements can lead to junction temperatures that exceed the device specifications.

Each application presents a unique interaction of thermal characteristics. Component proximity, air flow, and PC board layout can pose a problem for discrete memory, SiP applications, and MCPs, as well as PoP packages.

The following case study presents an illustration of these interactions.

Case Study: Cell Phone Thermal Simulation Using PoPs

The goal of this simulation is to determine the thermal impact on Micron memory when the memory is stacked on an application processor in PoP form.

Simulation Assumptions:

The following assumptions are made for this cell phone thermal simulation with PoPs:

- Phone exterior dimensions: 110mm x 55mm x 9mm
- Simulation performed using a conduction model only
- All interior space filled with (0.5W/mK) material to represent all the plastic that fills the interior
- 8-layer PCB, 0.68mm thick
- 4 signal layers
- 4 power/ground layers
- Natural convection on the entire exterior of the phone (6W/m²K)
- Ambient temperature = 0°C; required ambient operating temperature added to the results

Figure 1: Cell Phone Thermal Simulation Model Layout

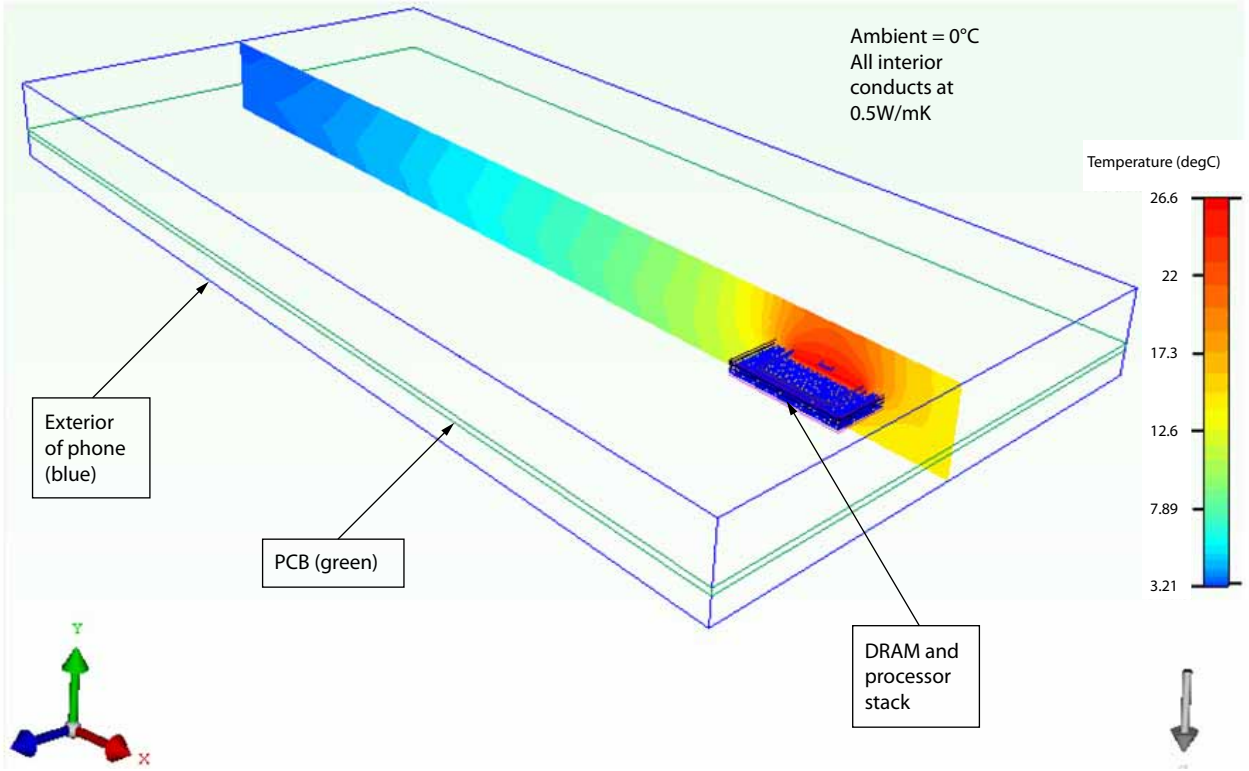


Figure 2: Cell Phone Thermal Simulation – Side View

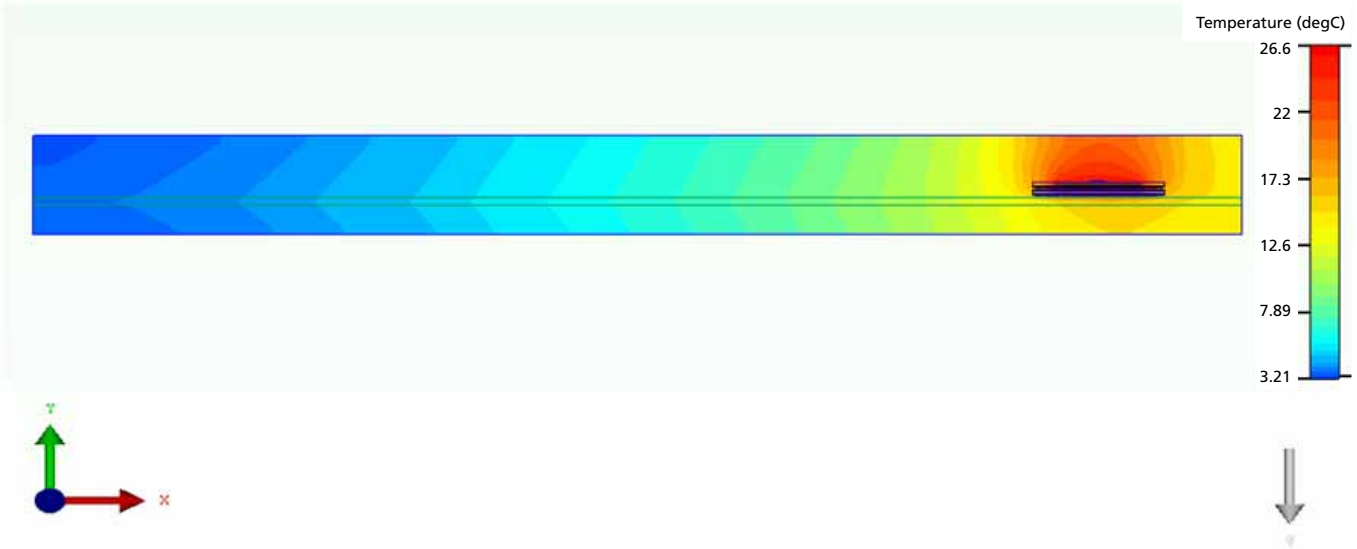
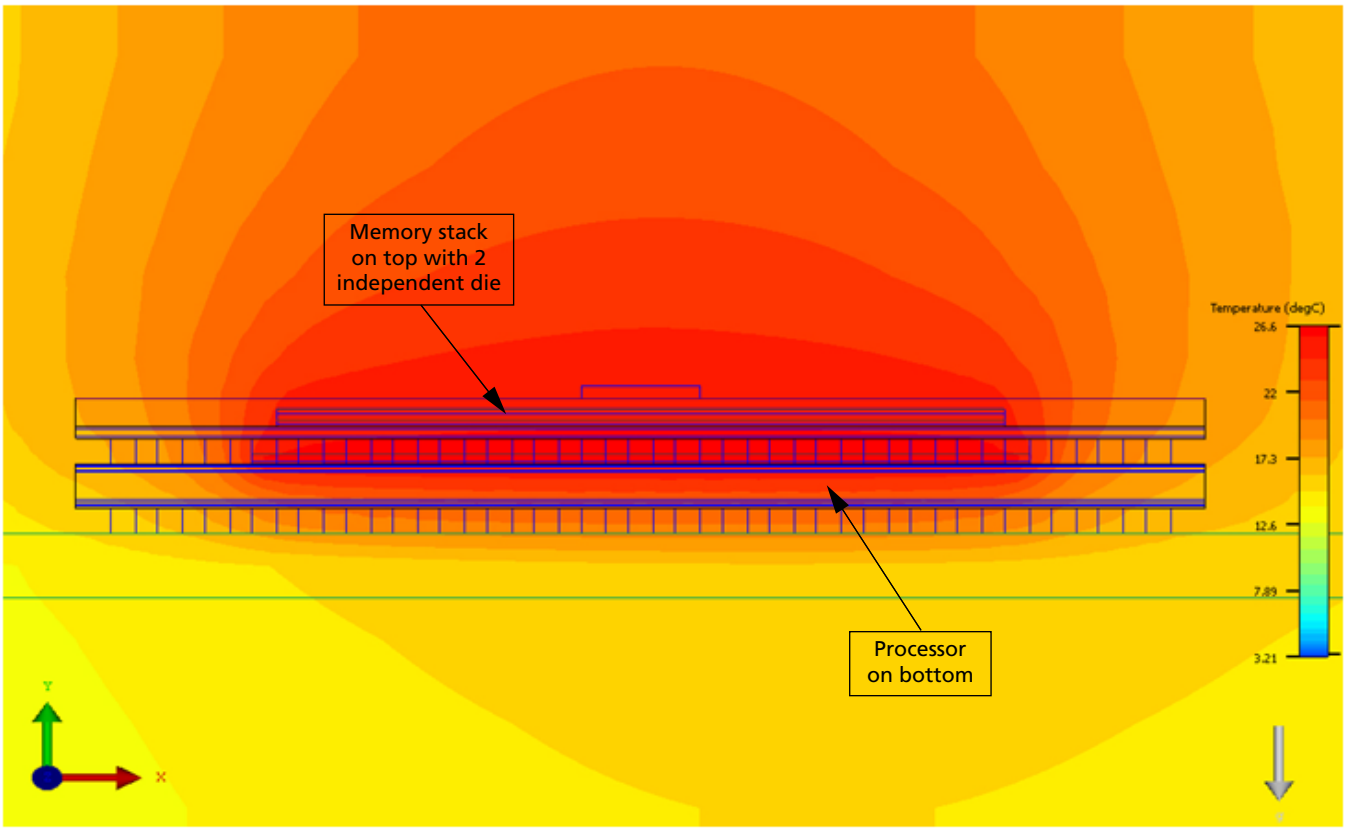


Figure 3: Cell Phone Thermal Simulation PoP Stack



The simulation shows that the processor and memory stack will operate at very close to the same temperatures.

Figure 4: Cell Phone Thermal Simulation Results

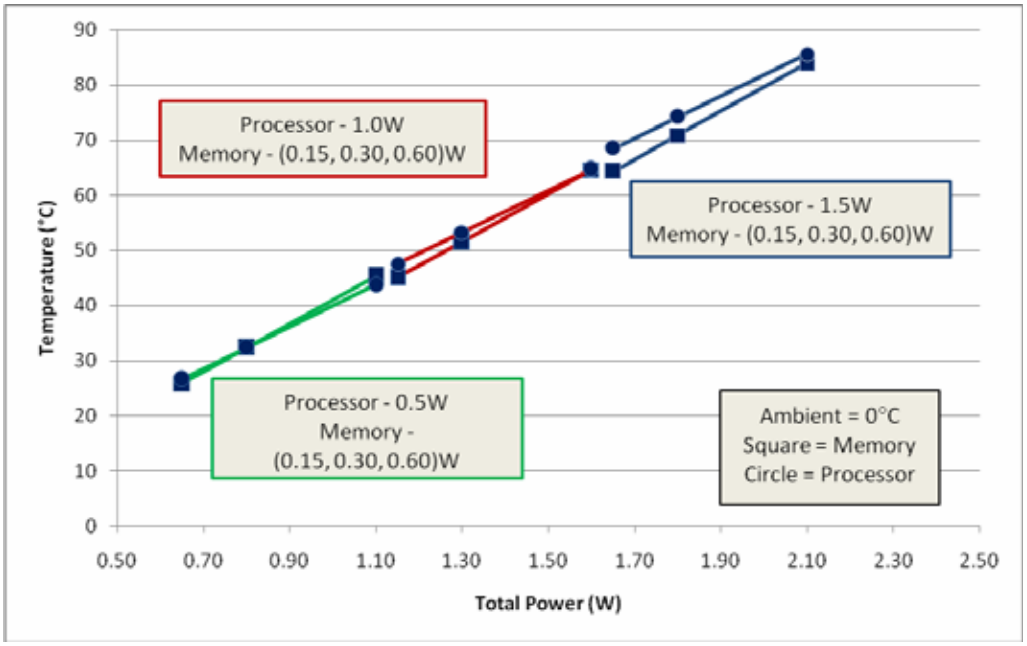


Figure 4 is a graphical illustration of power-consumption estimates for processor power (0.5W, 1.0W, and 1.5W) and memory power (0.15W, 0.30W, and 0.60W) cross-temperature.

- Memory average operating power = 0.15W is typical of a single LPDRAM low-usage case running continuous READ/WRITE/REFRESH operations.
- Memory average operating power = 0.30W is typical of a dual LPDRAM moderate-usage case running continuous READ/WRITE/REFRESH operations or a single LPDRAM high-usage case.
- Memory average operating power = 0.60W is typical of a multiple-channel LPDRAM high-usage case, running continuous READ/WRITE/REFRESH operations.

Simulation Conclusions

- The temperature of the processor and memory are very close for all scenarios; i.e., there is not a discernible gradient in temperature between the processor device and the memory PoP device. The PoP stack (the memory and the processor packages) can be modeled as a single die-stack using the power associated with all the die in the stack.
- Depending on the application ambient temperature, the processor power plus the memory power can cause the memory device to run at temperatures that exceed the memory operating-temperature maximum rating.
- Short time periods of high processor power might be acceptable, but a transient analysis would be required.

As demonstrated in the case study, the processor power plus the memory power can create temperatures that exceed the operating-temperature maximum rating of the memory devices. In order to maintain a reliable operational environment for the stack, it is important to monitor the operating temperature of the devices in the PoP stack and employ thermal-management techniques to decrease the stack temperature. At the very least, the refresh frequency of the memory must be increased to compensate for the temperature increase.

If the temperature of the stack is allowed to exceed the operating-temperature range for the memory, functionality and reliability of the memory are compromised.

LPDDR and LPDDR2 designs incorporate thermal-detection capabilities that can be used to determine the actual junction temperature of the memory devices.

LPDDR Thermal Features

Three low-power features can be used to monitor the device temperature or, as in the case of TCSR, to compensate for temperature changes.

1. Temperature-compensated self refresh (TCSR): By responding to an on-chip temperature sensor, the refresh rate automatically adjusts for changes in temperature. As temperature increases, the refresh oscillator frequency increases during self refresh. TCSR provides sufficient refresh only during self refresh for the operating temperature range of the device. If the junction temperature exceeds this range, self refresh will not be sufficient to maintaining data integrity. TCSR does not affect operation when the device is not in self refresh mode.
2. STATUS READ REGISTER (SRR): This register enables the user to read from the SRR temperature-dependent refresh multiplier information from SRR bits[10:8]. This register provides the correct refresh multiplier required for the appropriate refresh rate, based on the on-chip temperature sensor. The required refresh interval = ^{t}REFI x multiplier. Micron supports multipliers 2x, 1x band 0.25x. While providing a method to identify the required refresh interval, the application needs to read this register and adjust the refresh frequency as appropriate.
3. Temperature-output sensor signal (TQ): This signal is a LVCMOS output that transitions to a logic-HIGH level when the device temperature is greater than, or equal to, 85°C. For temperatures less than 85°C, the TQ signal outputs a logic_LOW level. The TQ signal is not valid during initialization and becomes valid ^{t}TQ following the first MRS command. When TQ is logic-HIGH, ^{t}REF is specified to be 16ms. Additionally, when TQ is at a logic-HIGH level, AC parameters are derated by 20%, and DC parameters are longer guaranteed. The TQ pin is only a READ out and does not actively change the device operation. The system will need to monitor this pin and respond accordingly when TQ toggles HIGH or LOW.

LPDDR2 Thermal Features

Micron mobile low-power DDR2 SDRAM is designed to allow the temperature-sensor status to be read from mode register 4 (MR4). This sensor can be used to determine an appropriate refresh rate and determine whether AC timing derating is required when operating in the extended temperature range (ET). The sensor can also be used to monitor the operating temperature.

MR4 bit 7 (OP7) indicates whether the temperature-sensor output bits[2:0] have changed since the last time MR4 was read. MR4 bit 7 is set to 0 on power-up and after each read of MR4. MR4 bit 7 is set to 1 if OP[2:0] has changed since last MR4 read.

MR4 bits[2:0] indicate the refresh rate required for a given operating temperature range and whether the device temperature has exceeded the low-temperature operating limit.

Table 1: Refresh Rate Required, Indicated by MR4[2:0]

MR4[2:0] Value	Indication
000b	The low-temperature operating limit is exceeded
001b	4 x ^{t}REFI, 4 x ^{t}REFIpb, and 4 x ^{t}REFW are required
010b	2 x ^{t}REFI, 2 x ^{t}REFIpb, and 2 x ^{t}REFW are required
011b	1 x ^{t}REFI, 1 x ^{t}REFIpb, and 1 x ^{t}REFW are required
100b	Reserved
101b	0.25 x ^{t}REFI, 0.25 x ^{t}REFIpb, and 0.25 x ^{t}REFW is required; derating of AC timing is not required
110b	0.25 x ^{t}REFI, 0.25 x ^{t}REFIpb and 0.25 x ^{t}REFW is required; derating of AC timing is required
111b	The device operating temperature is higher than the specified limit

Notes:
1. A MODE REGISTER READ from MR4 resets OP7 to 0.
2. OP7 is reset to 0 at power-up.
3. If OP2=1, the device temperature is greater than 85°C.
4. OP7 is set to 1 if OP[2:0] has changed at any time since the last MR4 read.
5. The device might not operate properly when OP[2:0] = 000b or 111b.
6. For specified operating-temperature range and maximum operating temperature, refer to the data sheet.
7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: ^{t}RCD, ^{t}RC, ^{t}RAS, ^{t}RP, and ^{t}RRD. The ^{t}DQSCK parameter must be derated as specified in the data sheet. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in the “Temperature Sensor” section of the data sheet.

LPDDR2 Temperature Compensation

Thermal monitoring of LPDDR2 memory requires that the MR4 register be checked at the appropriate interval to allow detection of temperature changes within the time needed for the application to respond. If the register is not checked as frequently as needed, temperatures that exceed the operating temperature range will be possible. Reading the MR4 register more frequently than needed may restrict the time that the memory is available for access and may impact system performance. The frequency that the MR4 is read is referred to as the ReadInterval.

Application characterization is needed to determine the system-dependent parameters in order to calculate the appropriate ReadInterval.

System characterization is required to determine:

- The device temperature offset, the device case temperature offset from the MR4 junction temperature reading.
- The temperature gradient of the system in °C/s; the maximum temperature gradient that the memory will see at the operating temperature of interest.
- The time between reading MR4 and actions taken in response to this reading. (For example, an MR4 READ might indicate MR4[2:0] = 001b, requiring 4 x ^{t}REFI, 4 x ^{t}REFIpb, and 4 x ^{t}REFW.) The delay from the MR4 READ to the system response, such as changing the refresh rate, would be the system-response delay.

After the application has been characterized to determine the system-dependent parameters, the ReadInterval can be calculated.

Table 2: Temperature-Sensor Definitions and Operating Considerations

Parameter	Description	Symbol	Min/Max	Value	Units
System temperature gradient	Maximum temperature gradient experienced by the memory device at the temperature of interest	TempGradient	MAX	System-dependent	°C/s
Register READ interval	Time period between Register READs from the system	ReadInterval	MAX	System-dependent	ms
Temperature sensor interval	Maximum delay between internal updates of Register	^{t}TSI	MAX	32	ms
System response delay	Maximum response time from a Register READ to the system response	SysRespDelay	MAX	System-dependent	ms
Device temperature margin	Margin above maximum temperature to support controller response	TempMargin	MAX	2	°C

Calculating the ReadInterval

Each application is different and requires a ReadInterval unique to the application. The ReadInterval can be derived from the following equations.

Equation 1: TempGradient × (ReadInterval + ^{t}TSI + SysRespDelay) ≤ 2°C

For example, assuming:

- TempGradient = 5°C/s
- System response delay of 50_{ms}
- Device temperature margin of 2°C

Equation 2: ReadInterval = (2°c/TempGradient°C/s) - ^{t}TSIms - SysRespDelayms

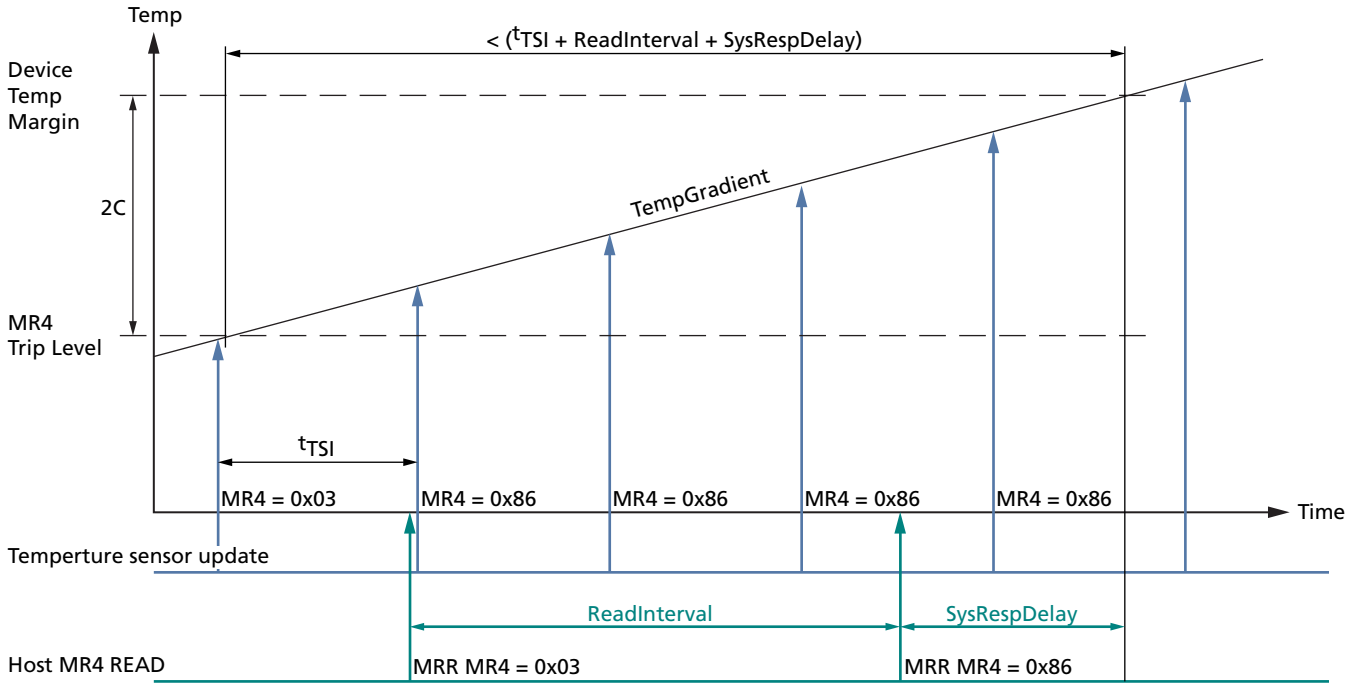
ReadInterval = (2°c/5°c/s) - 32ms- 50ms

ReadInterval = 0.4s - 32ms - 50ms

ReadInterval = 318ms

(See Figure 5 for a graphical representation of the ReadInterval calculation.)

Figure 5: Temperature-Sensor Timing



Summary

Operating LPDRAM memory within the specified temperature range is important in maintaining device functionality and reducing reliability risks.

Board layout, package type, and placement can have a thermal impact on other components in an application.

The PoP-based thermal study presented in this technical note indicates that components in close proximity look like a single device from a thermal viewpoint. The study illustrates that peak processor power-draw can result in temperatures that exceed the specified operating range.

Application designers should be aware of LPDDR and LPDDR2 temperature-sensing features. The presented method for calculating the ReadInterval for LPDDR2 would be valid for LPDDR designs, as well. Monitoring the memory junction temperature at the appropriate interval and responding by changing the refresh rate, derating timing specifications, or other appropriate application changes can help assure the functionality and reliability of the memory, regardless of the package choice.

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Revision History

Rev. A 7/10

- Initial release