

# Technical Note

## Power Integrity Simulation with IBIS 5.0 Models

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### Introduction

The I/O Buffer Information Specification (IBIS) is a modeling format used for signal integrity (SI) simulation. Recent support has extended IBIS into power integrity (PI) simulation, specifically enabling simultaneous switching output (SSO) noise simulation. A significant advantage of IBIS-based simulation over SPICE-based transistor-level simulation for SSO is considerable simulation time improvement without substantial loss of accuracy.

This document describes the new features in IBIS 5.0 enabling PI simulation. It also provides an overview of some of the modeling accuracy challenges and compares SSO simulation results using various electronic design automation (EDA) software tools.

## Overview

Wide parallel memory busses can present significant design challenges when it comes to designing a robust power delivery network (PDN). One critical focus of PDN design is delivery of power to the memory chip output drivers. The on-chip data (DQ) drivers can require significant amounts of current delivered through sometimes highly inductive package connections. Low power dual data rate (LPDDR) devices can have up to 32 DQ drivers on one die switching at the same time. Stacked die packages can increase this number for a single package. These simultaneous switching outputs can cause significant noise issues that translate into timing jitter and SI problems.

Mitigating system SSO issues requires optimizing the PDN design of the printed circuit board (PCB), the package, and on the die. Detailed circuit models are needed for each piece. Historically, these circuit models are combined and simulated in SPICE-based simulators to analyze SSO effects. These simulations are computationally intensive and lead to lengthy simulation times from hours to days.

SPICE-based transistor level models of the on-die drivers are often the most complex part of the system model. This is especially true for the most accurate models that include layout-based RC parasitic circuit elements, typical of Micron's DRAM buffer models. One effective way to reduce simulation time is to use behavioral buffer models. Behavioral models use simpler algorithms than SPICE models, enabling faster simulation with often similar levels of accuracy.

## IBIS 5.0 Power Integrity Features

At its core, an IBIS model uses only a few tables of data to represent the behavioral characteristics of a buffer. Sets of I-V tables represent the  $I_{DS}$  versus  $V_{DS}$  characteristics of the pull-down and pull-up transistors, showing the dynamic impedance of the buffer. The switching behavior of the buffer is shown through sets of V-T tables that capture the rising and falling edge transitions of the buffer driving resistive test loads. The capacitance of the buffer is also quantified. This information provides an accurate model for SI simulation, but it lacks behavioral characteristics necessary for PI simulation.

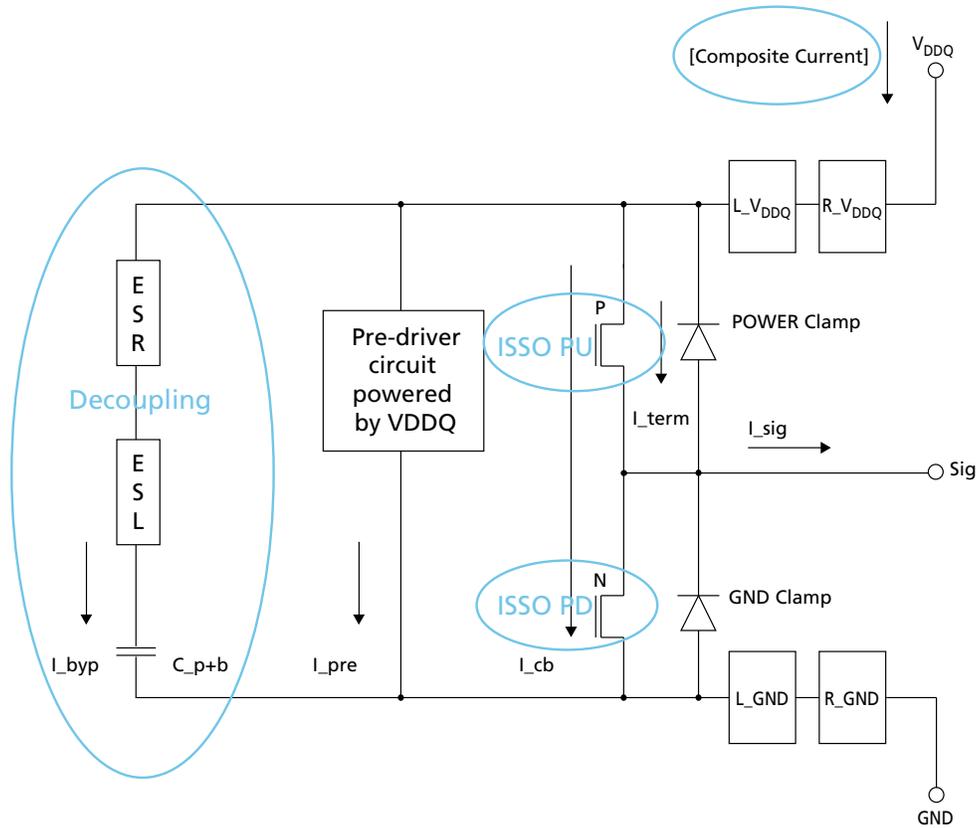
One of the major upgrades in the IBIS version 5.0 specification is the introduction of additional data tables to model buffer power characteristics. Models containing these data are known as power-aware IBIS models. Model data within an IBIS file is contained in sections headed by keywords in brackets. The new keywords in IBIS 5.0 specific to PI include [Composite Current], [ISSO PU], and [ISSO PD].

### [Composite Current] Data

[Composite Current] data are I-T tables that describe the shape of the rising and falling edge current waveforms from the power reference terminal of the buffer.

The I-T tables show the switching current associated with the V-T tables. As shown in Figure 1 (page 3), this switching current includes contributions from the on-die decoupling circuit ( $I_{byp}$ ), crow-bar current ( $I_{cb}$ ), any termination current ( $I_{term}$ ), signal driver current ( $I_{sig}$ ), and pre-driver current ( $I_{pre}$ ). The pre-driver current is the most significant current contribution besides the final driver current seen in DRAM device drivers. Final driver current could be derived accurately by simulating pre-IBIS 5.0 models; however, this significantly underestimates the total driver current without details of the pre-driver contribution.

**Figure 1: IBIS 5.0 Power-Aware Model Additions**



**[ISSO PU] and [ISSO PD] Data**

[ISSO PU] and [ISSO PD] data are tables describing the effective current of the pull-up and pull-down driver transistors as a function of the voltage on the pull-up and pull-down supply reference nodes (analogous to the driver transistor's  $I_{DS}$  versus  $V_{GS}$  characteristics).

The PI problem being modeled is known as gate modulation and is caused by drooping power supply voltages on-die as the die PDN attempts to pull current instantaneously through the inductive package PDN. The voltage droop is proportional to the package inductance ( $L_{PKG}$ ) and the rate of change of the current as in the following equation:

$$V_{\text{droop}} = L_{\text{PKG}} \frac{dI}{dt}$$

The most popular IBIS model simulation algorithms relate the static I-V and dynamic V-T data tables through two time-dependent multipliers  $K_u(t)$  and  $K_d(t)$  to describe the switching behavior of pull-up and pull-down transistors, respectively. [ISSO PU] and [ISSO PD] data tables are used to derive modulation coefficients  $K_{\text{ss0\_pu}}$  and  $K_{\text{ss0\_pd}}$ . These coefficients modulate the  $K_u(t)$  and  $K_d(t)$  variables when a voltage variation on the pull-up and pull-down reference nodes is revealed during power and/or ground bounce and/or SSO simulation events.

## On-Die Power Supply Decoupling and Die Capacitance

In addition to the [Composite Current], [ISSO PU], and [ISSO PD] data tables in the IBIS file, it is necessary to include the characteristics of the on-die power supply decoupling structure. A simplified example of this structure is shown in Figure 1 (page 3).  $C_{p+b}$  represents the bypass and parasitic capacitance, ESR is the equivalent series resistance, and ESL is the equivalent series inductance of the on-die coupling capacitance. On-die decoupling interacts with package inductance to form an LC tank circuit that will resonate at a specific frequency, resulting in ringing of the voltage waveform seen at the die. Due to current limitations in the IBIS specification, a model of the on-die decoupling electrical behavior must be included in SSO simulations external to the IBIS buffer model, connected across the power and ground reference terminals.

A final requirement for IBIS 5.0 power-aware models is to provide a complex model of the die capacitance. Die capacitance in IBIS models is called  $C_{comp}$ .  $C_{comp}$  is generally modeled as a simple capacitor to ground for SI purposes. However, this model is not accurate for PI simulations and must be adjusted to apportion the  $C_{comp}$  between capacitance to the power reference terminal and capacitance to the ground reference terminal. This splits  $C_{comp}$  into  $C_{comp\_pullup}$  and  $C_{comp\_pulldown}$ . Generally, this split is close to 50% of  $C_{comp}$  to each supply reference. These capacitances are not shown specifically in Figure 1 (page 3).

## Modeling Accuracy Challenges

Behavioral models are inherently less accurate than SPICE transistor-level models. Some sources of inaccuracies are model oversimplifications, EDA software algorithms, and behavioral model deficiencies.

### Model Oversimplifications

Oversimplified on-die decoupling modeling choices can lead to undesired consequences. The simplest on-die decoupling model is a single capacitor representing the decoupling capacitance from the output buffer's power reference to its ground reference. This simple model is unlikely to accurately predict the frequency of ringing as described in IBIS 5.0 Power Integrity Features. A more accurate model is an RC model that adds the equivalent series resistance (ESR) to the simple C model. This model better represents the electrical characteristics of on-die decoupling over a slightly wider frequency range. The best model for on-die decoupling is to create a broadband SPICE model that accurately models on-die decoupling over a frequency range from about 0Hz to 10GHz. This model is typically created through an S-parameter extraction from the silicon die SPICE model or from measurements. The S-parameter can then be converted to an equivalent broadband SPICE model that tends to behave better in time-domain circuit simulators than does the S-parameter model.

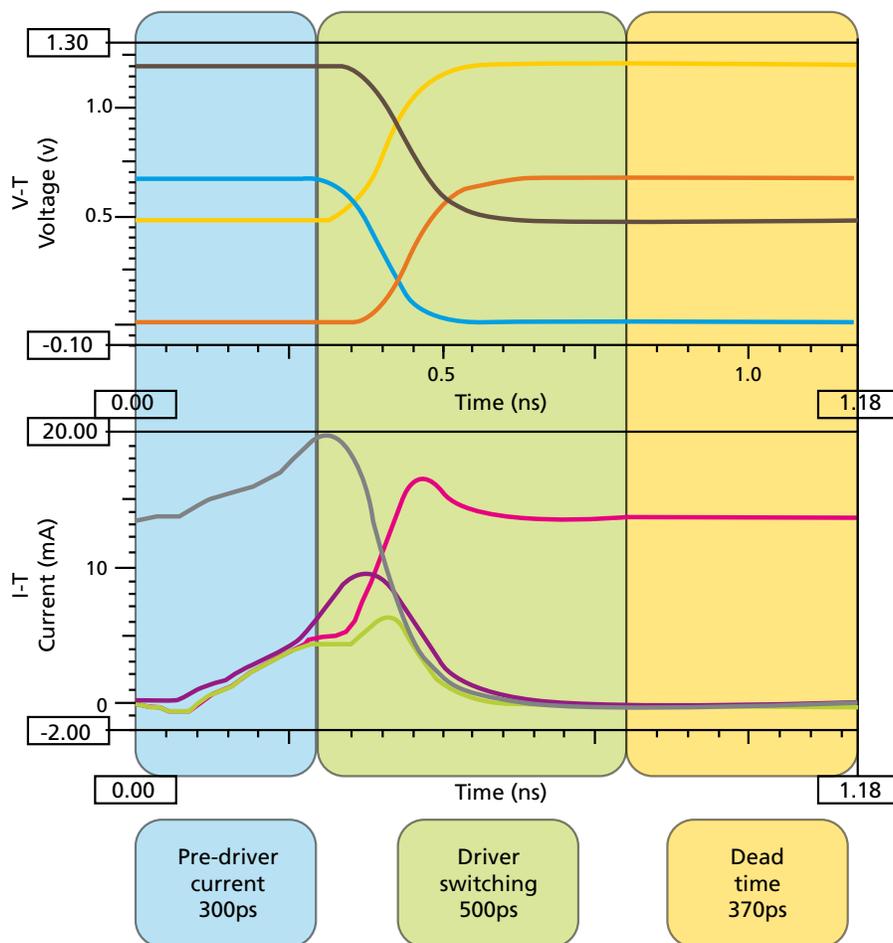
### EDA Software Algorithms

EDA software tools from various vendors differ in their simulation algorithms for IBIS models. Algorithms for the handling of model overclocking lead to some of the largest tool-to-tool simulation differences and inaccuracies. Model overclocking is related to the V-T and I-T data tables in an IBIS model. Figure 2 shows an example of the typical corner V-T and I-T waveforms for a buffer switching into four common test loads. For a given technology, the highest data rate determines the shortest unit interval (UI) or bit time. For example, LPDDR3-1600 has a UI of 625ps, indicating that a buffer should fully

switch a load from a high-to-low or low-to-high level within 625ps, otherwise it is over-clocked. The LPDDR3 IBIS model data shown in Figure 2 indicates that the driver switches within 500ps; however, the total length of the V-T data is 1.18ns, indicating potential overclocking problems. This is typical of IBIS power-aware models, as V-T data must contain data points showing steady-state behavior in order to time-align with I-T data that includes pre-driver switching currents as well as slow and fast corner data within the same data table (a slow corner buffer would finish switching within the dead time section in Figure 2).

EDA software must account for these idiosyncrasies by creating unique triggering events in the simulation algorithms for pre-driver and driver switching currents as well as ignoring data associated with steady-state behavior. Well-designed algorithms allow for time-correlated V-T and I-T data for a given corner case to span 2 UI in time. Buffers that do not reach steady-state conditions within this time period are exhibiting real overclocking behavior and may create further inaccuracies in simulation results compared to the transistor level model.

**Figure 2: V-T and I-T Waveform Data From a LPDDR3 Buffer IBIS Model**



## Pre-Driver Voltage-Delay Relationship

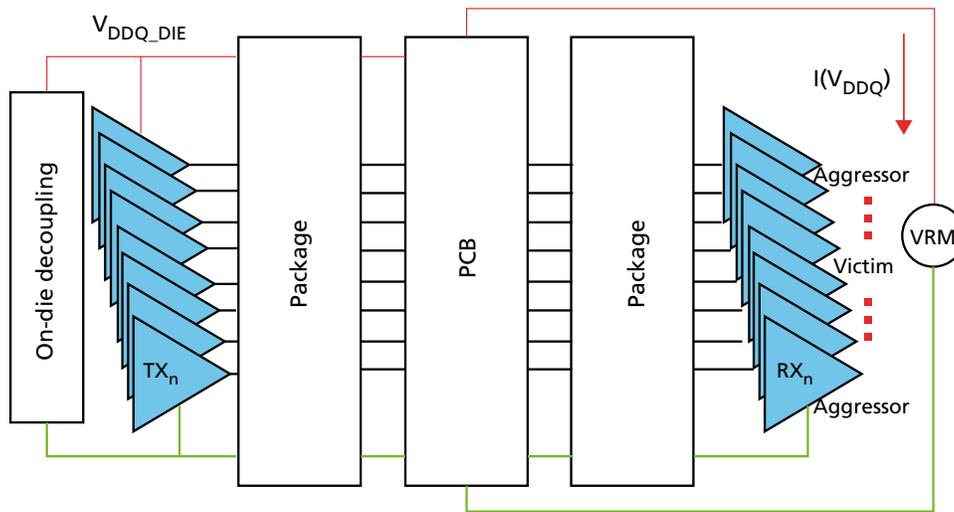
One recognized model deficiency with IBIS power-aware models is that they ignore the effects of voltage changes on pre-driver circuitry. Increasing voltage on-die makes transistors in the pre-driver circuits switch faster; the opposite effect is seen with decreasing voltage. These voltage changes can lead to mismatches in timing between pre-driver pull-up and pull-down signal paths, as well as overall added delay of the driver switching. Modeling the voltage versus timing relationship is difficult but could be added to a future release of the IBIS specification if it proves necessary for better model correlation.

## SSO Simulation

To quantify the loss in accuracy going from a SPICE transistor-level model to a behavioral model, an LPDDR3 SSO test case is examined. The test case compares simulation results using an IBIS 5.0 power-aware model with an equivalent transistor level model of the output driver. The IBIS power-aware model is simulated in two different EDA simulators—Synopsys HSPICE and Keysight Advance Design System (ADS)—both of which include support for the new IBIS 5.0 power-aware features.

The SSO simulation uses the 4Gb LPDDR3 DQ driver and the 178-ball single die package (SDP) fully coupled SPICE package model. The PCB and controller package are modeled with a simplified transmission line model neglecting crosstalk. The schematic of the simulation is shown below.

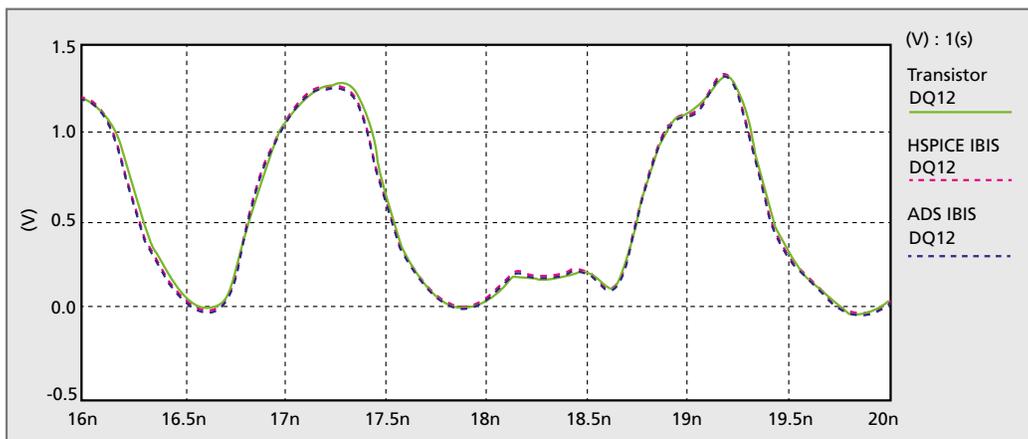
**Figure 3: SSO Simulation Schematic**



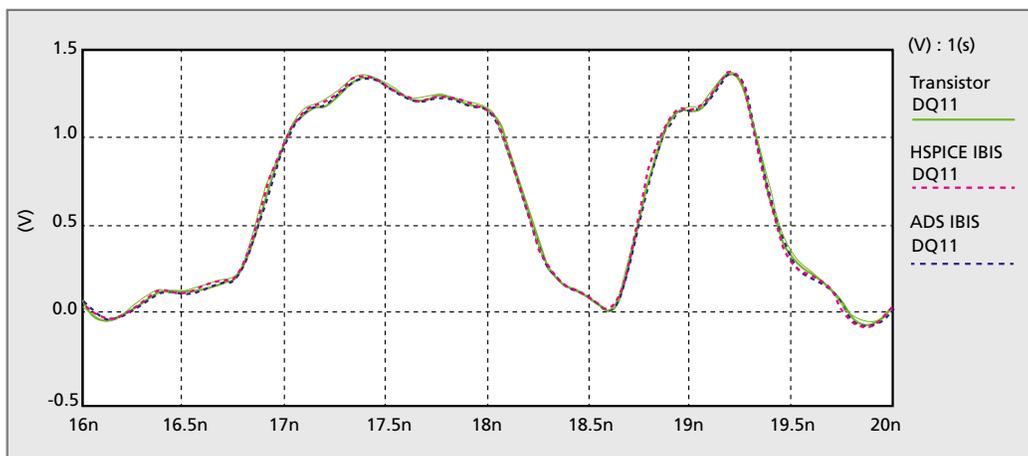
This SSO test case simulates a DRAM READ operation with 32 DQs and 4 DQS pairs switching. A model for the on-die decoupling capacitance is applied across the  $V_{DDQ}$  and  $V_{SSQ}$  at the die pads inside the package model. The on-die decoupling model for the IBIS simulations is a broadband SPICE model as described in Modeling Accuracy Challenges (page 4); the transistor model includes the on-die decoupling characteristics in the netlist on a per-DQ basis.

The simulation uses a pseudo random bit stream (PRBS) pattern for the DQ data. All of the DQ signal lines (referred to as aggressors) use the same PRBS pattern with one exception. One DQ signal uses a different PRBS pattern (referred to as *victim*). This method of aggressor and victim patterns considers all crosstalk and SSO effects. Using both HSPICE and ADS to simulate the IBIS power-aware model provides good correlation in terms of the waveform at the receiver (Rx) of the memory controller. These simulations are run at 1600MT/s with the 34ohm pull-down, 40ohm pull-up drive strength at the typical process, voltage, temperature (PVT) corner. The controller Rx load is modeled with a 240ohm termination to  $V_{DDQ}$  and a 3pF capacitance.

**Figure 4: SSO Simulation—Victim Waveform at Controller Rx**

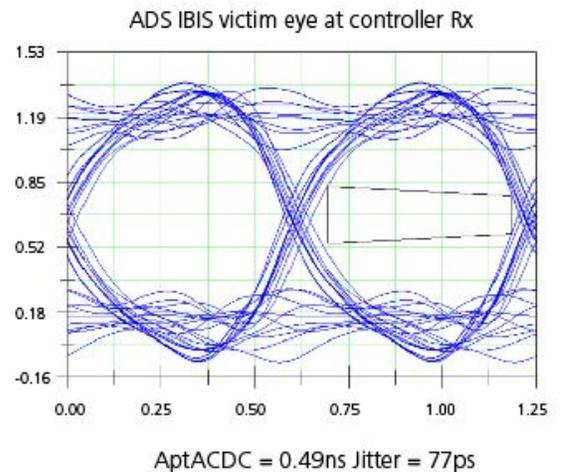
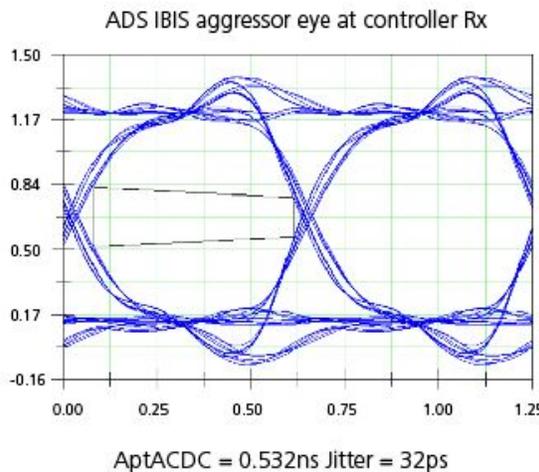
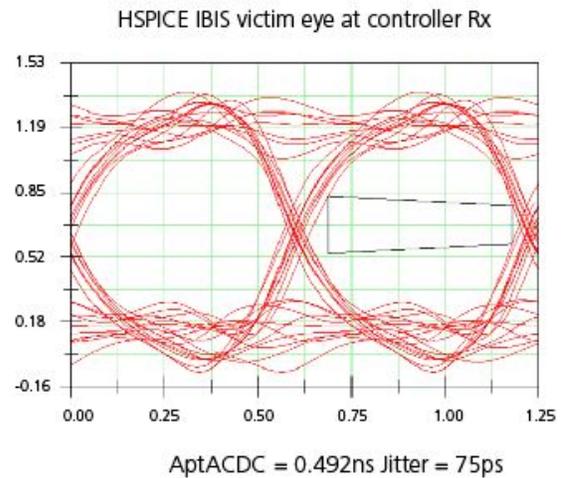
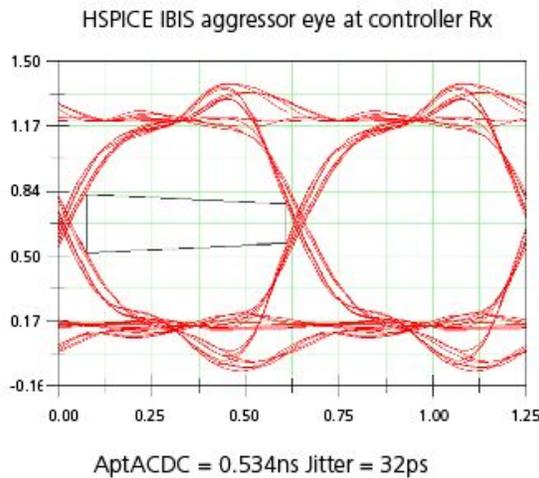
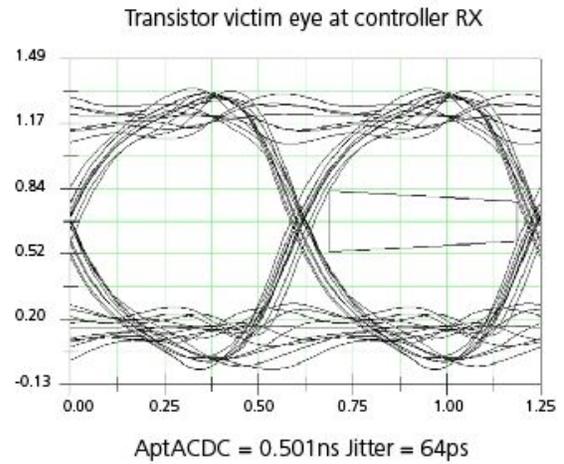
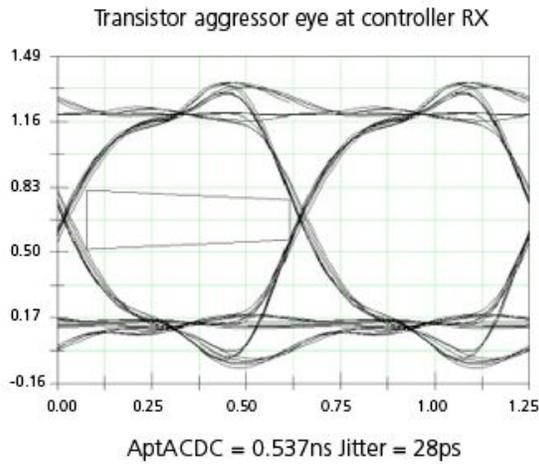


**Figure 5: SSO Simulation—Aggressor Waveform at Controller Rx**



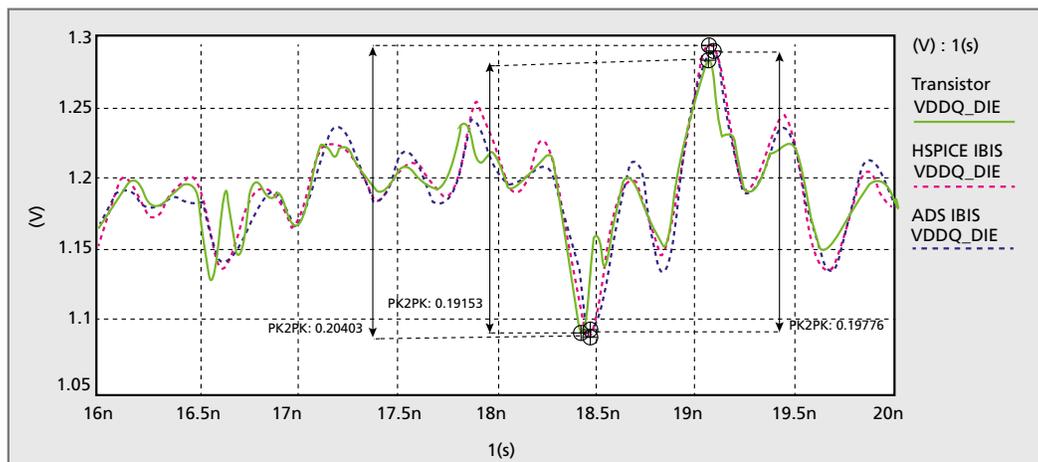
Examining the waveform overlays between the IBIS model and the transistor-level model shows that the correlation is good in terms of waveform shape. This includes the overshoot, undershoot, and ringing characteristics. To measure the correlation of timing characteristics such as jitter and eye aperture, review the eye diagram plots shown in Figure 6. The eye diagrams show the IBIS model gives similar looking eyes to that of the transistor-level model for both the victim and the aggressor signals.

**Figure 6: SSO Simulation Results**

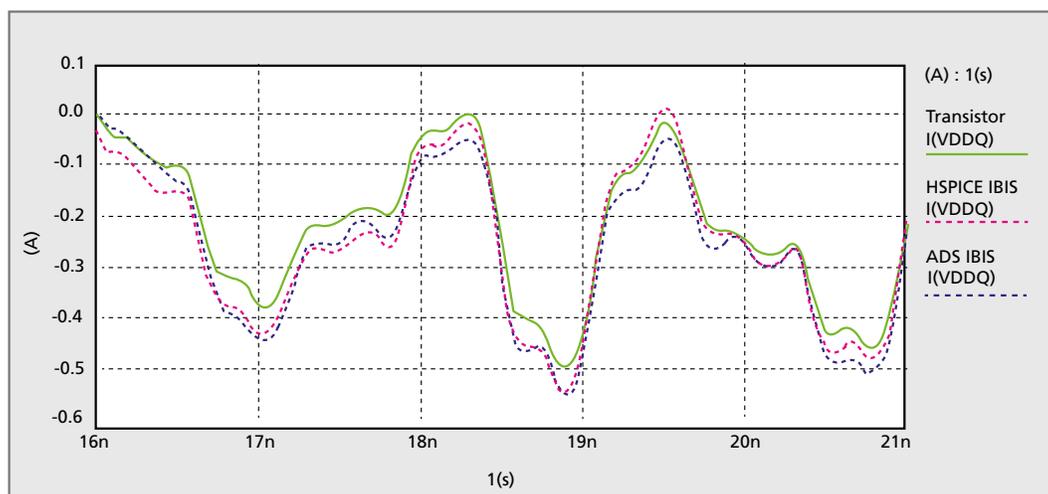


The power supply noise and current profile is also of interest in SSO simulations, since one of the major contributions of noise in the system is the output drivers. Figure 7 compares the  $V_{DDQ}$  noise voltage at the die pad. The peak-to-peak noise is measured for all three cases and correlates well over the time interval plotted. (Note that although this noise can be useful to look at and is valid for comparison purposes,  $V_{DDQ}$  noise above 4 GHz may not be accurate because of the quasi-static nature of the package model used in this analysis.) Figure 8 compares the  $V_{DDQ}$  current profile of the three simulation cases.

**Figure 7: SSO  $V_{DDQ}$  Noise Comparison**



**Figure 8: SSO  $V_{DDQ}$  Current Profile Comparison**



The following table summarizes the key metrics from the simulation plots including the victim jitter, victim eye aperture, peak-to-peak  $V_{DDQ}$  noise at the die, and simulation time.

The simulation time difference between using the IBIS model and the transistor-level model is significant. Although the results show some differences between the three simulations, the correlation is good and would lead to the same conclusions about the system design. Additionally, the improvement in simulation time can be worth the slight loss in accuracy when trying to quickly evaluate a system's performance.

**Table 1: SSO Simulation Metrics**

Sim Case	Victim Eye Aperture (ps)	Victim Jitter (ps)	VDDQ Noise PP (mV)	Simulation Time (hh:mm:ss)
Transistor	501	64	192	04:08:01
HSPICE IBIS	492	75	204	00:09:13
ADS IBIS	490	77	198	00:06:08

## IBIS Package Modeling Improvements

The current IBIS specification as of the publication of this technical note, version 6.1, lacks support and integration of advanced interconnect models for packaging and on-die routing. Advanced models include generic Spice models such as broadband Spice and lossy transmission line models as well as S-parameters. Lossy models that couple signal and power nets are critical for SSO simulations. S-parameters are commonly used in high-speed serializer/de-serializer (SerDes) link design but are increasingly used for SI and PI co-simulation enabled by the Touchstone 2.0 specification. Touchstone 2.0 allows for per-port reference impedances required for signal and power structures to be accurately included within the same model.

The IBIS committee began improving interconnect model definition and transportability between EDA tools by standardizing a subset of the HSPICE language from Synopsys. This document is called the IBIS Interconnect SPICE Subcircuit Specification (IBIS-ISS). IBIS-ISS created a standard, generic Spice language for modeling passive interconnect that could be used by all EDA software tools to output a common modeling format. Support for IBIS-ISS models within the IBIS specification for package and on-die interconnect will be in the next specification release.



## **Revision History**

### **Rev. A – 1/16**

- Initial release.

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