Technical Note

## LVTTL Derating for Slew Rate Violations

Introduction

SDRAM timings are tested and guaranteed under certain slew rates. However, specified timings are no longer valid when these slew rates fall below specification. If slew rates are slower than expected and fall below the minimum specification on the clock, command, and data signals, setup and hold time margins can vary significantly. This technical note describes the proper setup and hold time derating when the slew rate during transition time violates specification.

Setup Time

Setup time for the SDRAM command bus (^{t}CMS) includes signals CS#, RAS#, CAS#, WE#, and DQM. Setup time for the SDRAM data bus ^{t}DS includes signals DQ[3:0] (x4), DQ[7:0] (x8), and DQ[15:0] (x16).

Under ideal conditions, in which both the clock (CLK) and data/command signal transition times meet specification (slew rate $\geq$ 1V/ns), setup time is measured from the midpoint (1.4V) of the rising or falling command/data signal to the midpoint (1.4V) of the rising clock (CLK) edge, as shown in Figure 1. In this example, the shaded areas represent the guaranteed low time (area below 1.4V and above CLK) and time high (area below CLK and above 1.4V). To simplify the depiction of both the command and data buses, the symbol ^{t}SETUP will be used to represent both command setup (^{t}CMS) and data setup (^{t}DS) in this example.

Figure 1:   Clock and Commands/Data Transition Times Meet Specification

Clock and commands/data transition times meet specification
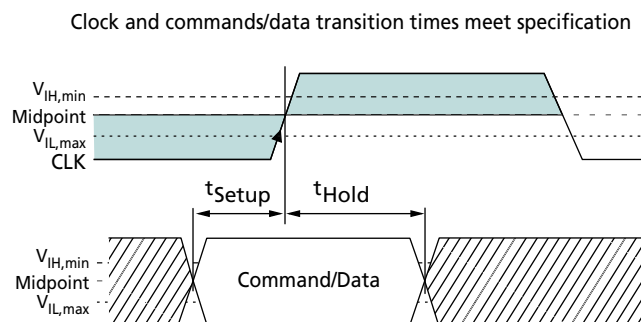
Hold Time

The hold time for the SDRAM command bus (^{t}CH) includes signals CS#, RAS#, CAS#, WE#, and DQM. Hold time for the SDRAM data bus (^{t}DH) includes signals DQ[3:0] (x4), DQ[7:0] (x8), and DQ[15:0] (x16).

If clock (CLK), data, and command signal transition times meet specification (slew rate ≥ 1V/ns), ^{t}HOLD is measured from the midpoint (1.4V) of the rising clock (CLK) edge to the midpoint (1.4V) of the rising or falling command/data signal, as shown in Figure 1 on page 1. To simplify the depiction of both the command and data buses in this example, the symbol ^{t}HOLD will be used to represent both command hold (^{t}CMH) and data hold (^{t}DH).

CLK Violates Slew Rate

The first example occurs when the clock (CLK) transition time falls below specification (slew rate < 1V/ns), but both command and data transition times meet specification, as seen in Figure 2.

For setup, since the rise time of CLK is slower than expected, ^{t}SETUP must be calculated from the midpoint (1.4V) of rising or falling command/data signal to the $V_{IL,max}$ (0.8V) of the rising CLK signal . It is important to note that $V_{IL,max}$ (0.8V) is used to calculate ^{t}SETUP, not $V_{IH,min}$ (2.0V).

Although $V_{IH,min}$ is the guaranteed latch point for a high state, it is possible for DRAM to latch anytime after $V_{IL,max}$ (0.8V). To guard against the possibility that the DRAM has not identified a CLK high transition, $V_{IL,max}$ (0.8V) must be used to calculate ^{t}SETUP. In Figure 2, the shaded region between $V_{IL,max}$ and CLK identifies the only guaranteed low area. This situation requires that the memory controller compensate by setting up command and data values earlier in order to maintain a minimum ^{t}SETUP condition.

For hold, ^{t}HOLD must be calculated from the $V_{IH,min}$ (2.0V) of the rising CLK signal to the midpoint (1.4V) of rising or falling command/data signal .

Note the shaded area between CLK and $V_{IH,min}$ in Figure 2, which shows the only guaranteed high time, which is why $V_{IH,min}$ (2.0V) is used to calculate ^{t}HOLD.

This situation causes the command/data signal to be pushed out longer in order to maintain the minimum ^{t}HOLD specification.

Figure 2: **Commands/Data Transition Times Meet Specification, Clock Transition Time Violates Slew Rate**
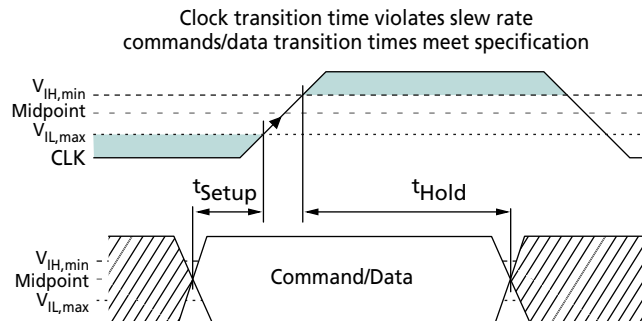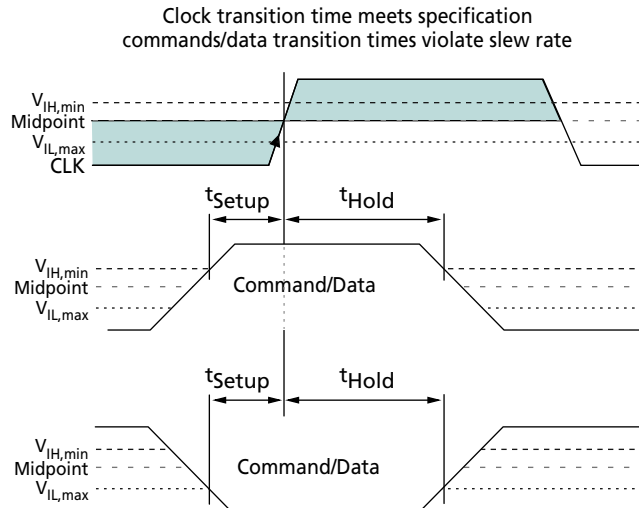
Command/Data Violates Slew Rate

The second example occurs when the clock (CLK) transition time meets specification, but the command/data transition time falls below specification (slew rate < 1V/ns), as seen in Figure 3.

For a rising edge of command/data, ^{t}SETUP must be calculated from the $V_{IH,min}$ (2.0V) of command/data signal to the midpoint (1.4V) of the rising CLK edge (see Figure 3). For a rising edge of command/data, ^{t}HOLD is calculated from the midpoint (1.4V) of the rising CLK signal to the $V_{IL,max}$ (0.8) of the command/data signal.

A falling edge of command/data requires ^{t}SETUP to be measured from the $V_{IL,max}$ (0.8V) of command/data signal to the midpoint (1.4V) of the rising CLK edge. For a falling edge of command/data, ^{t}HOLD is measured from the midpoint (1.4V) of the rising CLK signal to the $V_{IH,min}$ (2.0V) of the command/data signal.

Both rising and falling edge command/data situations require that the memory controller place the command/data values on the bus earlier in order to guarantee the minimum ^{t}SETUP specification. The memory controller must also hold command/data signals longer in order to maintain the minimum ^{t}HOLD specification.

Figure 3:   Clock Transition Time Meets Specification, Commands/Data Transition Times Violate Slew Rate

CLK and Command/Data Violate Slew Rates

The third example occurs when both the clock (CLK) and command/data signal transition times fall below specification, as seen in Figure 4.

For a rising edge of command/data, ^{t}SETUP is calculated from the $V_{IH,min}$ (2.0V) of command/data to the $V_{IL,max}$ (0.8V) of the rising CLK edge. For a falling edge of command/data, ^{t}HOLD is calculated from the $V_{IH,min}$ (2.0V) of the rising CLK edge to the $V_{IH,min}$ (2.0V) of the command/data signal.

For a falling edge of command/data, ^{t}SETUP is calculated from the $V_{IL,max}$ (0.8V) of command/data to the $V_{IL,max}$ (0.8V) of the rising CLK edge. For a rising edge of command/data, the ^{t}HOLD is calculated from the $V_{IH,min}$ (2.0V) of the rising CLK edge to the $V_{IL,max}$ (0.8V) of the rising command/data signal.

Both rising and falling edge command/data situations require that the memory controller place the command/data values on the bus earlier in order to guarantee the minimum ^{t}SETUP specification. The memory controller must also hold command/data signals longer in order to maintain the minimum ^{t}HOLD specification.

Figure 4:   Commands/Data Transition and Clock Times Violate Slew Rate

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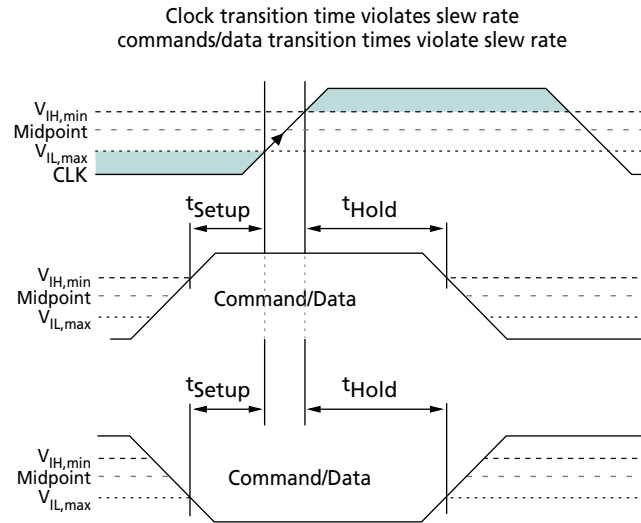
^{t}SETUP EXAMPLE

The example given in Figure 5 uses a Micron MT48LC16M8A2TG-75, PC133, CL = 3 SDRAM to show a scenario in which the clock transition time meets specification, but the command/data transition times exceed specification.

For the following examples, midpoint is represented by MP:

- Clock cycle time: ^{t}CK (CLK) = 7.5ns, slew rate = 1.0V/ns
- Input high voltage (MIN), Logic 1: $V_{IH,min}$ = 2.0V
- Input low voltage (MAX), Logic 0: $V_{IL,max}$ = 0.8V
- Setup time (^{t}SETUP): (^{t}CMS) (MIN) = 1.5ns
- Hold time (^{t}HOLD): ^{t}CMH (MIN) = 0.8ns

For this example, the command/data signals shown in Figure 5 have a slew rate = 0.8V/ns, which falls below the minimum specification of 1.0V/ns.

If the DRAM controller is using the midpoint (1.4V) as a timing reference point for the command/data signal, with a slew rate of 0.8V/ns, ^{t}SETUP$_{MP}$ for the DRAM controller is calculated as follows:

$$^t\text{SETUP(MIN)} + (V_{IH,min} - \text{midpoint})/\text{slew rate}$$

$$^t\text{SETUP}_{MP} = 1.5\text{ns} + (2.0\text{V} - 1.4\text{V})/0.8\text{V/ns}$$

$$^t\text{SETUP}_{MP} = 2.25\text{ns}$$

RESULT: In order to guarantee a minimum setup time of 1.5ns, the DRAM controller needs to start driving command/data signal so that the signal must cross the midpoint 2.25ns prior to the rising CLK reaching 1.4V.

Figure 5: **Clock Transition Time Meets Specification, Commands/Data Transition Times Violate Slew Rate**
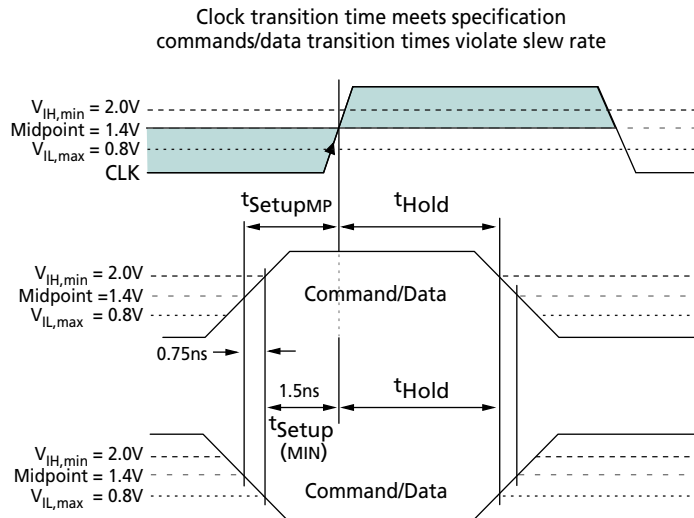
^tHOLD EXAMPLE

The ^tHOLD example in Figure 6 uses the same parameters as the ^tSETUP example in Figure 5—a Micron MT48LC16M8A2TG-75, PC133, CL = 3 SDRAM to show a scenario in which the clock transition time meets specification, but the command/data transition times fall below specification.

For the following examples, midpoint is represented by MP:

- Clock cycle time: ^tCK (CLK) = 7.5ns, slew rate = 1.0V/ns
- Input high voltage (MIN), Logic 1: $V_{IH,min}$ = 2.0V
- Input low voltage (MAX), Logic 0: $V_{IL,max}$ = 0.8V
- Setup time (^tSETUP): (^tCMS) (MIN) = 1.5ns
- Hold time (^tHOLD): ^tCMH (MIN) = 0.8ns

For this example, the command/data signals shown in Figure 6 have a slew rate = 0.8V/ns, which falls below the minimum specification of 1.0V/ns.

If the DRAM controller is using the midpoint (1.4V) as a timing reference point for the command/data signal, with a slew rate of 0.8V/ns, $^tHOLD_{MP}$ for the DRAM controller is calculated as follows:

$$^tHOLD(MIN) + (V_{IH,min} - midpoint)/slew\ rate$$

$$^tHOLD_{MP} = 0.8ns + (2.0V - 1.4V)/0.8V/ns$$

$$^tHOLD_{MP} = 1.55ns$$

RESULT: In order to guarantee a minimum hold time of 0.8ns, the DRAM controller must hold the command/data signal so that the signal does not cross the midpoint sooner than 1.55ns after a rising CLK reaches 1.4V .

Figure 6:   Clock Transition Time Meets Specification, Commands/Data Transition Times Violate Slew Rate
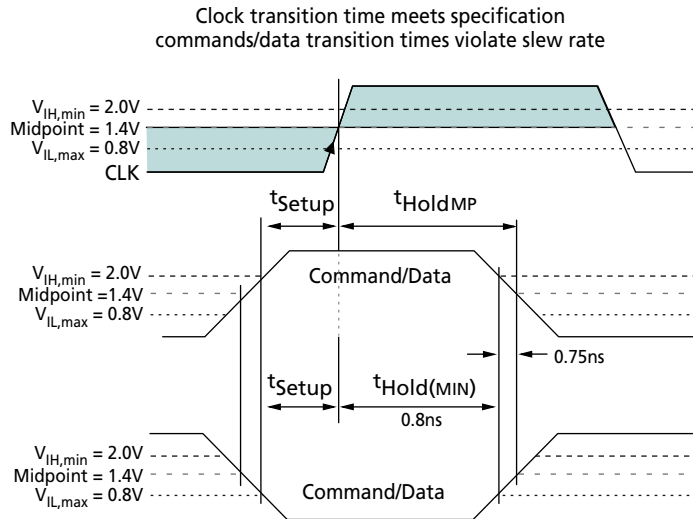
SUMMARY

Designers should pay special attention to the slew rate of SDRAM signals when calculating setup and hold times. If a slower-than-expected slew rate on the clock, command, and/or data signals violates the minimum specification, setup and hold time margins can vary significantly. The midpoint of a transitioning edge is used to calculate setup and hold times when the slew rate meets specification ($\geq$1V/ns). In order to calculate for proper setup and hold times under a slower slew rate conditions (<1V/ns), $V_{IL,max}$ and $V_{IH,min}$ are used instead of the midpoint.

Revision History

Rev. B **11/09**

- Format update and copyediting/wording tweaks.
- "Introduction" on page 1: Reworded first paragraph.
- Changed all instances of "exceed/exceeded" specifications to "fall(s) below" specifications.

Rev. A **10/00**

- Initial release.