

Technical Note

DDR2 (Point-to-Point) Features and Functionality

Introduction

Point-to-point design layouts have unique memory requirements and selecting the right memory can be critical to project success. With many point-to-point designs, memory accounts for only a small percentage of the overall chip count. Other point-to-point designs are complex and may incorporate specialized processors, large pin-count custom ASICs, sophisticated analog circuitry, and thick, multilayered printed circuit boards. Still others may even use the memory on a common node—where memory is shared and independently accessed by different devices.

DRAM has been used extensively on modules and consumed in the personal computer industry where the user can plug and play. For this to happen, the DRAM must be generic and only the minimum functionality is needed. However, DDR2 SDRAM memory has changed this legendary tradition. Unlike previous DRAM, DDR2 SDRAM is designed to provide the point-to-point system designer with versatile options. These options not only enable robust designs, they may also help reduce the overall design time and system cost.

DDR2 SDRAM offers several options:

- Maximum bandwidth up to 800 MT/s (mega transfers per second)
- Supports operations down to 125 MHz clock for debugging and low-power applications
- Adjustable on-die termination (ODT) for I/O that promotes high-quality signal integrity without additional on-board termination
- Signal reflections controlled through selectable output drive levels. Unlike DDR, DDR2 supports this feature on x4, x8, and x16 devices
- Small FBGA package sizes, enabling the placement of high-density devices in extremely compact footprints

A side-by-side comparison of DDR2 with SDR and DDR reveals how DDR2 facilitates these capabilities (see Figure 1 on page 2).

Figure 1: Comparison of DDR2 with Previous Memory Technologies

Single Data Rate (SDR)		Double Data Rate (DDR2)	
Maximum transfer rate	133 MT/s/pin	Maximum transfer rate	800 MT/s/pin
Maximum density	512Mb	Maximum density	2Gb
Maximum operating temperature	85°C	Maximum operating temperature	95°C
Operating voltage ($V_{DD} = V_{DDQ}$)	3.3V	Operating voltage ($V_{DD} = V_{DDQ}$)	1.8V
I/O interface	LVTTTL	I/O interface	SSTL_18
Architecture	Synchronous	Architecture	Source - Synchronous 4n/Prefetch Up to 8 banks
		Features	Differential strobes On-Die termination (50, 75, 100 Ω) Reduced drive on all configurations Small FBGA package sizes Additive latency Supports CL = 3, 4, 5, 6 Change frequency during power-down mode Low-power I_{DD3P} setting
Double Data Rate (DDR)			
Maximum transfer rate	400 MT/s/pin		
Maximum density	1Gb		
Maximum operating temperature	85°C		
Operating voltage ($V_{DD} = V_{DDQ}$)	2.5V		
I/O interface	SSTL_25		
Architecture	Source - Synchronous 2n/Prefetch		

MT/s = Mega transfers per second per pin

DDR2 SDRAM Functional Overview

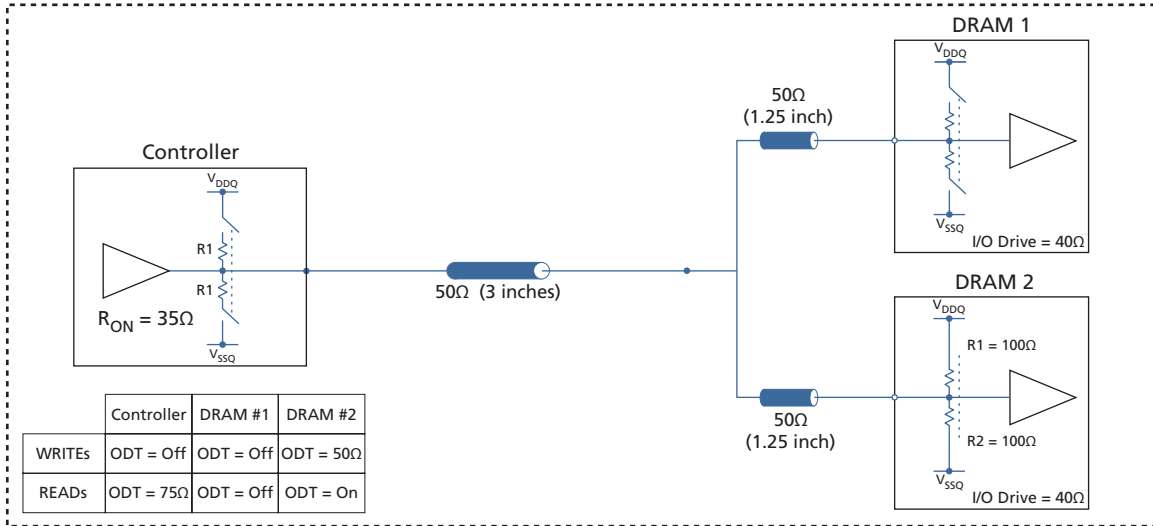
DDR2 SDRAM functions much like DDR SDRAM—a source-synchronous data strobe is used and data is transferred on both the leading and trailing clock edges. However, DDR2 SDRAM has a $4n$ prefetch architecture where the internal data cycle time is one-fourth of the external clock rate and the internal data bus width is four times the size of the external data bus width. For example, a DDR2 SDRAM (x16) device has a 64-bit wide internal data bus, so for each single access into the internal array 64 bits of data are fetched; externally this will provide four data transfers of 16-bits each. Because of the $4n$ prefetch, burst lengths are limited to BL = 4 or BL = 8. In addition to $4n$ prefetch, both the DDR2 core and the I/O operate from a 1.8V power source. Combined with the advanced process technology and lower operating voltage, when compared to SDR or DDR1, DDR2 provides a considerable reduction in overall power consumption.

ODT Examples

By using Micron’s simulator, a one-point-to-two-point layout using DDR2 devices with on-die termination can be compared to DDR2 devices using fixed termination to V_{TT} (ODT = off).

The first example shows the topology using ODT, which is dynamically optimized for READs and WRITEs with DRAM 1 (see Figure 3).

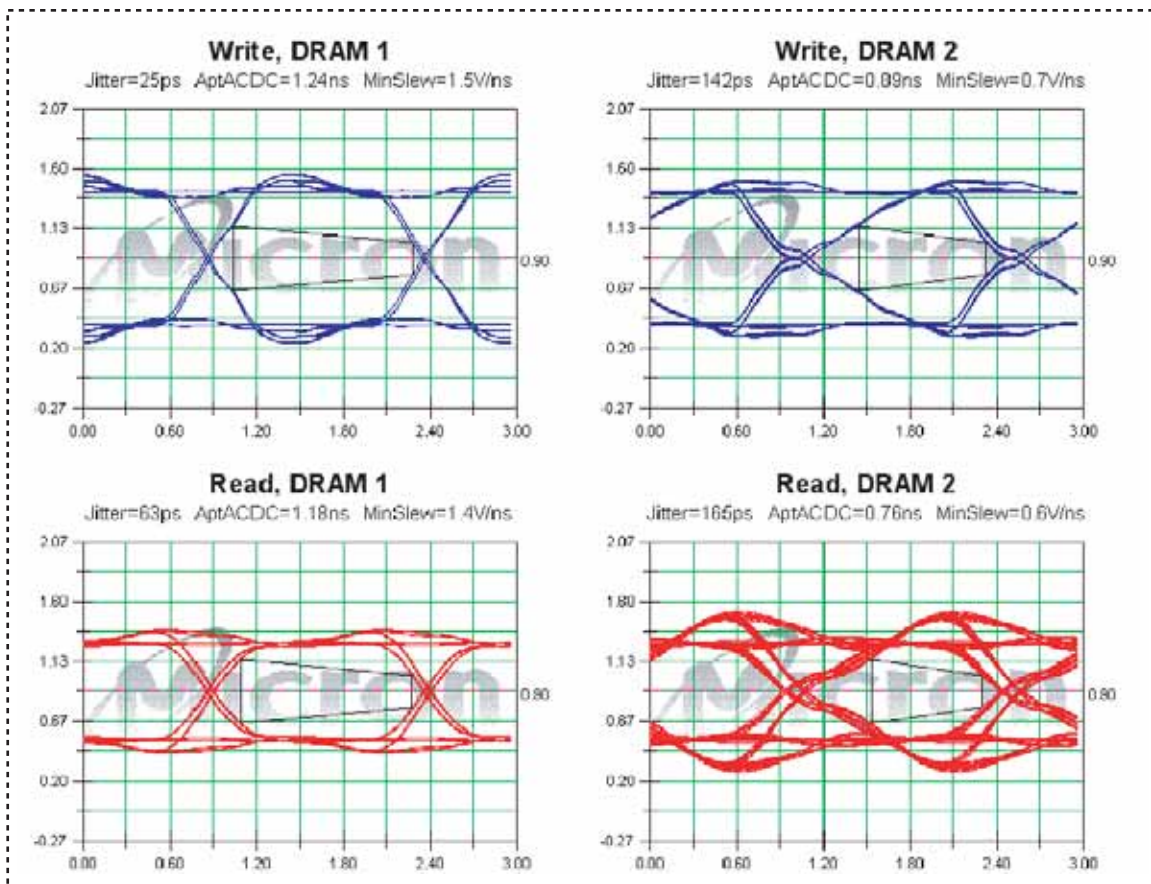
Figure 3: Example 1: Circuit Using ODT



When performing a WRITE to DRAM 1, DRAM 1 has ODT off; DRAM 2 has ODT set to 50Ω, and the memory controller has ODT off. When reading from DRAM 1, the memory controller changes its ODT value to 75Ω; DRAM 1 ODT is off, and DRAM 2 is set to 50Ω

READ and WRITE waveforms for the above example are shown in Figure 4. For READs, the waveforms are captured at the memory controller. For WRITEs, the waveforms are captured at the DRAM.

Figure 4: Example 1: Waveforms Using ODT (-667 Speed Grade)



In Figure 5, the second example has a 100Ω R_{TT} pull-up placed at each DRAM input; this provides an effective 50Ω termination. As an alternative method, some designers may prefer to add only a single R_{TT} pull-up just past the end of the first trace segment. Again, the WRITE waveforms are probed at the DRAM which is written to and the READ waveforms are sampled at the controller. During the READS, the controller provides an effective 75Ω termination to V_{TT} .

Figure 5: Example 2: Circuit Using Fixed R_{TT} Resistors to V_{DD}

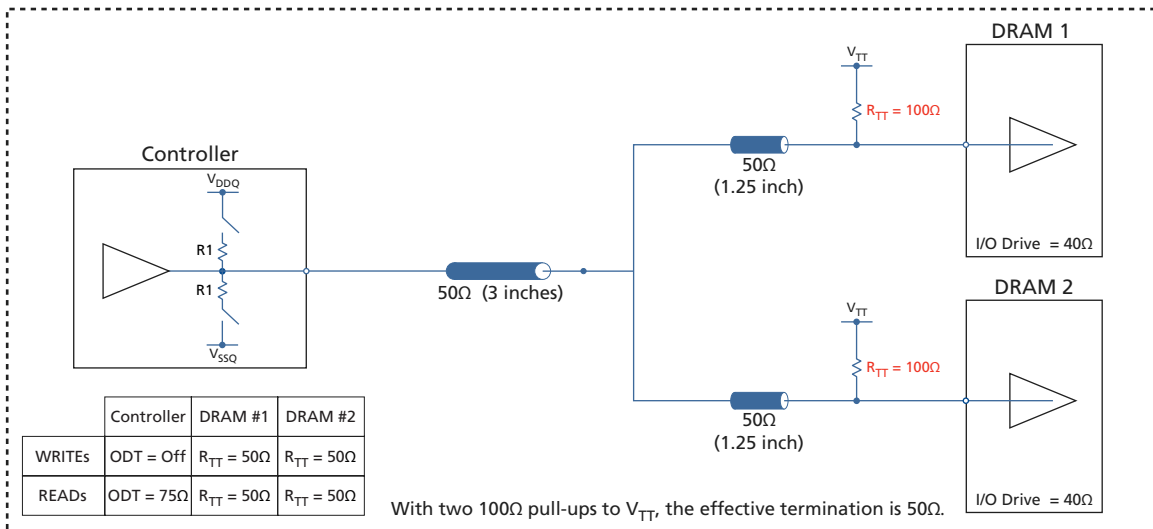
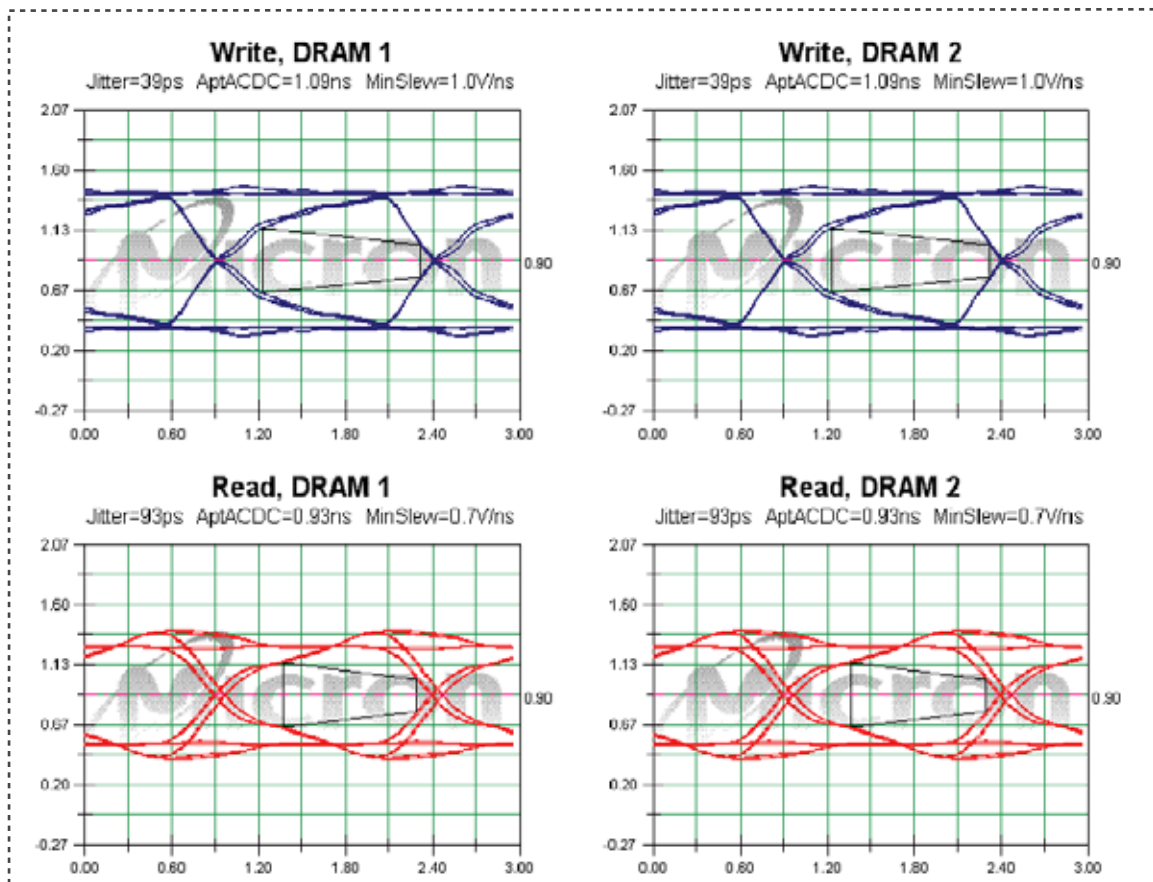


Figure 6: Example 2: Waveforms Using Fixed R_{TT} Resistors to V_{DD} (-667 Speed Grade)



As expected, when the ODT solution is compared to the fixed RTT solution, the eye diagrams from the ODT solutions are better. For example, the ODT optimized WRITE to DRAM #1 shows a larger aperture (aperture width increases from 1.09ns to 1.24ns with improvements in both slew rate and jitter). Likewise, when observing a READ from DRAM #1, there is also a slight improvement in aperture margins and a significant improvement in slew rate (aperture size increases from 0.93ns to 1.18ns, slew rate increases from 0.7V/ns to 1.4V/ns, and jitter is reduced from 93ps to 63ps).

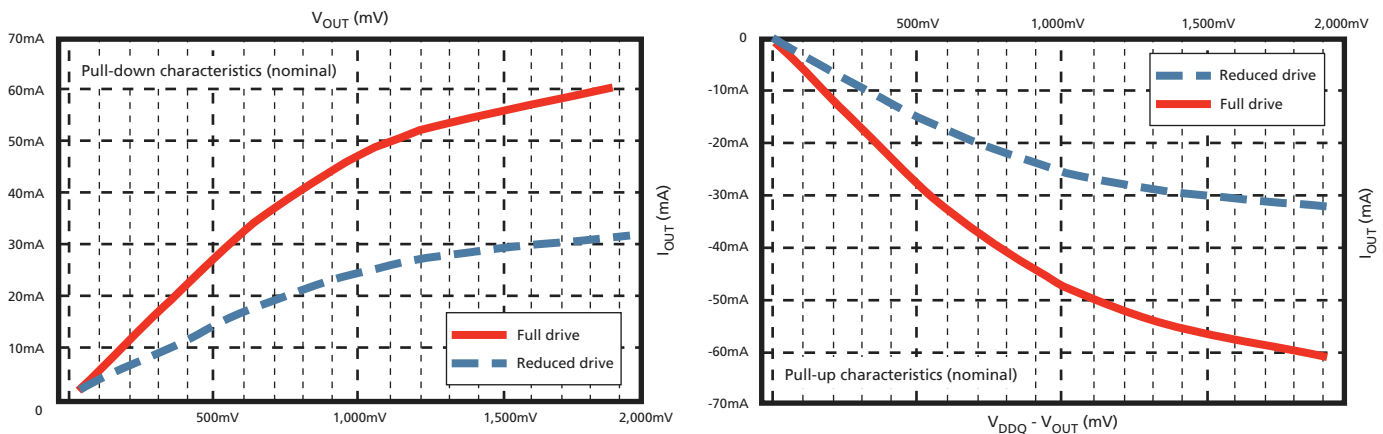
Topology, layout, and device parasitics all play a large role in signal quality, so the results of these simulations are intended for comparison purposes and not as a recommendation for laying out a design.

Output Drive Levels

Point-to-point layout requirements are significantly different from multidrop module layouts. Typically in point-to-point layouts, the position of the memory to the controller is close and the trace lengths are short. Loading rarely includes more than two or three DRAM devices and termination schemes are relaxed. Due to these unique aspects, many point-to-point designs rely on the DRAM's reduced output drive levels to obtain better signal quality and to better match the board impedance. Previous DRAM technologies offered reduced drive I/O on the x16 configuration only. DDR2 SDRAM provides more flexibility because it supports reduced drive I/O on all configurations (x4, x8, and x16).

DDR2 SDRAM configured as full drive has a target output impedance of approximately 18Ω . When the device is configured as reduced drive, the target output impedance is approximately 40Ω . Configuration of the DDR2 device requires the extended mode register (EMR) bit E1 to be set to 0 for full drive or to 1 for reduced drive. Setting the mode register is part of the normal initialization sequence upon device power-up (see the DDR2 device data sheet).

Figure 7: Comparison of Full-Drive to Reduced-Drive I/O (Supported on All Configurations)



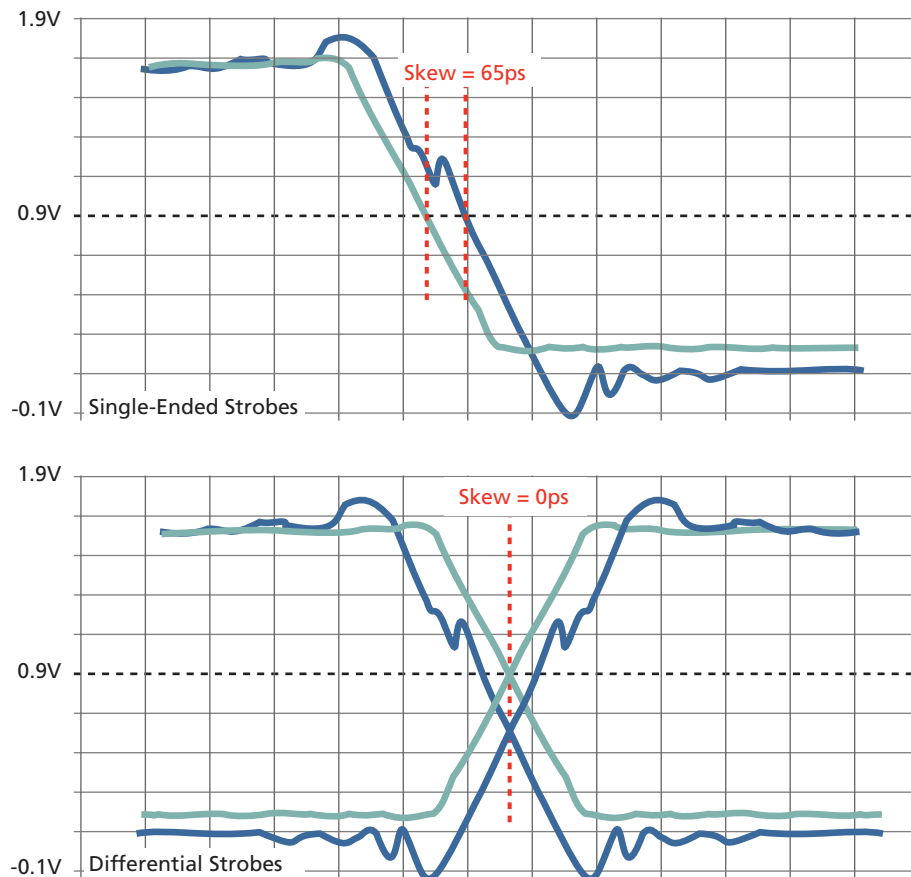
Differential Strobes

A “clean” strobe edge to capture data is essential for a reliable design. Frequently, due to system topology and very high clock rates, a clean strobe can be difficult to obtain. DDR2 technology resolves this problem by supporting differential strobes. With matched differential strobes, the board-level effects are minimized and there is less

interval device switching noise, helping to improve the overall timing margins. For example, on a single-ended strobe, with crosstalk or power supply variations, there can be greater skew in timing. If the same signal variations appear on the differential strobe, the timing offset is minimal, if not zero. Skew examples of single-ended and differential strobe skew are shown in Figure 8.

All DDR2 devices support differential strobes as an option. As with ODT, the DDR2 device must be configured for differential strobes. This is easily done by setting EMR bit E10 to a 1 during the initialization sequence. This will result in the DDR2 SDRAM device driving both DQS and DQS# pads for READ cycles and utilizing both DQS and DQS# inputs for WRITE cycles. If differential strobes are not required, bit E10 is set to 0.

Figure 8: Example of Skew Between Like Single-Ended and Differential Strobes

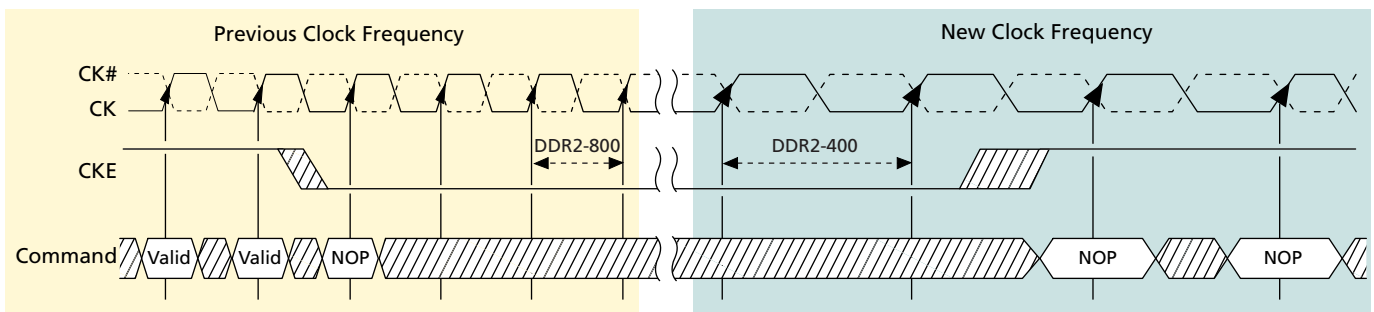


Bandwidth

Micron offers DDR2 devices with maximum input clock rates of 200 MHz, 266 MHz, 333 MHz, 400 MHz, and 533 MHz. These rates translate to high bandwidth for the data bus, with up to 1066 MT/s per pin or 8.5 GB/s for a 64-bit bus. Each of these devices is also tested and guaranteed to operate with a 125 MHz input clock. This slow clock aids with the initial design bring-up or debug process and it assists the system test engineer throughout the life of the product. Additionally, the slower operating frequency can greatly reduce overall power consumption.

The ability to change clock frequencies without power cycling can significantly increase the flexibility of DRAM use, particularly when more than one controller may be sharing the DDR2 memory bus. DDR2 supports changing the clock frequency from its existing clock frequency to any other specified data sheet value while in precharge power-down mode (see Figure 9).

Figure 9: DDR2 Flexibility – Changing the Clock Frequency While in Power-Down Mode

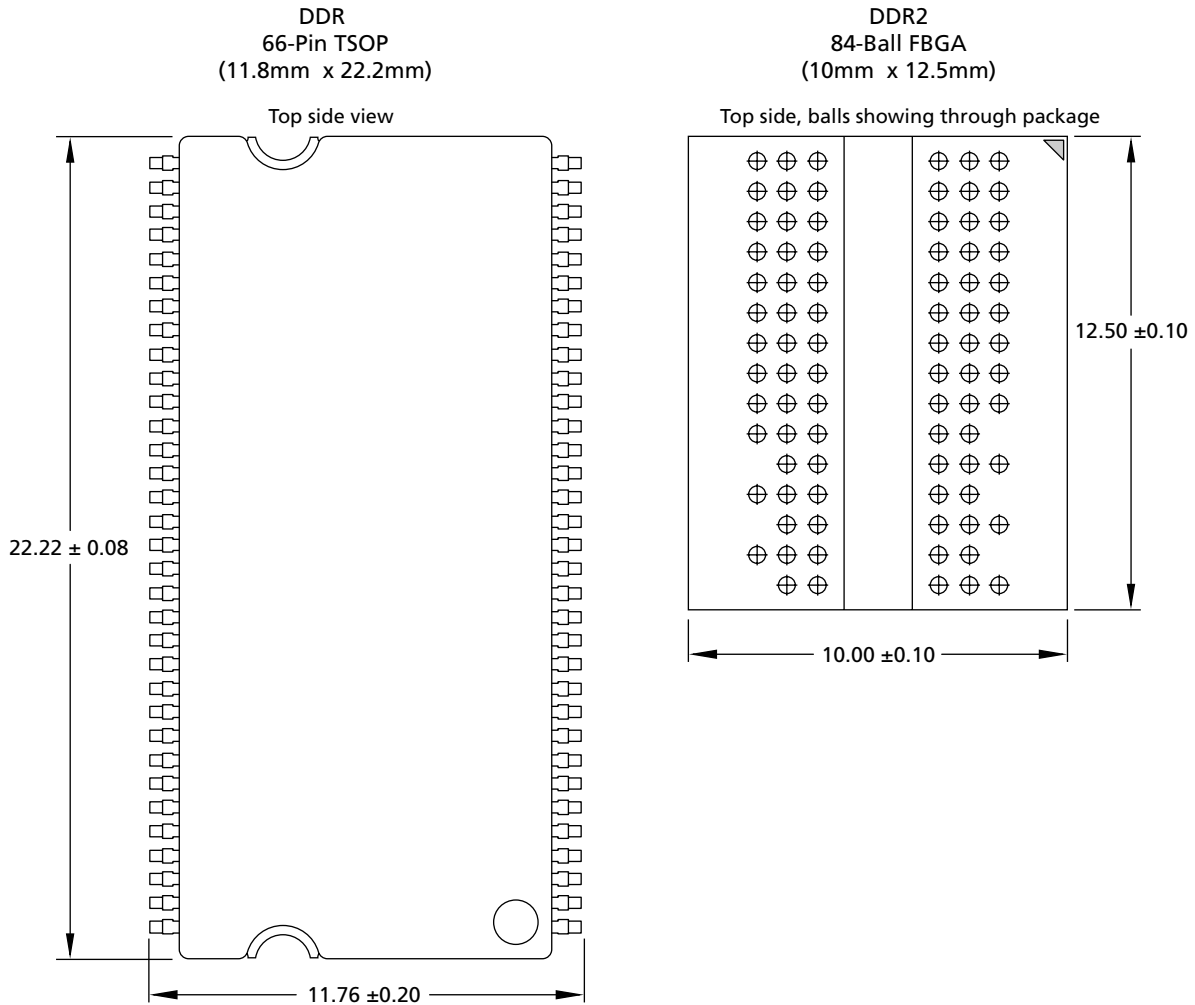


Small Package Size

DDR2 is the first high-volume DRAM product to support compact packages preferred by point-to-point layout designers. All DDR2 packages are FBGA and support compact and common JEDEC footprints. For example, Micron's 2Gb (x16) component is almost identical in size to Micron's 512Mb (x16) component and uses the same 84-ball array.

JEDEC has defined four primary footprints for DDR2 SDRAM. They include the 60-ball or 68-ball for x4/x8 configurations and 84-ball or 92-ball for the x16 configuration. For layout simplicity, a single landing pattern—which can accommodate all DDR2 densities and all configurations—has been developed. Micron® Technical Note TN-47-08, "DDR2 Package Sizes and Layout Requirements," covers this topic in extensive detail. It is available at www.micron.com/ddr2.

Figure 10: 512Mb (x16) Package Size Comparison – DDR to DDR2



High-Temperature Operation

Many point-to-point systems run in adverse system environments where the operating conditions are extreme. Previous DRAM technologies required high-cost industrial temperature parts for support of the extended-temperature operating range of 85°C or higher. The standard commercial grade DDR2 parts are specified with an operating temperature of 85°C.

Note: Previous DRAM devices were specified with an ambient operating temperature, which was difficult to quantify. For all DDR2 parts, the operating temperatures are specified at the case (t^{CASE}). In addition, DDR2 devices are also available with an operating temperature of t^{CASE} equal to 95°C.

For high-temperature operation, the device requires a higher refresh rate. The standard periodic refresh interval (t^{REFI}) is 7.8 μ s (64ms for the full array) for all DDR2 densities. However, when operating DDR2 devices above a t^{CASE} of 85°C, the periodic refresh interval (t^{REFI}) changes from 7.8 μ s to 3.9 μ s (32ms for the full array).

To ensure self refresh also performs at the increased refresh rate, the device must be configured at its initialization sequence. To configure self refresh mode for high-temperature operation, the extended mode register 2 (EMR2) bit E7 must be set to 1.

Addressing

The majority of point-to-point designs do not utilize high-density memory, but after the layout is complete and released to production, the product life span may be five to ten years. Throughout this time, system requirements may demand a shift to a higher density part. DDR2 addressing makes this transition easy because the page size for all components is either 1KB or 2KB, depending on density and configuration. See Figure 11 for address mapping.

Figure 11: Required Addresses for Density and Configuration

Configuration	Required Addresses	(Connected / Not Connected)
256Mb (x4/x8)	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2	
256Mb (x16)	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2	
512Mb (x4/x8)	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2	
512Mb (x16)	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2	
1Gb (x4/x8)	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2	
1Gb (x16)	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2	
2Gb (x4/x8)	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2	
2Gb (x16)	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2	

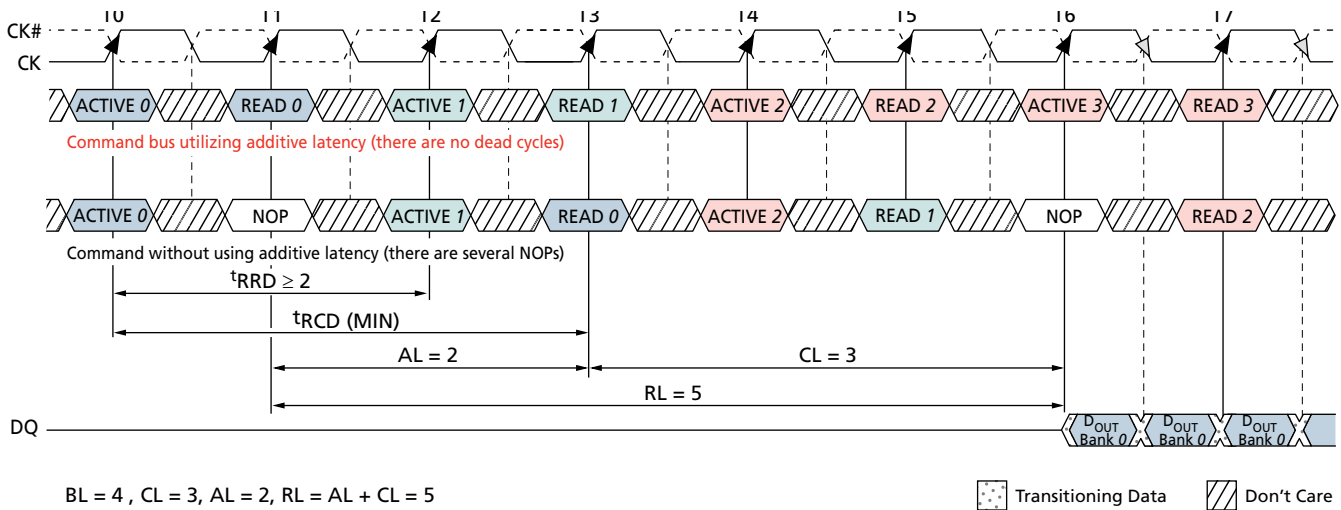
DDR2 Enhancements

Beyond the features related directly to point-to-point designs, DDR2 SDRAM supports a rich array of enhancements, including additive READ/WRITE latency and a low-power, power-down exit mode.

Additive Latency

To optimize the command bus for maximum bandwidth, DDR2 enables the controller to select an additional 1-, 2-, 3-, or 4-clock-cycle delay from the time of the READ or WRITE command to the standard CAS latency. This feature provides more throughput and flexibility on the command bus while interleaving banks within the DRAM.

Figure 12: Additive Latency Example (Command Bus Optimization)



Reduced Power Consumption

Even though the percentage of DRAM to other components is typically low on most point-to-point designs, power consumption is still a concern. DDR2 SDRAM operates with both the core and I/O voltage set to 1.8V nominal. This low voltage setting combined with Micron’s advanced process technologies help to significantly reduce overall memory power consumption. In addition, some point-to-point designs that use ODT in an optimized layout have eliminated the need for a dedicated V_{TT} power source.

Low Power (Active Power-Down)

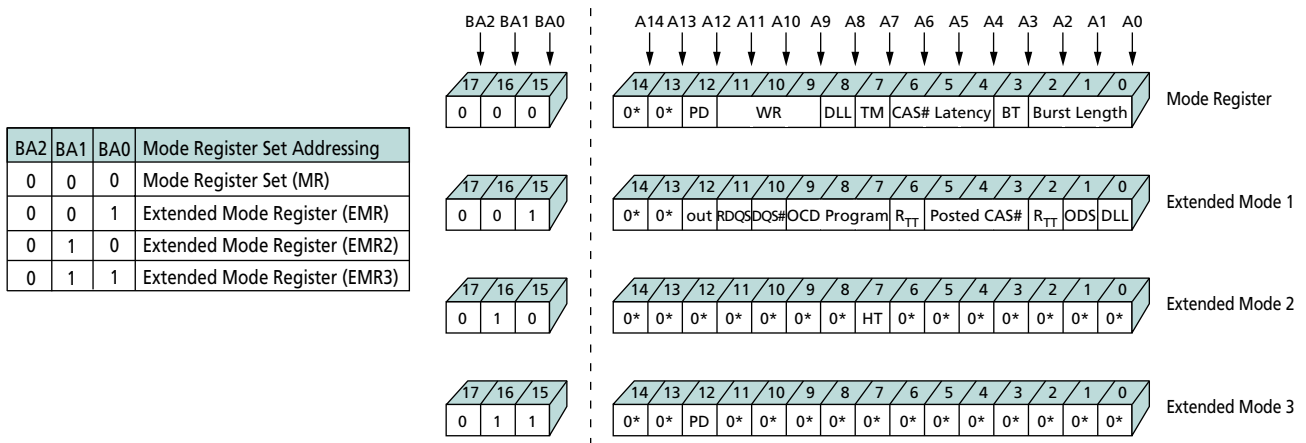
When the DDR2 device exits the standard I_{DD3P} condition (active power-down), it can accept a READ command immediately after t_{XARD} time ($t_{XARD} = 2$ clocks). To do this, the internal DLL is kept running while the device is in the power-down mode. The typical DLL consumes approximately 15mA.

To save power, the DDR2 SDRAM can be configured for a “slow” I_{DD3P} exit where the first READ command comes t_{XARDS} after the exit (t_{XARDS} time = 7 clocks, assumes DDR2-667 with AL = 0). By pushing out the READ command several clock cycles, the DLL can be frozen during the I_{DD3P} time, which reduces active power-down current. To do this, the mode register (bit M12) must be set to 0 for standard (fast) exit or 1 for low-power (slow) exit.

Configurable Options

DDR2 configuration options are enabled and set within the mode registers. DDR2 SDRAM has four mode registers. First is the base mode register (MR), which has the basic functions—CAS latency, burst type, burst length, and several others. Second is the extended mode register 1 (EMR or EMR1), which covers most of the more unique options—ODT, additive CAS latency, output drive strength, and more. Third is the extended mode register 2 (EMR2), which enables the controller to configure the device for 2x refresh while in high-temperature operation. Fourth is the extended mode register 3 (EMR3), which is reserved for future use. Figure 13 on page 13 shows an overview of the DDR2 mode registers. Refer to the Micron DDR2 SDRAM data sheet for complete description and functionality.

Figure 13: Extended Mode Registers (Addressing and Register Locations)



Design Support and Availability

Micron makes it easy to design and lay out point-to-point systems using DDR2 SDRAM. A full collection of complete device models, in-depth DDR2 data sheets, power calculators, a library of extensive DDR2 technical notes, a custom DDR2 signal simulator that produces eye diagrams for timing analysis, and other unique, design-related resources are available at: www.micron.com/ddr2.

Not only is there an abundance of support and tools exclusively from Micron, but most ASIC and FPGA vendors offer DDR2 cores and interfaces. Some of the companies supporting DDR2 development include Altera, Lattice, LSI, and Xilinx. Micron offers all densities, configurations, and speed grades from 256Mb through 2Gb, including DDR2-800 for most devices.

Conclusion

DDR2 SDRAM provides unprecedented features for point-to-point system designs. Some of the most popular options include ODT, differential strobes, ultra small FBGA package sizes, high-temperature operating capability, and 40Ω output impedance.

The flexibility of ODT enables most layouts to be completed without needing additional discrete passive components for termination—saving board space, simplifying routing, and reducing production costs. Smaller DDR2 FBGA packages support the placement of DRAM in close proximity to the memory controller. This keeps signal traces shorter which helps with signaling concerns and optimizes board space.

The reduced drive I/O has an impedance of approximately 40Ω to help control signal quality. For DDR2 devices, the reduced I/O feature is now offered in all configurations (x4, x8 and x16). For applications that are used in demanding environments where the ambient temperature is extreme, DDR2 offers flexible solutions with its extended maximum case temperature of up to 95°C, with 2x refresh.

With the added benefits of volume-produced DDR2 SDRAM, this technology is has become the preferred choice for point-to-point designs.

For additional DDR2 information, and for the latest data sheets, refer to Micron's Web site at www.micron.com/ddr2.

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Revision History

Rev. B	3/11
<ul style="list-style-type: none">• Updated to reflect current product performance• Updated formats	
Rev. A	4/06
<ul style="list-style-type: none">• Initial release	