Technical Note

Backward Compatibility for Faster LPDDR SDRAM

Introduction

LPDDR SDRAM speed grades have increased significantly over years of design evolution, but Micron's newer, faster parts are designed to be fully backward compatible with older, slower parts, providing flexibility and compatibility between speed grades. In fact, Micron's faster speed grade parts use the same designs as slower speed grade parts, but the faster parts are tested to tighter limits.

This technical note reviews the timing differences between the faster and slower speeds and explains how faster parts function compatibly with slower parts.

This technical note covers only the speed grades and configurations defined by JEDEC standard JESD209B.

AC Timing Parameters

The AC timings listed in all of Micron's data sheets are asynchronous unless they appear in clock cycles in the units column of the AC timing tables. The timing parameters listed in the data sheet are also independent of the clock frequency. The asynchronous timing parameters need to be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge for the appropriate command, regardless of the speed grade. For example, a ^{t}RCD specification of 15ns with a 200 MHz clock (5ns period) results in 3 clocks. Equation 1 covers any case where 2 < ^{t}RCD (MIN) / ^{t}CK = 3. (The same procedure is used to convert other specification limits from time units to clock cycles.)

(EQ 1)

$$\begin{aligned}\text{Actual clocks required} &= {}^{t}\text{RCD}_{(\text{Spec})} \;/\; \text{Actual clock cycle time}\\ &= 15\text{ns} / 5\text{ns}\\ &= 3.0 \text{ clocks}\\ &= 3 \text{ clocks (rounded up to whole number)}\end{aligned}$$

Table 1 shows some of the core timing parameters for the x16 and x32 configurations. The higher speed grade is fully backward compatible with the lower speed grade.

Table 1: Comparison of Key Timing Parameters (x16, x32)

Parameter	-5	-6	Units
^{t}CK @ CL3	5	6	ns
^{t}CK @ CL2	12	12	ns
^{t}RP	15	18	ns
^{t}RCD	15	18	ns
^{t}RAS	40	42	ns
^{t}RC	55	60	ns
^{t}RFC	72	72	ns
^{t}QH	1.75	2.05	ns

Frequency

Unlike standard DDR, there is no minimum clock frequency for LPDDR SDRAM, regardless of the speed grade. The minimum clock frequency found in the DDR specification results from using the DLL to align the data and strobe with the clock. LPDDR SDRAM devices do not use a DLL; therefore, there is no required minimum ^{t}CK restriction. LPDDR SDRAM devices can be run at almost any speed so long as the AC timing parameters are met. The two timing parameters that restrict the minimum clock frequency are refresh and ^{t}RAS MAX. This allows the operating frequency to move from the maximum specified in the data sheet well into the kHz range.

Low Power and Automotive Industrial Temperature

Low power and automotive industrial temperature LPDDR SDRAM devices have been tested to tighter specifications. This allows applications that do not use the extended temperature range or lower self refresh power to use parts that have been tested for automotive industrial temperature ranges.

Conclusion

Micron strives for full backward compatibility in its planning, testing, and development. Micron speed grades are 100% backward compatible with original, industry-standard speed grades.

For the latest data sheets and other technical information, visit Micron's Web site at www.micron.com/datasheets.

Revision History

Rev. B 2/13

- Update ^{t}QH row values in Comparison of Key Timing Parameters (x16, x32) table.

Rev. A 1/13

- Initial release

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