Technical Note

LPDDR2 Dual Die Package to Single Die Package Migration

Introduction

This technical note provides information to enable migration of a Micron 1Gb LPDDR2 product from a dual-die package to a single-die package. Changes to density, bandwidth, or trace routing in the PCB design are unnecessary.

For complete specifications, see the respective product data sheet. This technical note does not include memory controller firmware changes required to move from dual die to single die. Customers are advised to re-simulate the system for SI confirmation.

The LPDDR2 Product Details table shows dual-die and single-die part numbers and essential differences between the DDP and SDP devices.

Table 1: LPDDR2 Device Details

Architecture	Device	
	MT42H16M32D2 (DDP)	MT42H32M32D1 (SDP, Monolithic)
Density per package	1Gb	1Gb
Die per package	2	1
Ranks (CS_n) per channel	1	1
Channels per die	1	1

Address Changes

Timing related changes necessary to transition from DDP to SDP are shown in the Address Changes table here.

Table 2: Address Changes – All Configurations

Parameter	DDP	SDP
Configuration	4 Meg x 32 x 4 banks x 1ch	4 Meg x 32 x 8 banks x 1ch
Die	2	1
Row address	8K (A[12:0])	8K (A[12:0])
Bank address	4 (BA[1:0])	8 (BA[2:0])
Column address	1K (A[9:0])	512 (A[8:0])
Page size	2KB	2KB

Ball Connection Changes

After completing the following ball connection changes, verify all connections, values, and system signal integrity simulations. Information to help verify these design changes and confirm signal integrity is in technical note *TN-52-02: Point-to-Point System Design: Layout and Routing Tips for LPDDR2 and LPDDR3 Devices*.

A system firmware change to adjust the controller and DRAM DQ/DQS drive strength may be required depending on system signal integrity simulation results.

Table 3: Ball Connection Changes

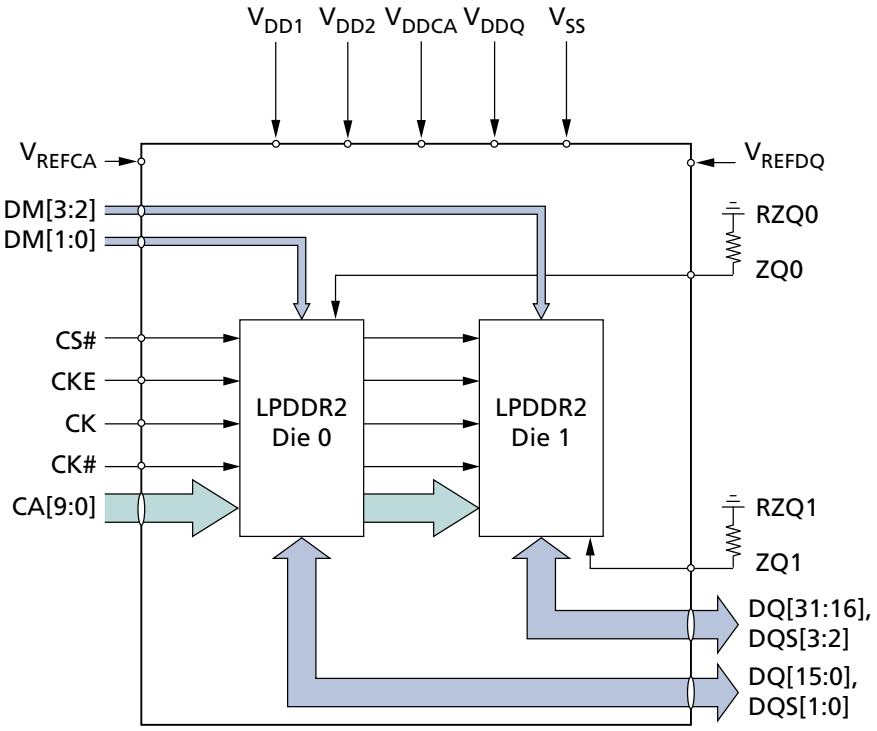
Note applies to entire table.

Ball Number	DDP	SDP
C3	ZQ1	NC

Note: 1. NC = No connection, either to the SDP device or to other balls within the SDRAM package. It is recommended that remaining PCB traces connected to the NC balls be driven to V_{SS} or V_{DD} via a system firmware change.

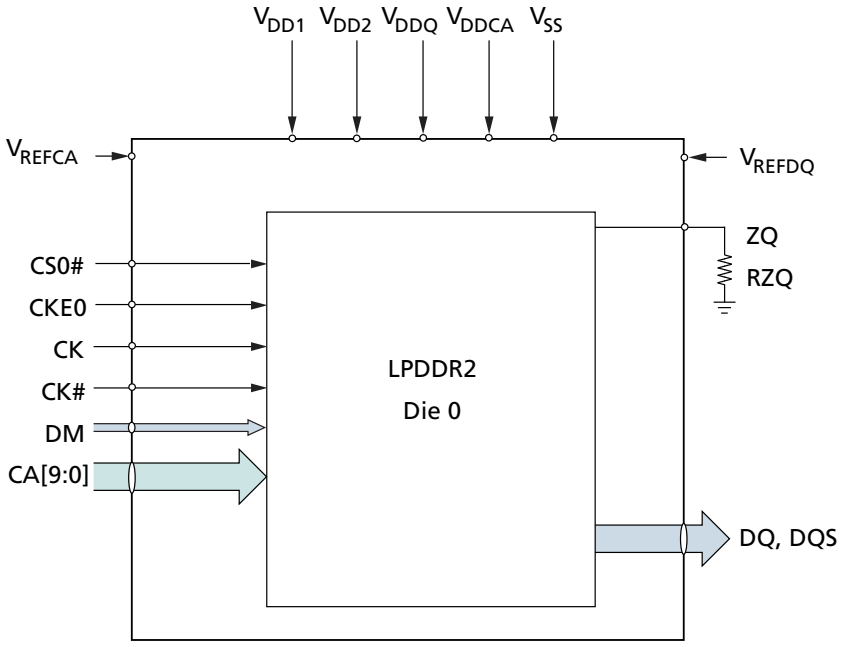
Block Diagram – DDP

Figure 1: Functional Block Diagram for DDP – 4 Meg x 32 x 4 Banks x 1 Channel (2 Die)



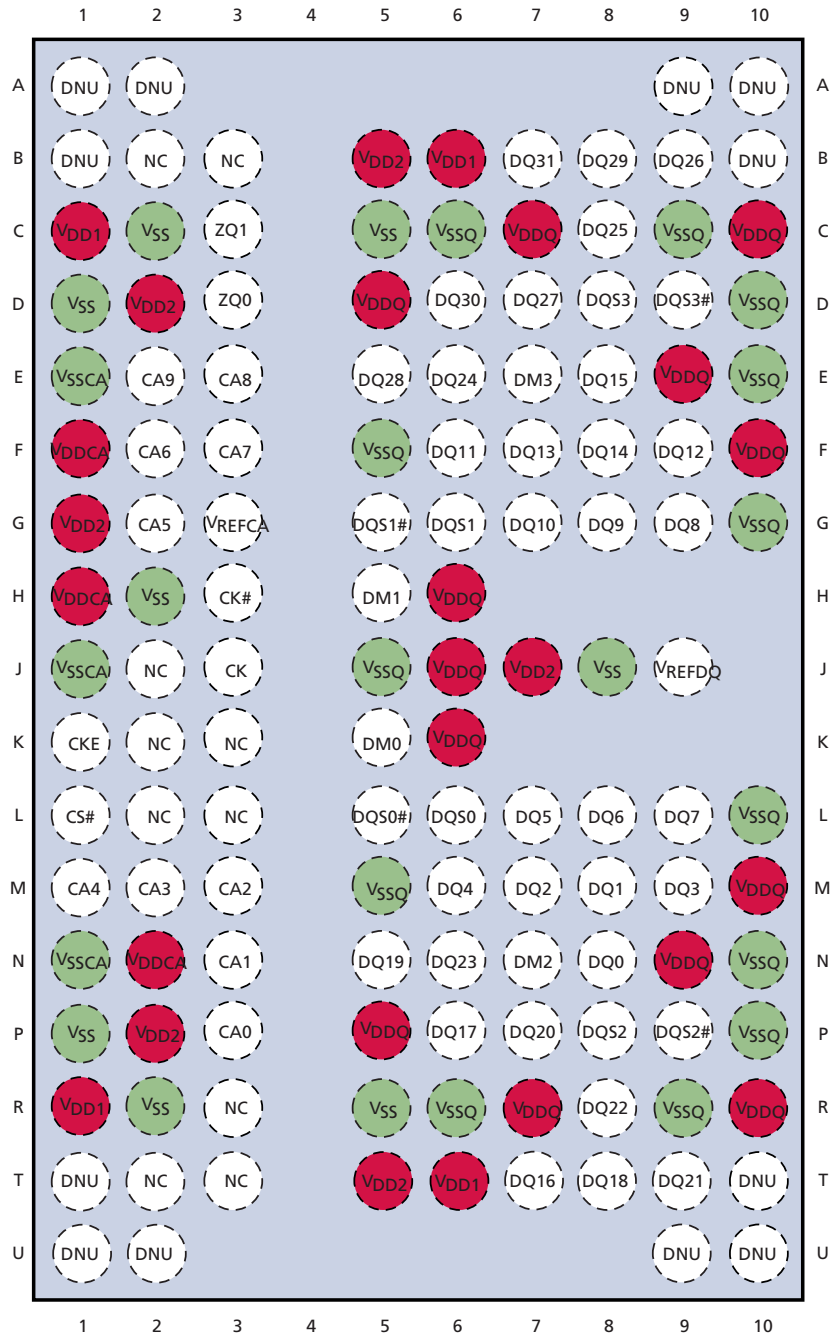
Block Diagram – SDP

Figure 2: Functional Block Diagram for SDP – 4 Meg x 32 x 8 Banks x 1 Channel



Ballout – DDP

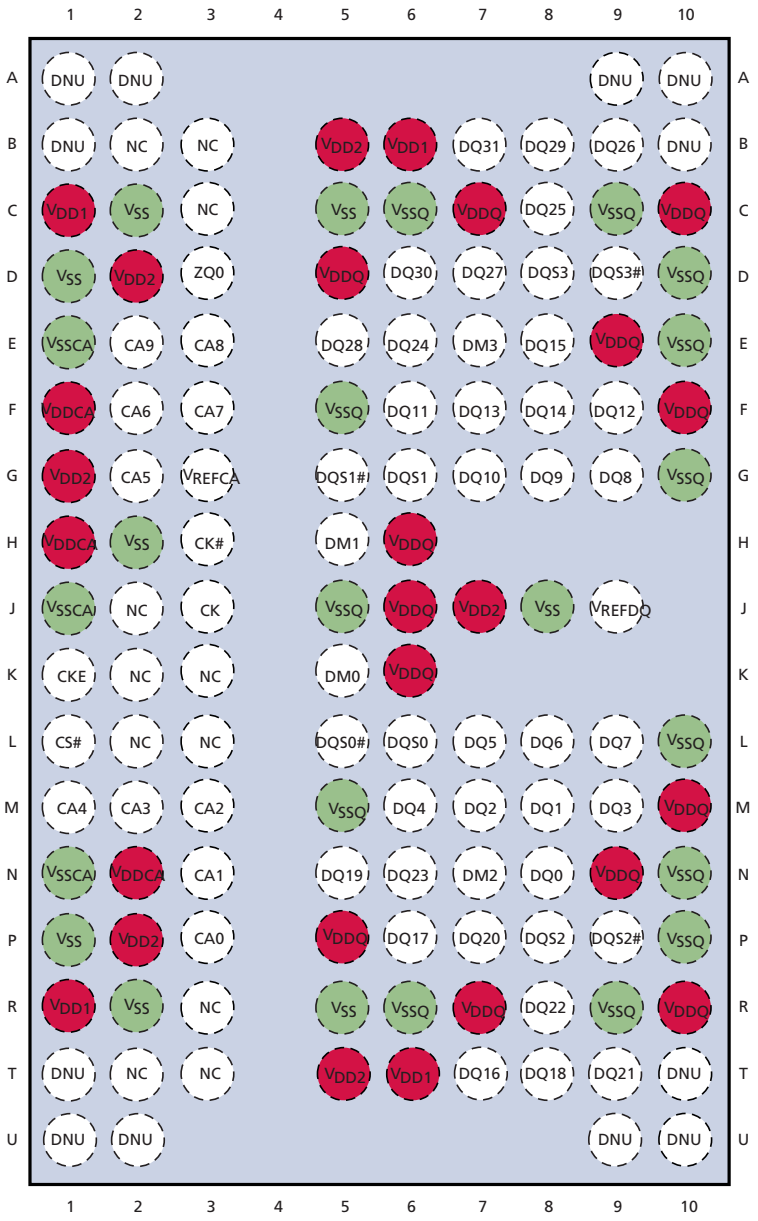
Figure 3: DDP Ball Assignments – 134-Ball FBGA (x32 Top View)



Notes: 1. Die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.
2. See the Ball Connection Changes table for DDP to SDP migration.

Ballout – SDP

Figure 4: SDP Ball Assignments – 134-Ball FBGA (x32 Top View)



Notes: 1. Die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.
2. See Ball Connection Changes table for DDP to SDP migration.

Revision History

Rev. A – 12/14

- Initial release

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