Technical Note

Adding ECC to a Data Bus with DDR4 x16 Components

Introduction

Systems with lower density memory requirements use x16 DRAM components to save space, cost and power. System designers who also have high data integrity requirements may want to implement ECC using an extra 8-bit data path, making for some awkward combinations of components on the data bus. DDR4 creates additional challenges caused by the different number of bank groups on x8 and x16 components. This technical note provides guidance for adding ECC on a single-rank, point-to-point DDR4 data bus when using x16 components.

Note: All tables in this technical note are based on current production DDR4 devices available at the time of publishing: 4Gb Rev. B (25nm Z90B) and 8Gb Rev. B (20nm Z01A). Component area is based on package size only and does not include board area needed for signal routing.

DDR4 Bus Configurations

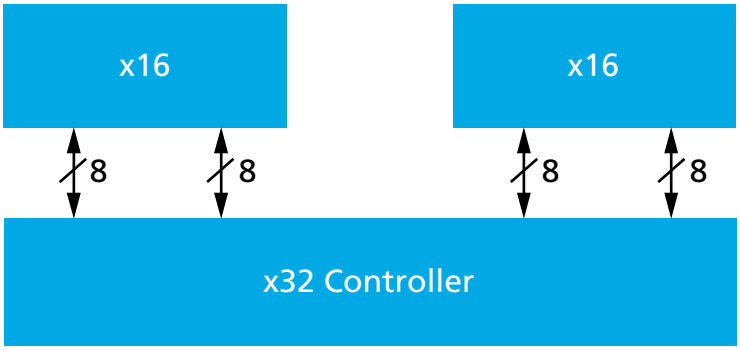
The most common data widths for adding ECC to data paths are x32 and x64. Table 1 shows the three lowest densities that can be configured on a single-rank 32-bit DDR4 bus; Table 2 shows the same information for a 64-bit DDR4 bus. The lowest density is always achieved using x16 components, but there are two ways to configure the next highest density. Figures 1 and 2 outline how the components are connected for each bus width.

Table 1: DDR4 Single-Rank x32 Bus Configuration Options

Configuration	Density	Component Area	I_{DD7} @ 2400 MT/s
4Gb x16 (2 pcs)	1GB	252 mm2 (Rev. B)	578 mA
8Gb x16 (2 pcs)	2GB	224 mm2 (Rev. B)	498 mA
4Gb x8 (4 pcs)	2GB	378 mm2 (Rev. B)	844 mA
8Gb x8 (4 pcs)	4GB	384 mm2 (Rev. B)	700 mA

Figure 1: x32 Bus Configuration Diagrams

a) With x16 Components



b) With x8 Components

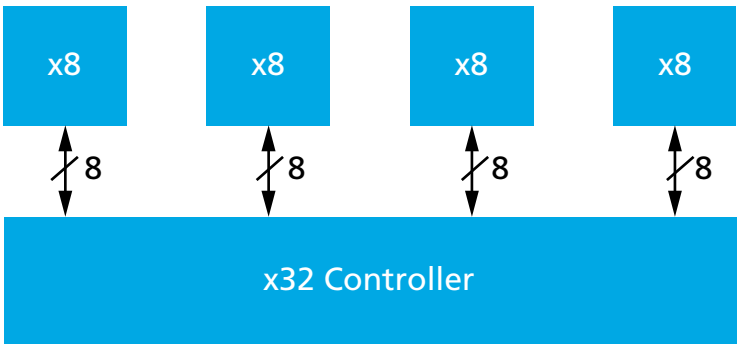
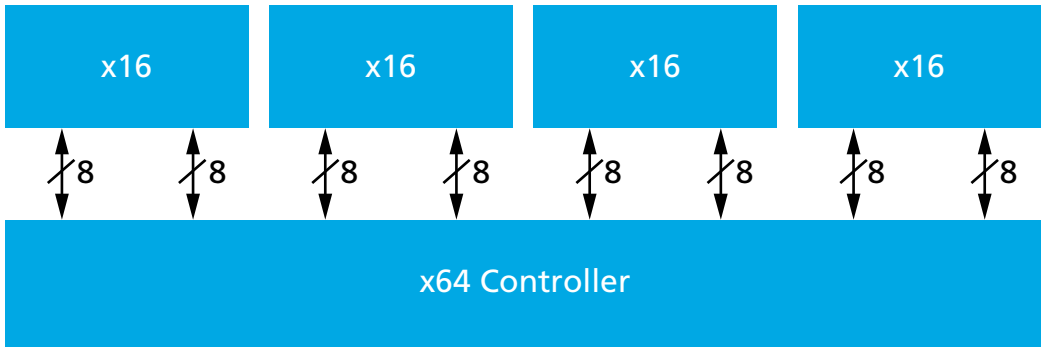


Table 2: DDR4 Single-Rank x64 Bus Configuration Options

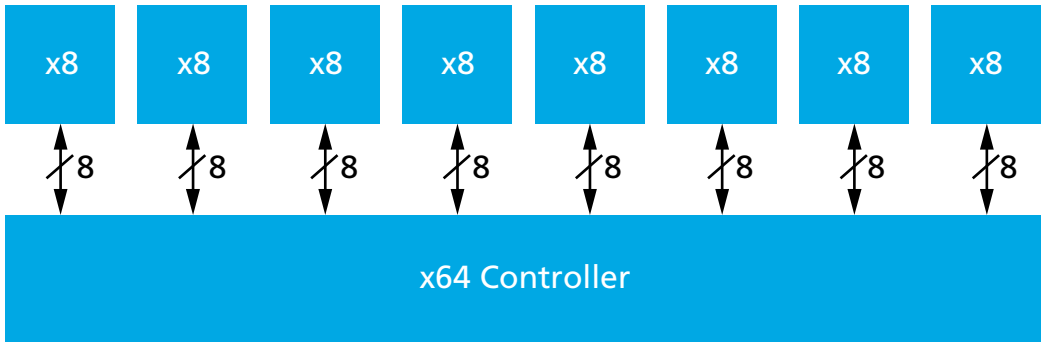
Configuration	Density	Component Area	I_{DD7} @ 2400 MT/s
4Gb x16 (4 pcs)	2GB	504 mm2 (Rev. B)	1156 mA
8Gb x16 (4 pcs)	4GB	448 mm2 (Rev. B)	996 mA
4Gb x8 (8 pcs)	4GB	756 mm2 (Rev. B)	1688 mA
8Gb x8 (8 pcs)	8GB	768 mm2 (Rev. B)	1400 mA

Figure 2: x64 Bus Configuration Diagrams

a) With x16 Components



b) With x8 Components



The tables above show that when there is a choice between x16 and x8 components, the x16 configuration has clear advantages in board area and power consumption over the same density x8 configuration. In addition, the controller has fewer loads on the command/address/clock signals when using x16 components. The reduced loading can help with layout, signal integrity and even controller power for driving these signals.

Adding ECC

As mentioned in the introduction, the system requirements for some applications require an additional level of data integrity and confidence, and this is commonly addressed using ECC. For 32- and 64-bit data paths, ECC protection is provided by adding an extra 8 bits, making buses that are 40-bits and 72-bits wide, respectively. (It is beyond the scope of this document to discuss the implementation and merits of specific ECC schemes.)

There are several challenges when adding ECC to a DDR4 bus. The ECC component must be selected to match the addressing used by the other components on the bus. Because x16 DDR4 components have only two bank groups and x8 components have four bank groups, it is not possible to use a x8 component of half the density (as could be done for DDR3 designs). The addressing for a x8 DDR4 component forces the ECC device to be the same density as the x16 component, and half of the density goes unused in the form of two extra bank groups.

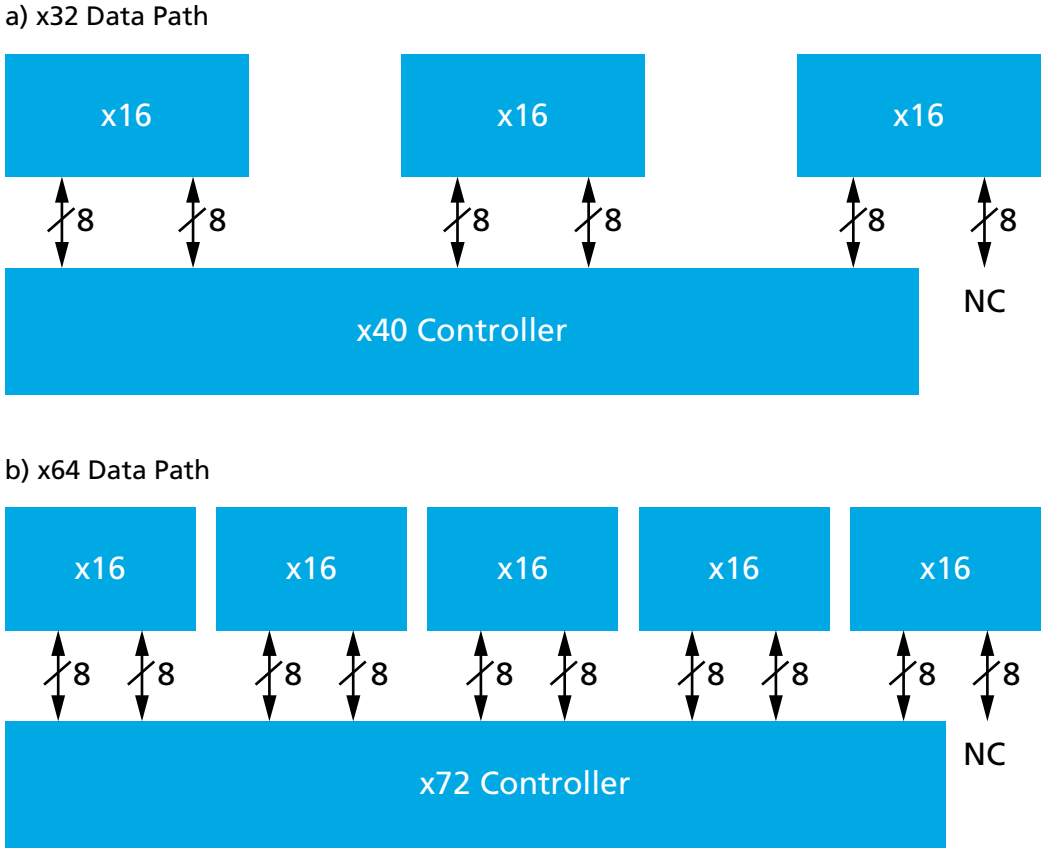
The alternative is to use a x16 component for ECC. To make the row and column addressing match the data components, the ECC component must have the same density. Using the same density x16 component has the advantage of simplifying the BOM somewhat (all DDR4 devices are identical), but it does result in an unused byte lane on the ECC component.

We will examine both options.

ECC With an Additional x16 Component

As mentioned above, using an additional x16 component for ECC simplifies the DRAM portion of the BOM because the same component is used for all placements on the bus, but it has disadvantages as well. Compared to a x8 ECC component, the x16 power will be slightly higher and it will use a bit more board space. In addition, there is an unused byte lane that must be terminated. The following figure shows a high-level diagram of adding a x16 component for ECC.

Figure 3: Adding a x16 Component for ECC



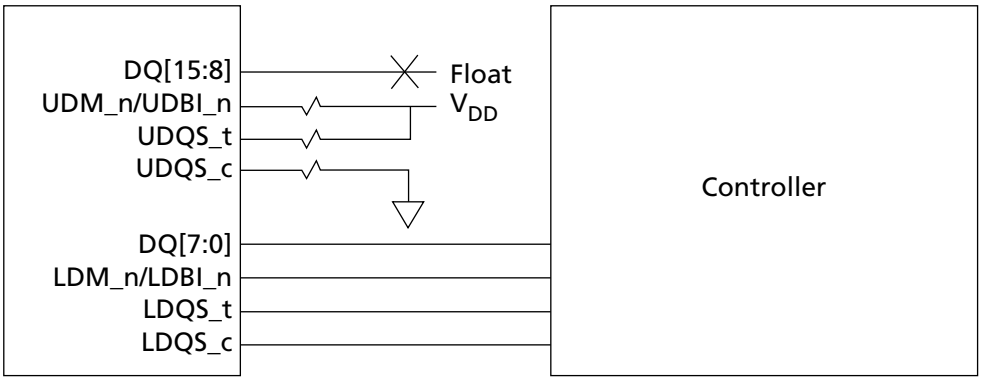
When using a x16 component for ECC, the lower byte lane (DQ[7:0]) must be used for the ECC bits. DDR4 memory is capable of per-DRAM addressability (PDA), and this function is used during the DDR4 device initialization sequence for V_{REFDQ} calibration. PDA is enabled by DQ0, so the lower byte lane must be used and connected to the controller.

The unused upper byte lane should be terminated as follows:

- DQ[15:8] can be left floating (ODT will terminate to V_{DDQ})
- UDM_n/UDBI_n should be terminated to V_{DDQ} (allows DM or DBI to be enabled)
- UDQS_t should be terminated to V_{DDQ}
- UDQS_c should be terminated to V_{SSQ}

Figure 4 shows the details of these connections.

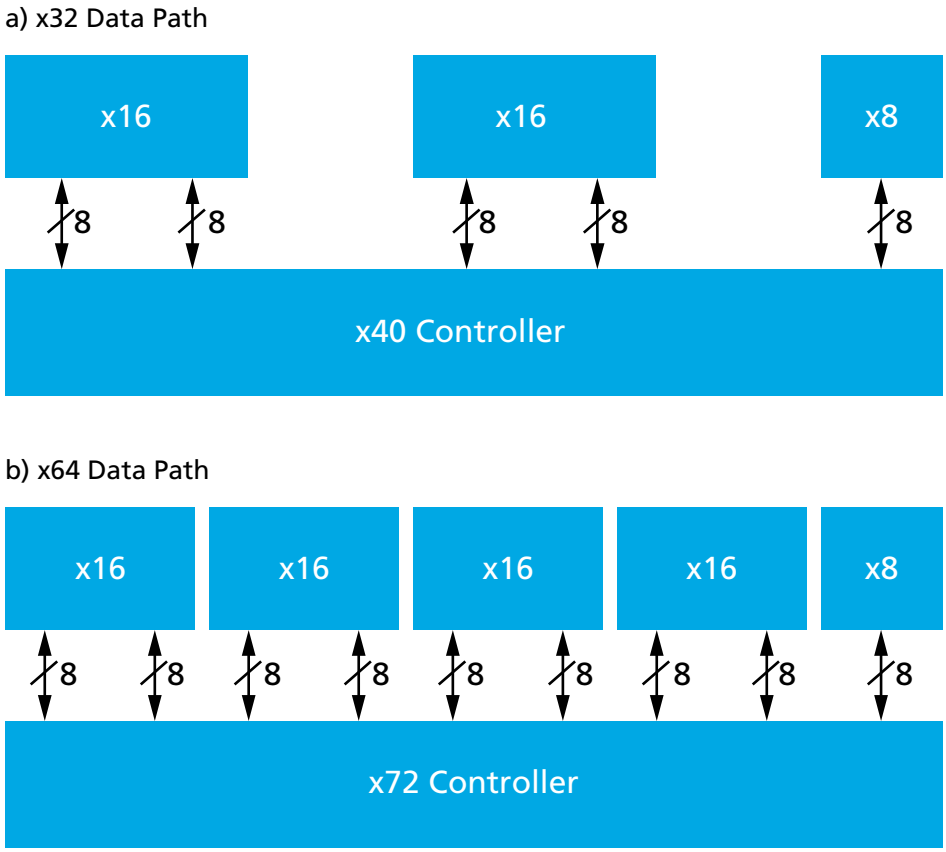
Figure 4: DDR4 x16 Component Connected as ECC Device



ECC With an Additional x8 Component

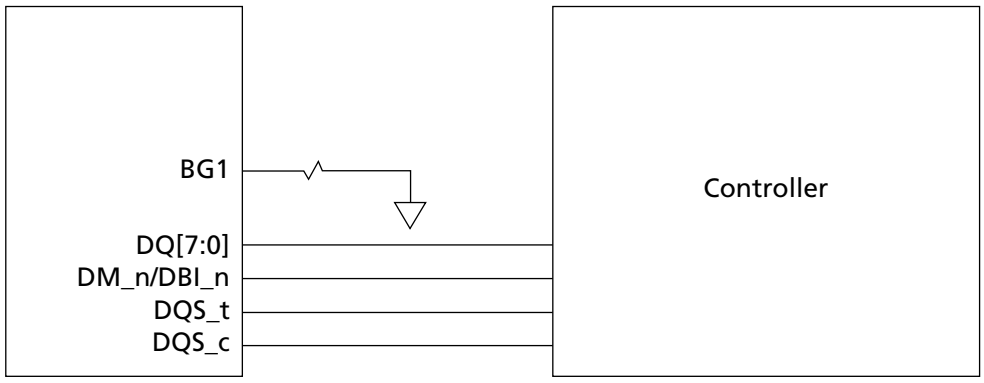
Using an additional x8 component for ECC results in slightly lower power and will use slightly less board space than a x16 component. In addition, there is no unused byte lane to terminate. But, matching the address configuration of the x16 data components begins with a x8 ECC component of the same density as the x16, with half of the bank groups disabled. Figure 5 shows a high-level diagram of adding a x8 component for ECC.

Figure 5: Adding a x8 Component for ECC



Half of the bank groups are disabled by tying BG1 to V_{SSQ}, as shown in Figure 6. This enables command/address parity. Because the unused BG1 input on the x16 devices is treated as a zero, the parity generated by both the x16 and the x8 devices will be the same.

Figure 6: DDR4 x8 Component Connected as ECC Device

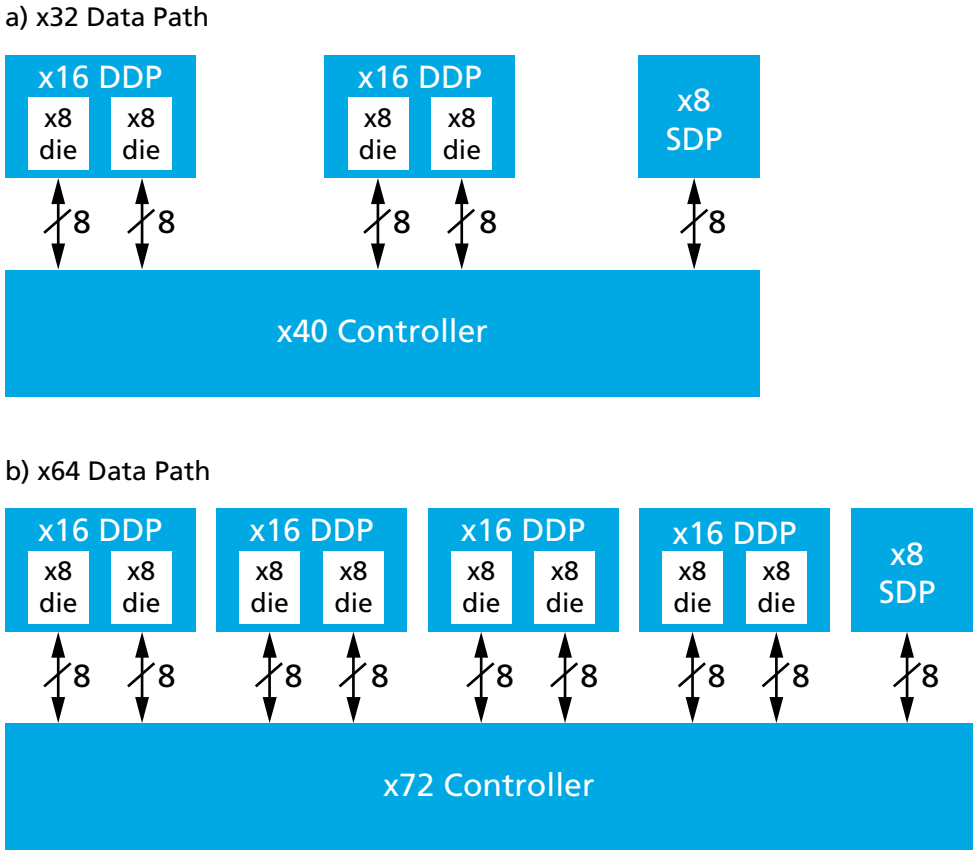


Considerations for Using DDR4 x16 DDP

The DDR4 standard includes a special configuration for a x16 dual die package (DDP). This device contains two x8 die connected as a single rank. Although more expensive than two discrete x8 DDR4 packages, the DDP occupies considerably less board area. This makes it an excellent option where higher density is needed, but board space is constrained. Because the DDP uses x8 die, BG1 is required on the x16 DDP package. (A second ZQ is also required on the board; for suggestions on designing a board that accepts both standard x16 DDR4 and DDP x16 DDR4 devices, see TN-40-40: DDR4 Point-to-Point Design Guide.)

When adding ECC to a data bus using x16 DDP devices, the most economic choice is to use an additional discrete x8 component for the ECC device. No special connections are needed, as all devices use BG1, and all DQ signals (byte lanes) are used. Figure 7 shows an overview for adding ECC when using x16 DDP devices.

Figure 7: Adding ECC to x16 DDP Components



DDR4 Bus with ECC

Tables 3 and 4 compare the key parameters for the various options of adding ECC to DDR4 buses of various densities. Table 3 shows these results for a x32 data path (x40 total bus width), and Table 4 shows them for a x64 data path (x72 total bus width).

Table 3: Key Parameters for x32 DDR4 Data Path With ECC

x32 w/ECC	Density	Component Area	I_{DD7} @ 2400 MT/s
Using x8 ECC Component			
4Gb x16 (2 + 1 pcs)	1GB	347 mm2 (Rev. B)	789 mA
8Gb x16 (2 + 1 pcs)	2GB	320 mm2 (Rev. B)	673 mA
4Gb x8 (5 pcs)	2GB	473 mm2 (Rev. B)	1055 mA
8Gb x8 (5 pcs)	4GB	480 mm2 (Rev. B)	875 mA
16Gb x16 DDP (2 + 1 pcs)	4GB	320 mm2 (Rev. B)	875 mA
Using x16 ECC Component			
4Gb x16 (3 pcs)	1GB	378 mm2 (Rev. B)	876 mA
8Gb x16 (3 pcs)	2GB	336 mm2 (Rev. B)	747 mA

Table 4: Key Parameters for x64 DDR4 Data Path With ECC

x64 w/ECC	Density	Component Area	I_{DD7} @ 2400 MT/s
Using x8 ECC Component			
4Gb x16 (4 + 1 pcs)	2GB	599 mm2 (Rev. B)	1367 mA
8Gb x16 (4 + 1 pcs)	4GB	544 mm2 (Rev. B)	1171 mA
4Gb x8 (9 pcs)	4GB	851 mm2 (Rev. B)	1899 mA
8Gb x8 (9 pcs)	8GB	864 mm2 (Rev. B)	1575 mA
16Gb x16 DDP (4 + 1 pcs)	8GB	544 mm2 (Rev. B)	1575 mA
Using x16 ECC Component			
4Gb x16 (5 pcs)	2GB	630 mm2 (Rev. B)	1455 mA
8Gb x16 (5 pcs)	4GB	560 mm2 (Rev. B)	1245 mA

As the tables show, using x16 data components with a x8 component for ECC results in the lowest power and the least board area. Using a x16 component for ECC simplifies the BOM (and thus the procurement process) at the cost of small increases in power and board area, plus a slight added complexity in terminating an unused byte lane.

The x16 DDP provides the same density and power as using all x8 components, but at the same component area as the standard x16 with the x8 ECC component. Thus, you get twice the density in the same board area.

Write CRC

System designers who wish to use the DDR4 write CRC feature as a debug or verification tool should be aware that using this feature also influences the choice of which component to use for ECC. Because the inputs of the x16 component's unused byte lane are left floating and pulled up by on-die termination (ODT), it is not possible to insert zeroes that would be required for the CRC bits and ALERT_n will be triggered.

If write CRC is a desired feature for the system, a x8 component must be used.

Conclusion

There are several viable choices for adding ECC to low-density DDR4 buses. The optimal choice for any design will be the balance of power, board space and BOM complexity (including additional terminations for unused signals on the byte lane). The guidelines presented here will help the designer find the implementation with the right balance for their needs.

Revision History

Rev. A – 3/18

- Initial release

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