Technical Note

SDRAM I/O Characteristics Comparison of 54nm to 130nm Die

Introduction

This technical note compares the I/O characteristics of the 54nm to the 130nm single data rate (SDR) synchronous dynamic random access memory (SDRAM) die. It includes the following graphical representations: pull-up and pull-down I/V curves and transient analysis simulations representing the 130nm SDRAM product and comparing this data to the more recently released 54nm product.

Note: The graphs and diagrams in this technical note are for general reference only. We suggest that customers use simulations to ensure that their systems are not adversely affected by the differences in I/O characteristics between 54nm and 130nm devices. The models referenced in this technical note are available at: www.micron.com.

SDRAM Process Shrink

Micron SDR SDRAM devices built with the 130nm process have been available and in use for many years. However, it has become necessary to migrate these devices to a smaller 54nm process to take advantage of the latest manufacturing processes and technology.

The SDRAM devices built with the 54nm process are fully compatible with those built with the 130nm process. However, there are differences in the I/O (driver and receiver) characteristics between the 54nm and 130nm devices.

Pull-Up/Pull-Down I-V Curves

The graphs for pull-up/pull-down characteristics are derived from the specific IBIS models for each SDRAM device. The red curves represent the fast, typical, and slow corners for the 130nm devices; the blue curves represent 54nm devices.

Simulations

The 130nm and 54nm SDRAM models were optimized to work with an industry-standard controller model. Transient analysis simulations were performed using IBIS models in two industry-standard simulators using a pulse stimulus. A PRBS pattern was used as a stimulus in the second simulator to generate eye diagrams.

Technology Comparisons by Density

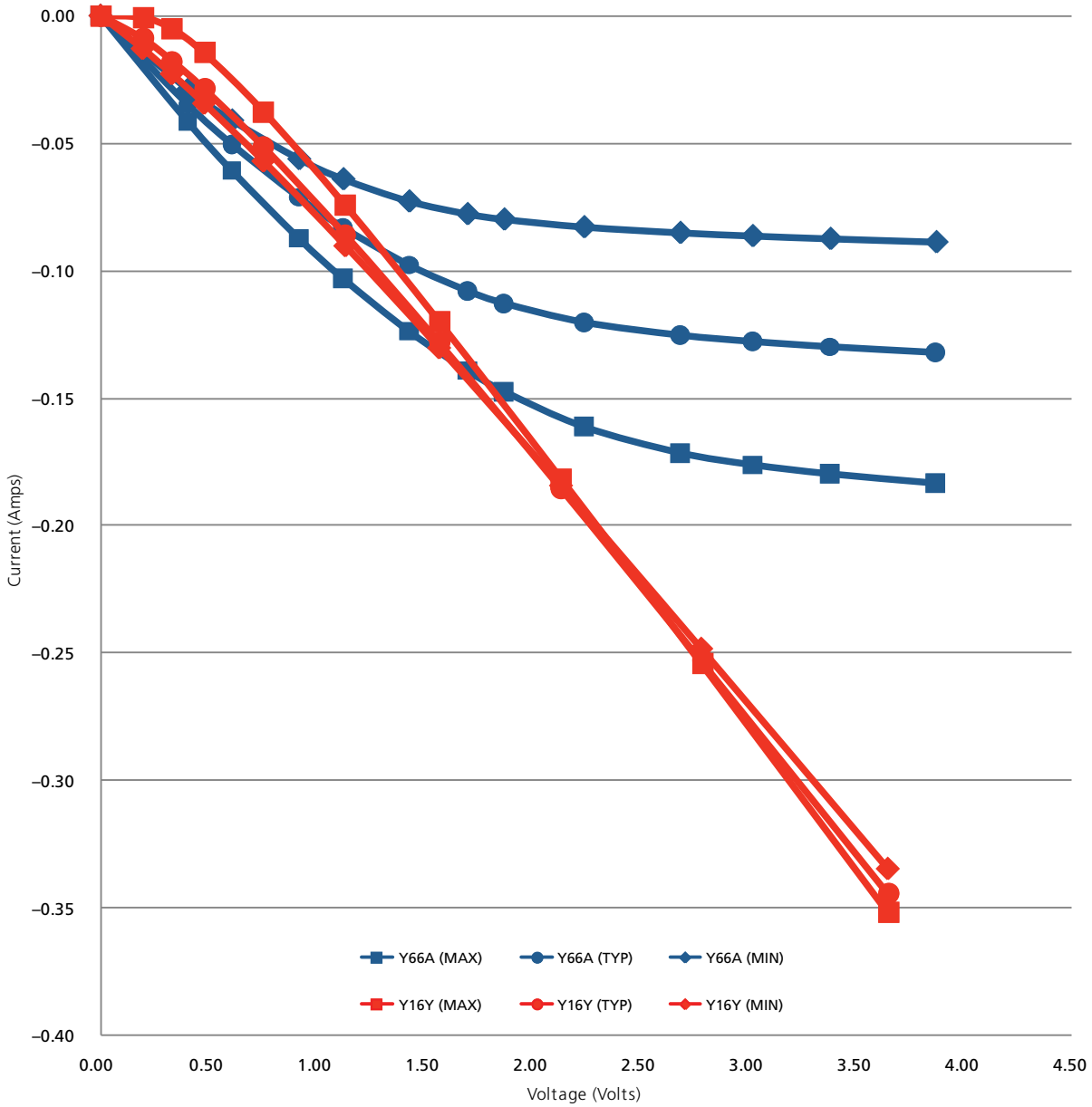
The following sections compare the 54nm technology to the 130nm technology by density:

- I/O Characteristics Comparison – 256Mb 54nm/130nm (Y66A/Y16Y)
- I/O Characteristics Comparison – 128Mb 54nm/130nm (Y65A/Y15W)
- I/O Characteristics Comparison – 64Mb 54nm/130nm (Y64A/Y14W)

I/O Characteristics Comparison – 256Mb 54nm/130nm (Y66A/Y16Y)

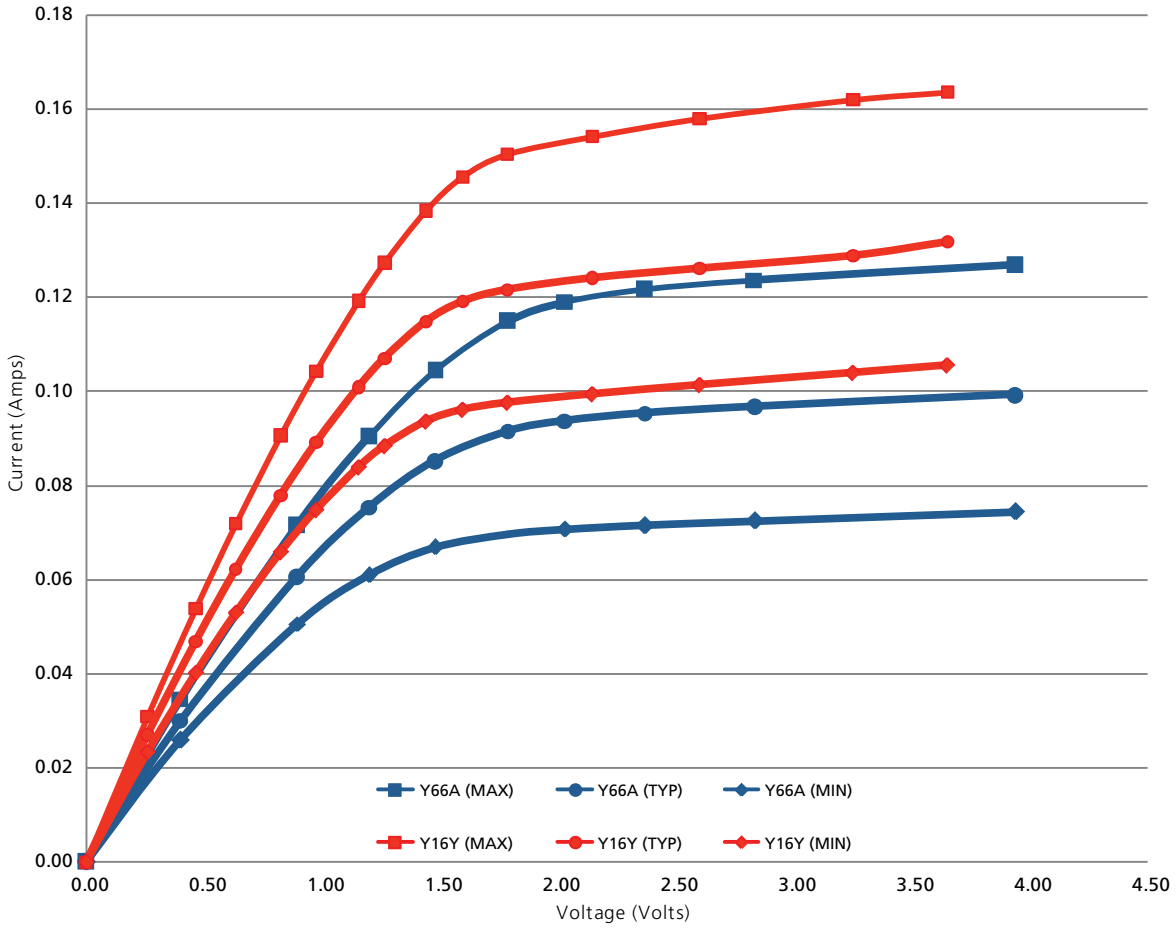
Pull-Up/Pull-Down I-V Curves – 256Mb 54nm/130nm (Y66A/Y16Y)

Figure 1: Pull-Up I-V Curves – 256Mb 54nm/130nm (Y66A/Y16Y)



Notes:
1. Blue curves represent fast, typical, and slow corners for the 54nm pull-up I-V curves.
2. Red curves represent fast, typical, and slow corners for the 130nm pull-up I-V curves.

Figure 2: Pull-Down I-V Curves – 256Mb 54nm/130nm (Y66A/Y16Y)



Notes:
1. Blue curves represent fast, typical, and slow corners for the 54nm pull-down I-V curves.
2. Red curves represent fast, typical, and slow corners for the 130nm pull-down I-V curves.

Test Procedure – 256Mb 54nm/130nm (Y66A/Y16Y)

The following setup and test procedures were used to perform transient and eye diagram simulations:

1. The Y16Y device was optimized to work in a test setup with a customer controller.
2. Transient and eye diagram simulations were performed using the Y16Y device in the system.
3. The Y16Y device was replaced with the Y66A device while the rest of the system remained unchanged.
4. Transient and eye diagram simulations were performed using the Y66A device in the system.
5. Test results for the Y66A and Y16Y devices were compared.

Figure 3: Test Setup – 256Mb 54nm/130nm (Y66A/Y16Y)

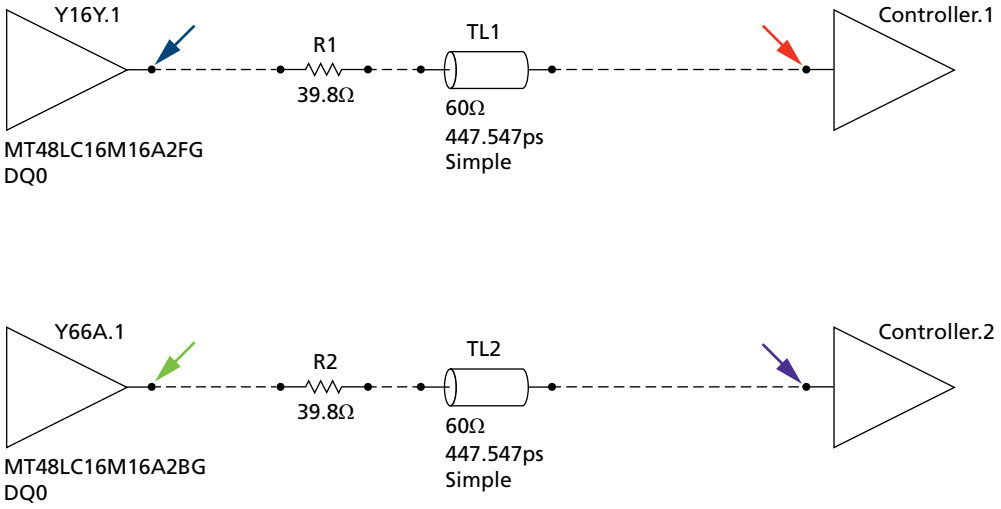


Figure 4: Transient Analysis 1 – 256Mb 54nm/130nm (Y66A/Y16Y)

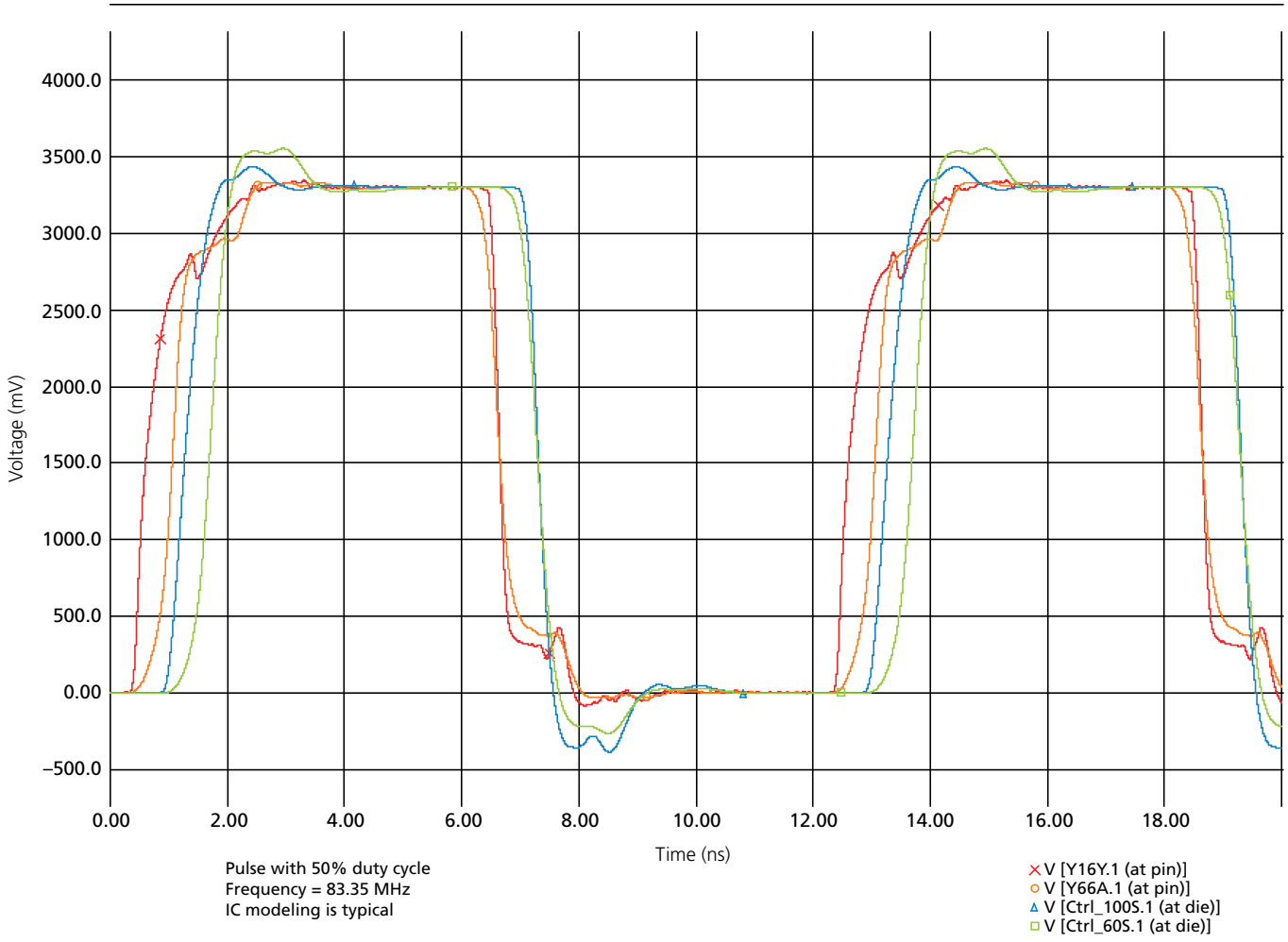


Figure 5: Transient Analysis 2 – 256Mb 54nm/130nm (Y66A/Y16Y)

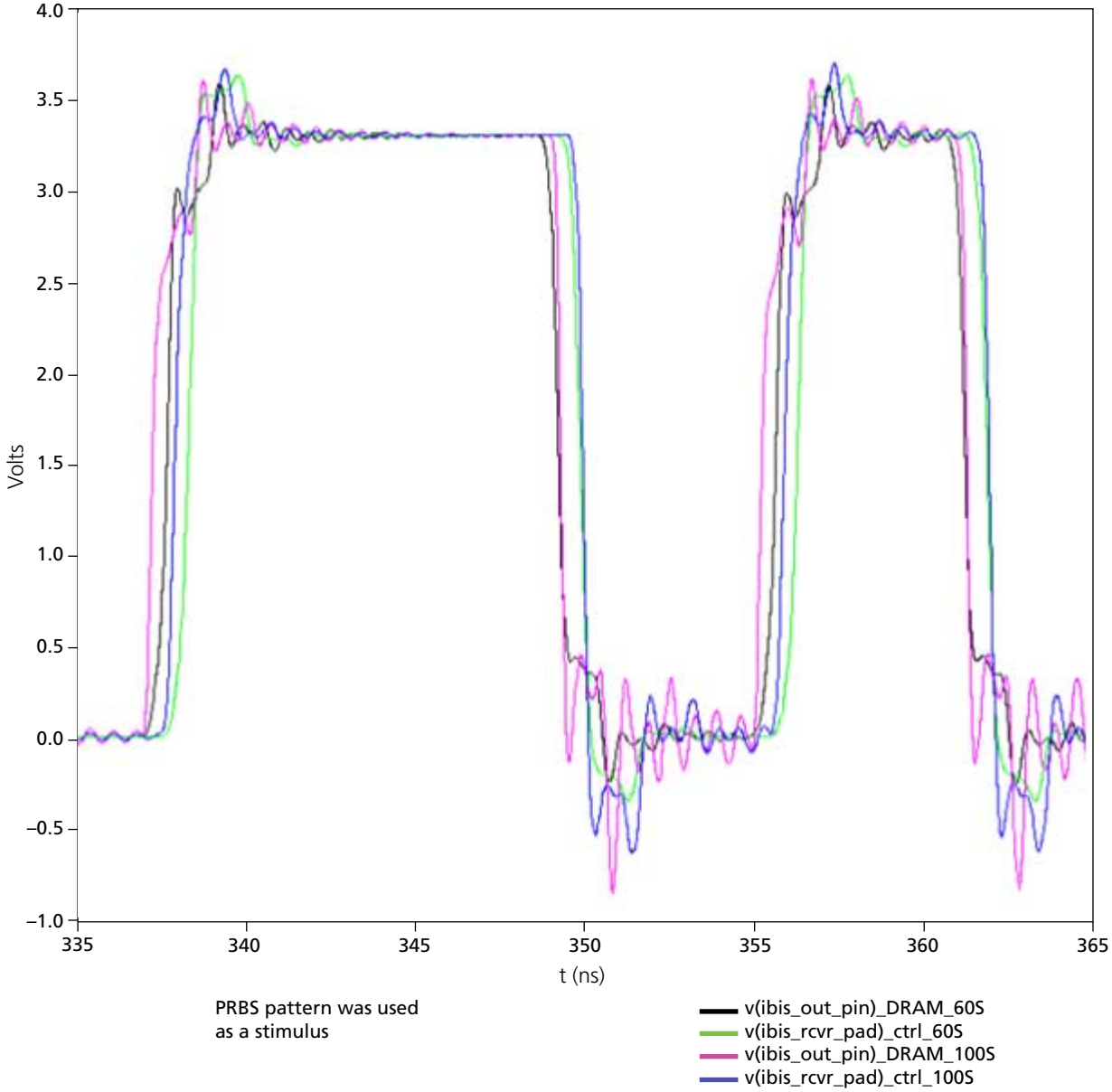
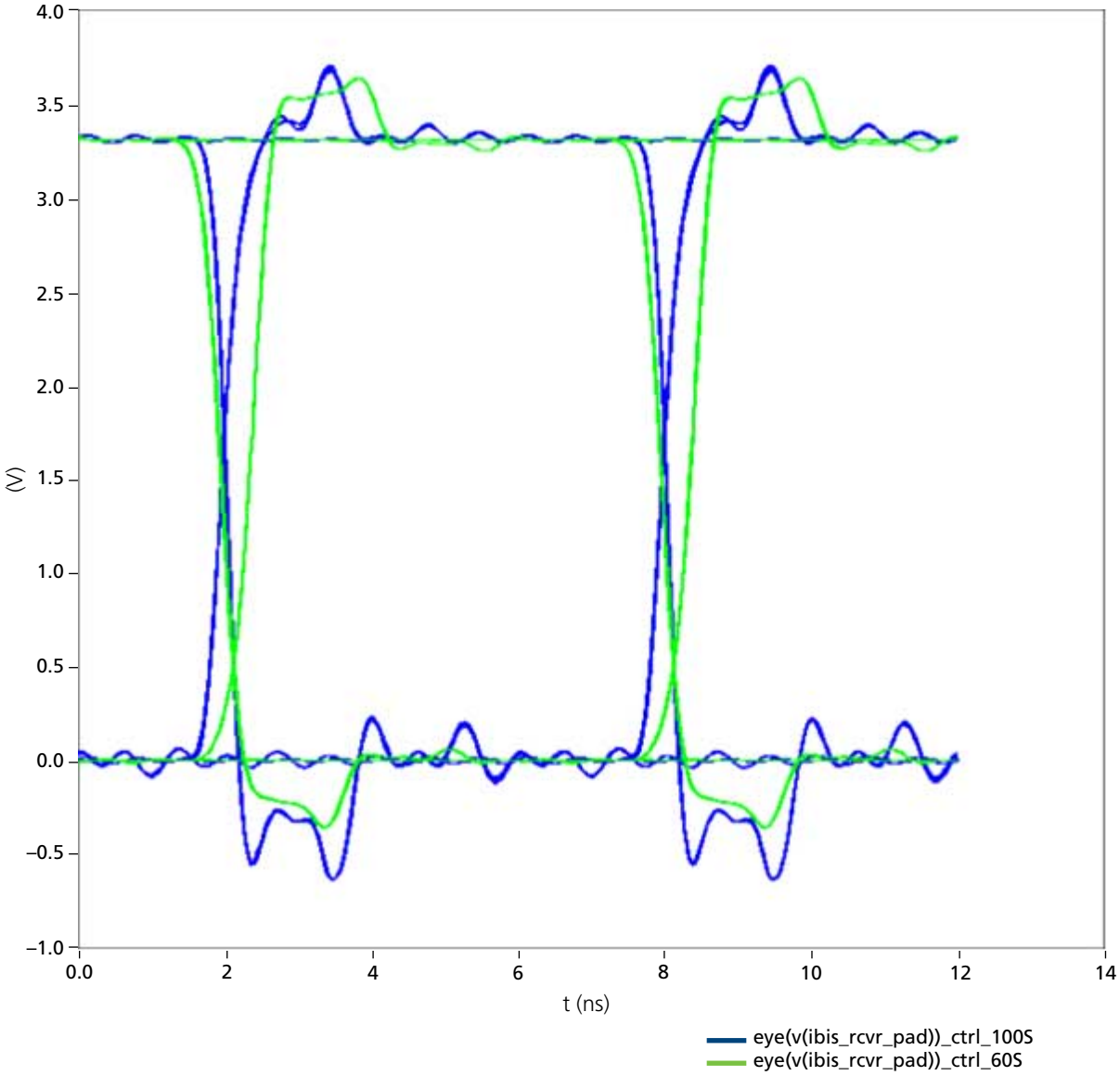


Figure 6: Eye Diagram – 256Mb 54nm/130nm (Y66A/Y16Y)

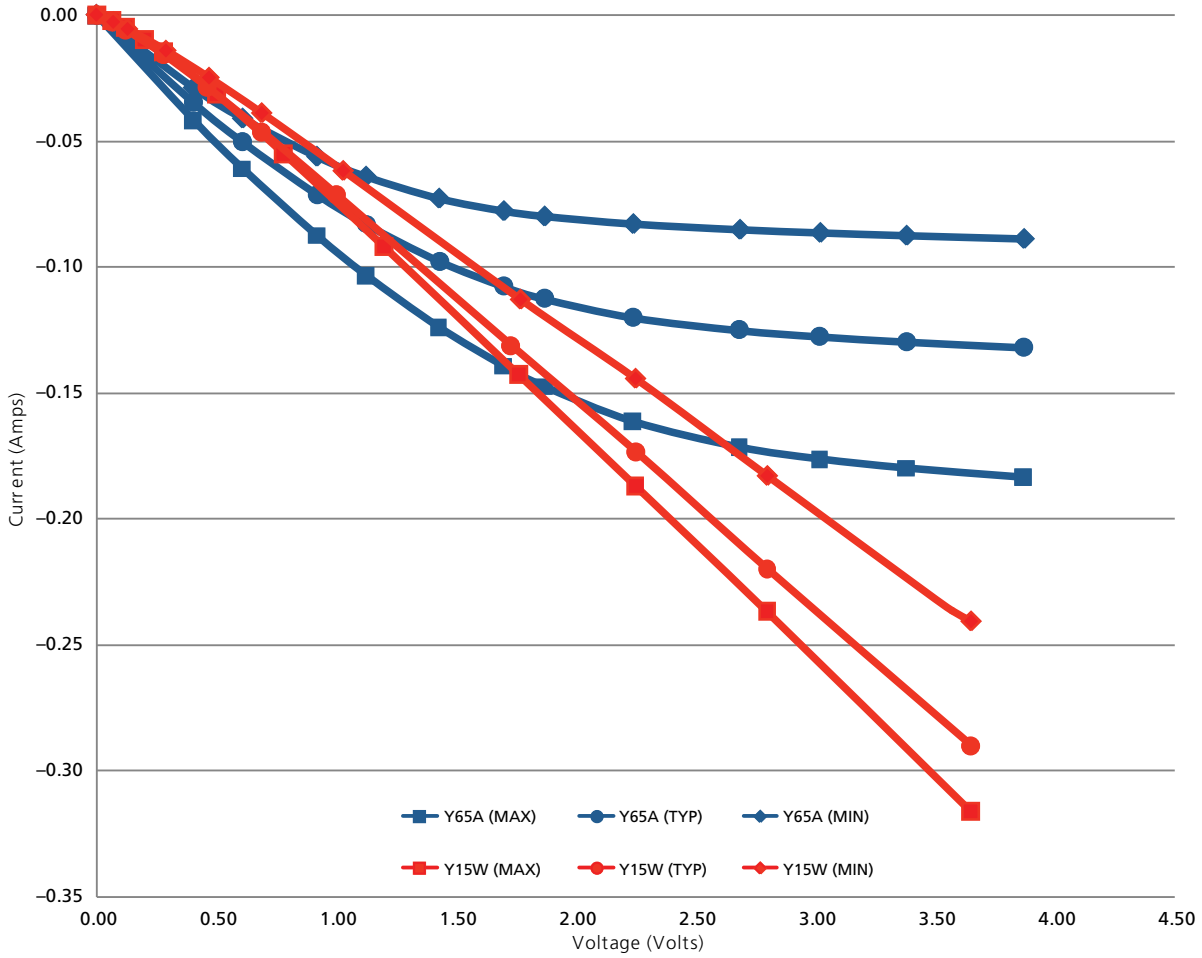


I/O Characteristics Comparison – 128Mb 54nm/130nm (Y65A/Y15W)

Pull-Up/Pull-Down I-V Curves – 128Mb 54nm/130nm (Y65A/Y15W)

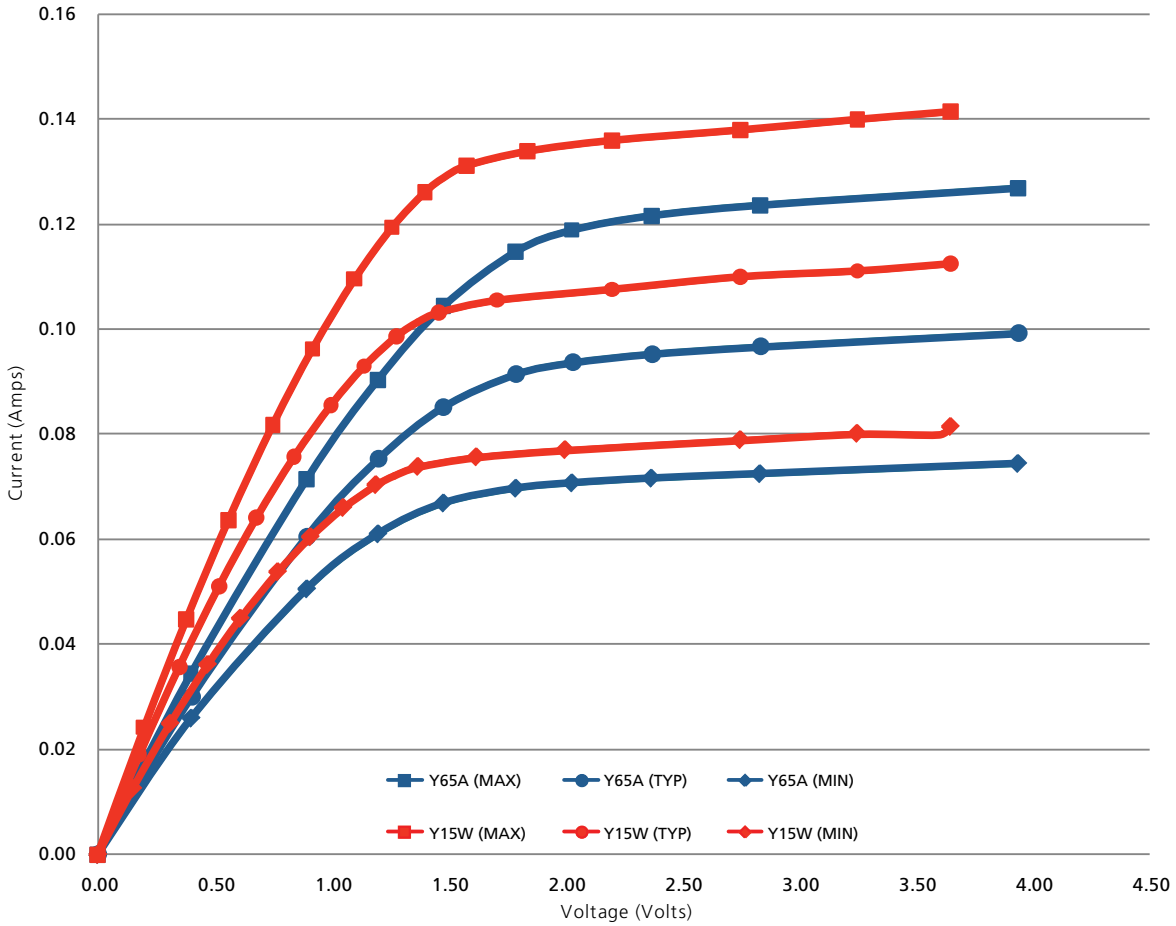
The two figures below show pull-up and pull-down current-versus-voltage curves for the Y65A and Y15W devices.

Figure 7: Pull-Up I-V Curves – 128Mb 54nm/130nm (Y65A/Y15W)



Notes:
1. Blue curves represent fast, typical, and slow corners for the 54nm pull-up I-V curves.
2. Red curves represent fast, typical, and slow corners for the 130nm pull-up I-V curves.

Figure 8: Pull-Down I-V Curves – 128Mb 54nm/130nm (Y65A/Y15W)



Notes:
1. Blue curves represent fast, typical, and slow corners for the 54nm pull-down I-V curves.
2. Red curves represent fast, typical, and slow corners for the 130nm pull-down I-V curves.

Test Procedure – 128Mb 54nm/130nm (Y65A/Y15W)

The following setup and test procedures were used to perform transient and eye diagram simulations:

1. The Y15W device was optimized to work in a test setup with a customer controller.
2. Transient and eye diagram simulations were performed using the Y15W device in the system.
3. The Y15W device was replaced with the Y65A device while the rest of the system remained unchanged.
4. Transient and eye diagram simulations were performed using the Y65A device in the system.
5. Test results for the Y65A and Y15W devices were compared.

Figure 9: Test Setup – 128Mb 54nm/130nm (Y65A/Y15W)

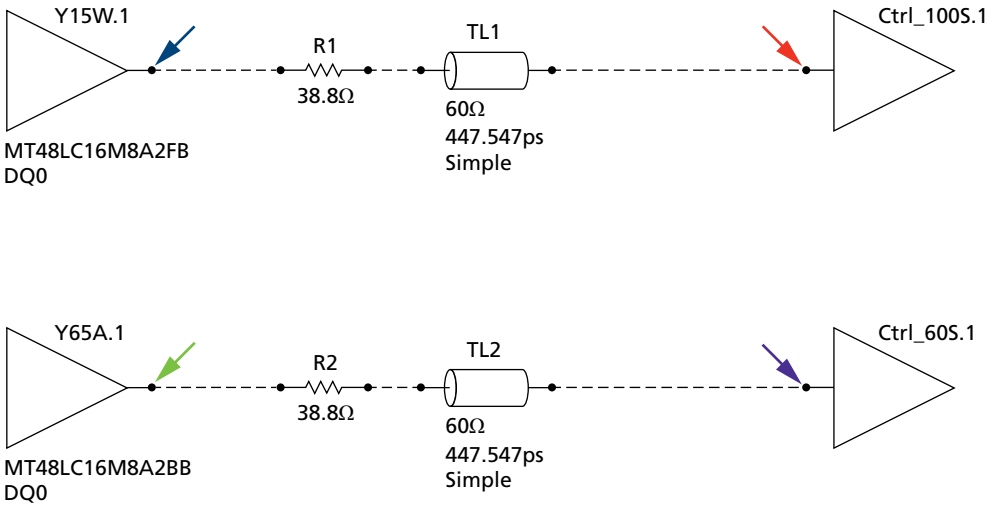


Figure 10: Transient Analysis 1 – 128Mb 54nm/130nm (Y65A/Y15W)

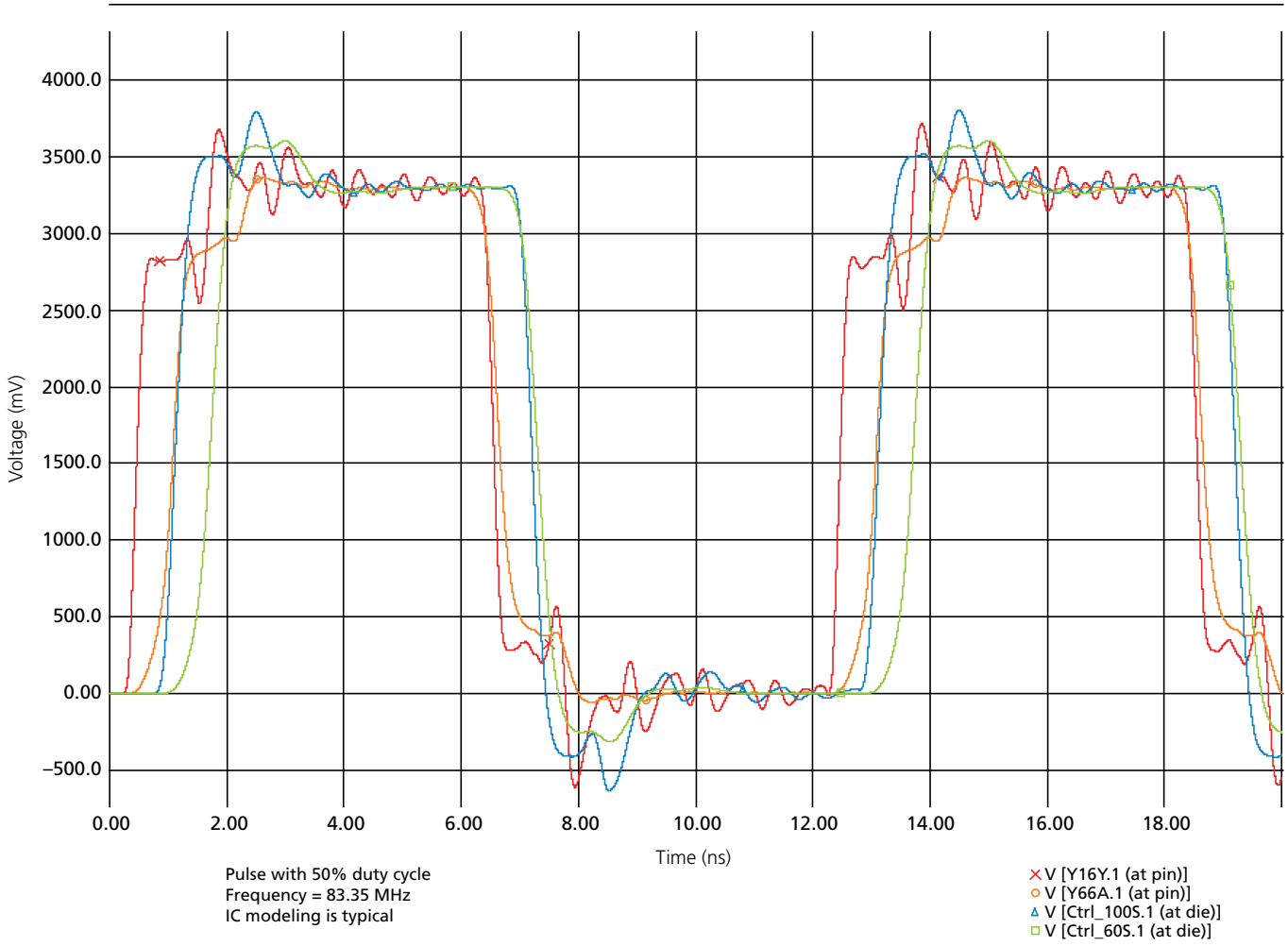


Figure 11: Transient Analysis 2 – 128Mb 54nm/130nm (Y65A/Y15W)

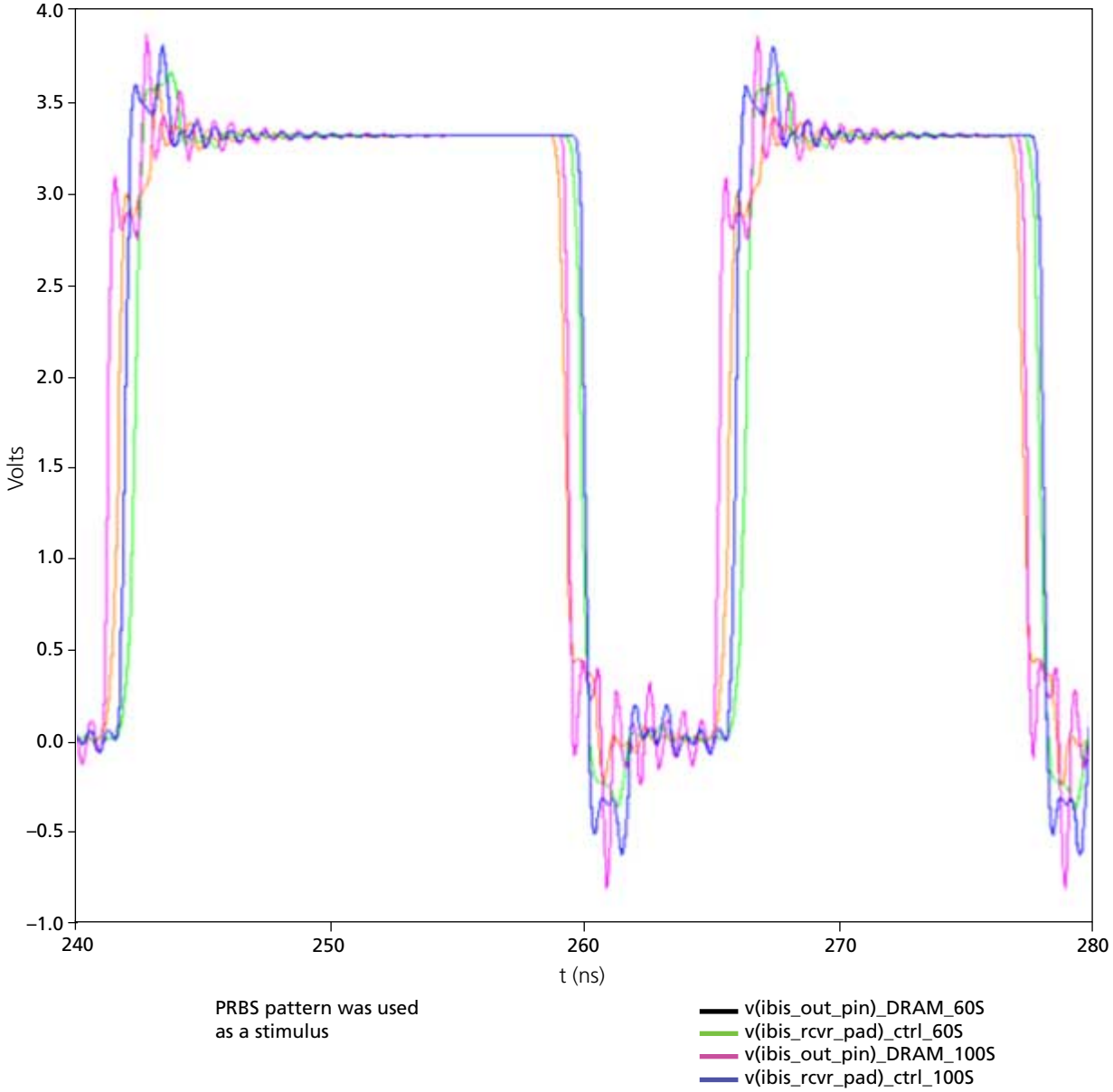
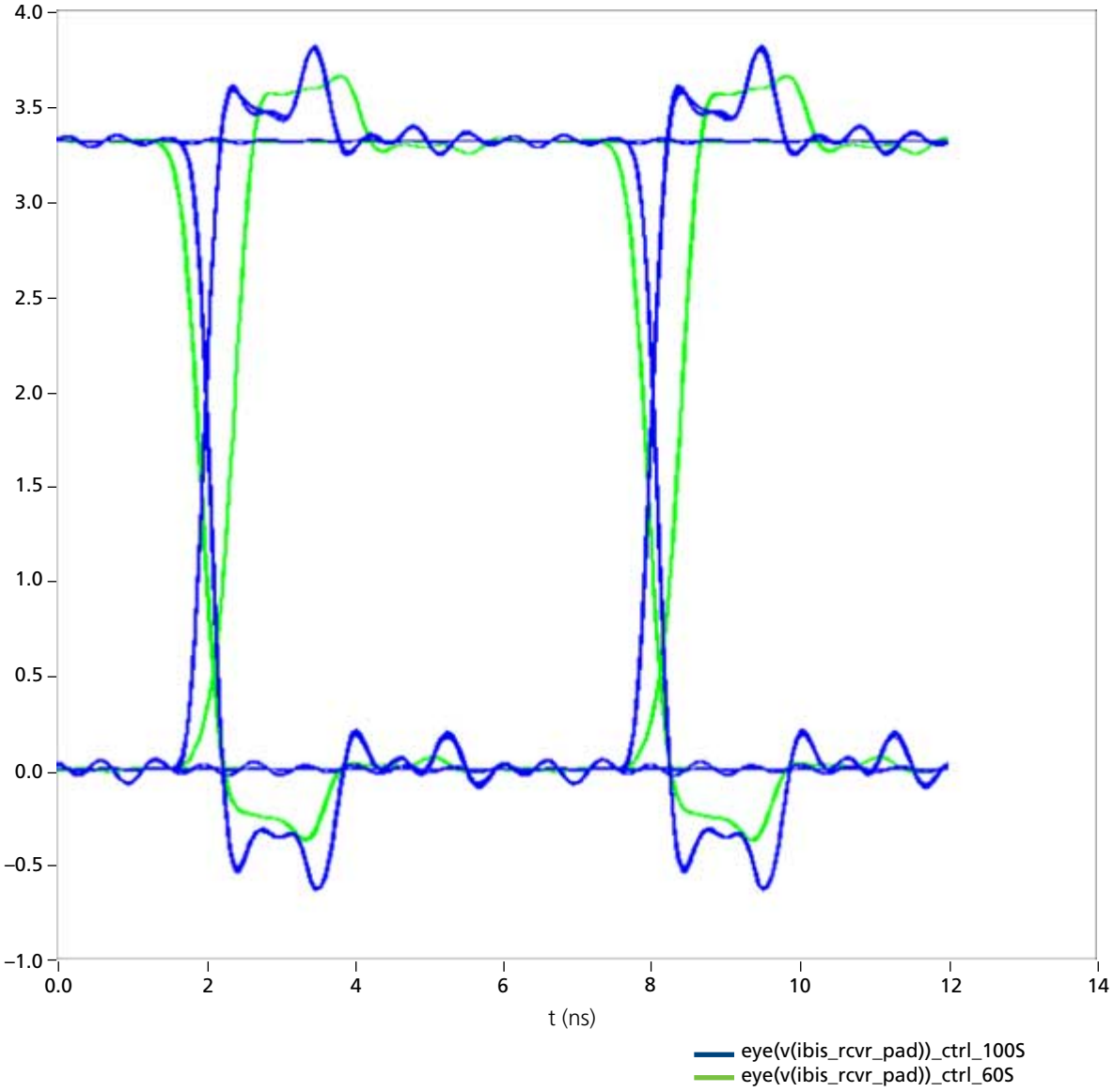


Figure 12: Eye Diagram – 128Mb 54nm/130nm (Y65A/Y15W)

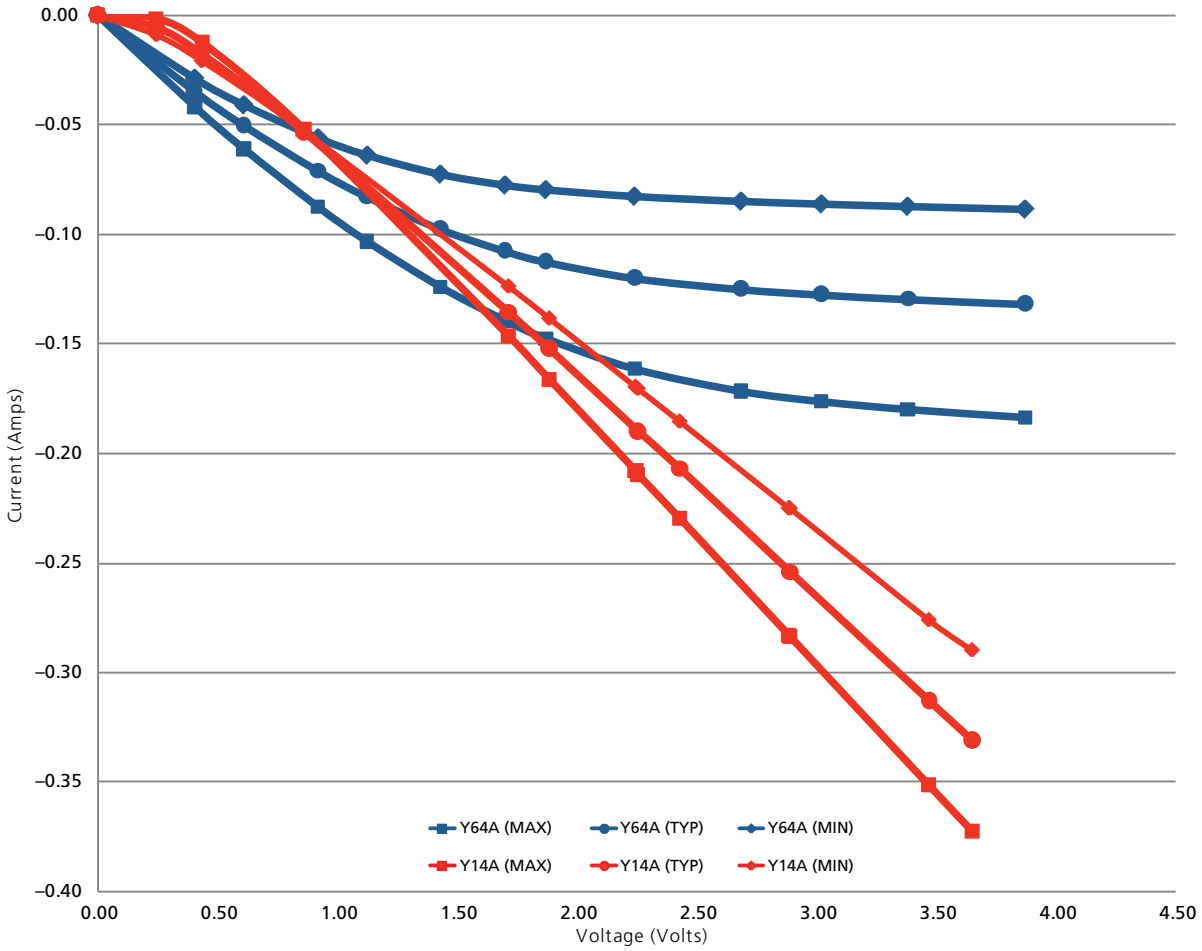


I/O Characteristics Comparison – 64Mb 54nm/130nm (Y64A/Y14W)

Pull-Up/Pull-Down I-V Curves – 64Mb 54nm/130nm (Y64A/Y14W)

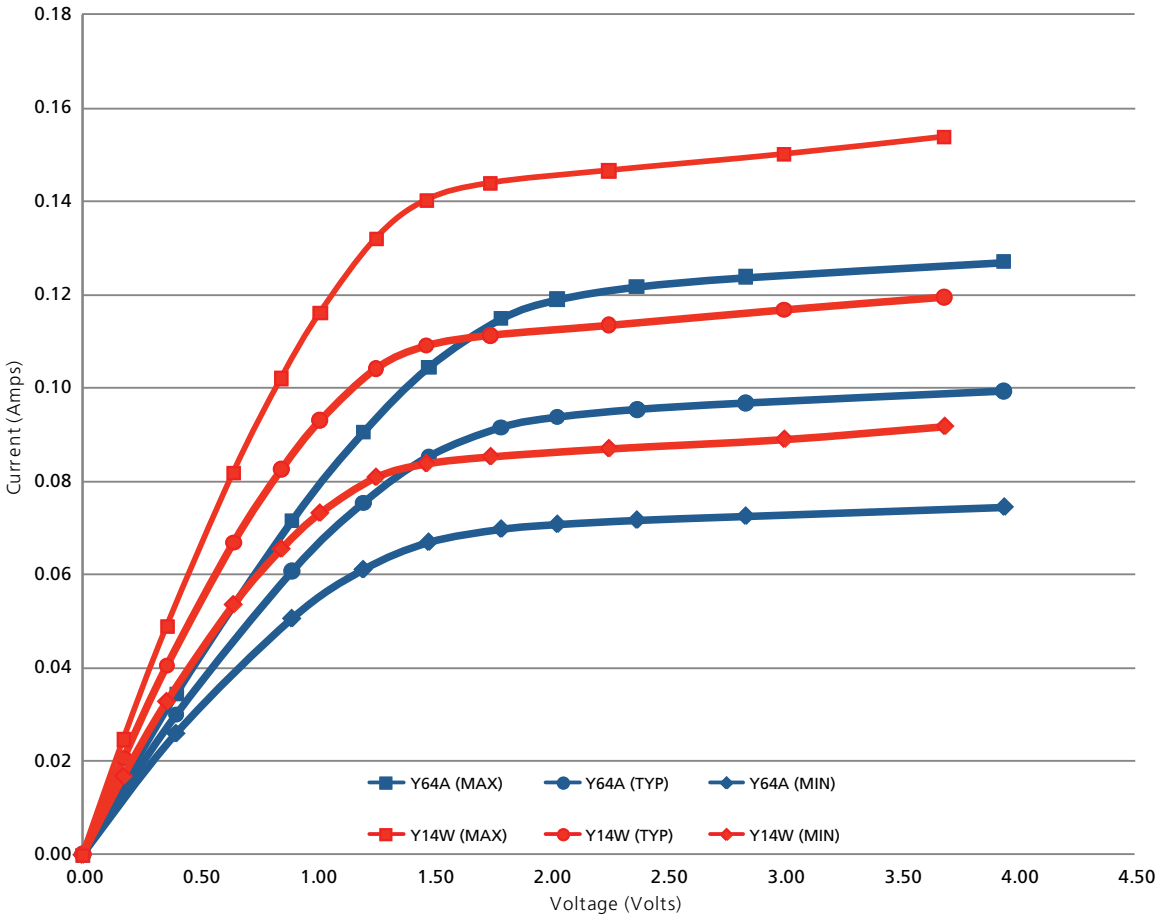
The two figures below show pull-up and pull-down current-versus-voltage curves for the Y64A and Y14W devices.

Figure 13: Pull-Up I-V Curves – 64Mb 54nm/130nm (Y64A/Y14W)



Notes:
1. Blue curves represent fast, typical, and slow corners for the 54nm pull-up I-V curves.
2. Red curves represent fast, typical, and slow corners for the 130nm pull-up I-V curves.

Figure 14: Pull-Down I-V Curves – 64Mb 54nm/130nm (Y64A/Y14W)



Notes:
1. Blue curves represent fast, typical, and slow corners for the 54nm pull-down I-V curves.
2. Red curves represent fast, typical, and slow corners for the 130nm pull-down I-V curves.

Test Procedure – 64Mb 54nm/130nm (Y64A/Y14W)

The following setup and test procedures were used to perform transient and eye diagram simulations:

1. The Y14W device was optimized to work in a test setup with a customer controller.
2. Transient and eye diagram simulations were performed using the Y14W device in the system.
3. The Y14W device was replaced with the Y64A device while the rest of the system remained unchanged.
4. Transient and eye diagram simulations were performed using the Y64A device in the system.
5. Test results for the Y64A and Y14W devices were compared.

Figure 15: Test Setup – 64Mb 54nm/130nm (Y64A/Y14W)

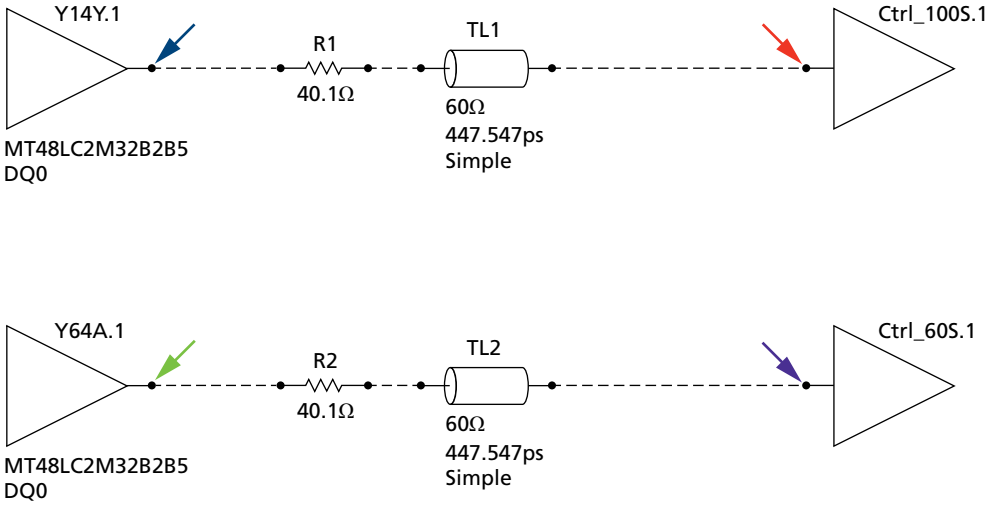


Figure 16: Transient Analysis 1 – 64Mb 54nm/130nm (Y64A/Y14W)

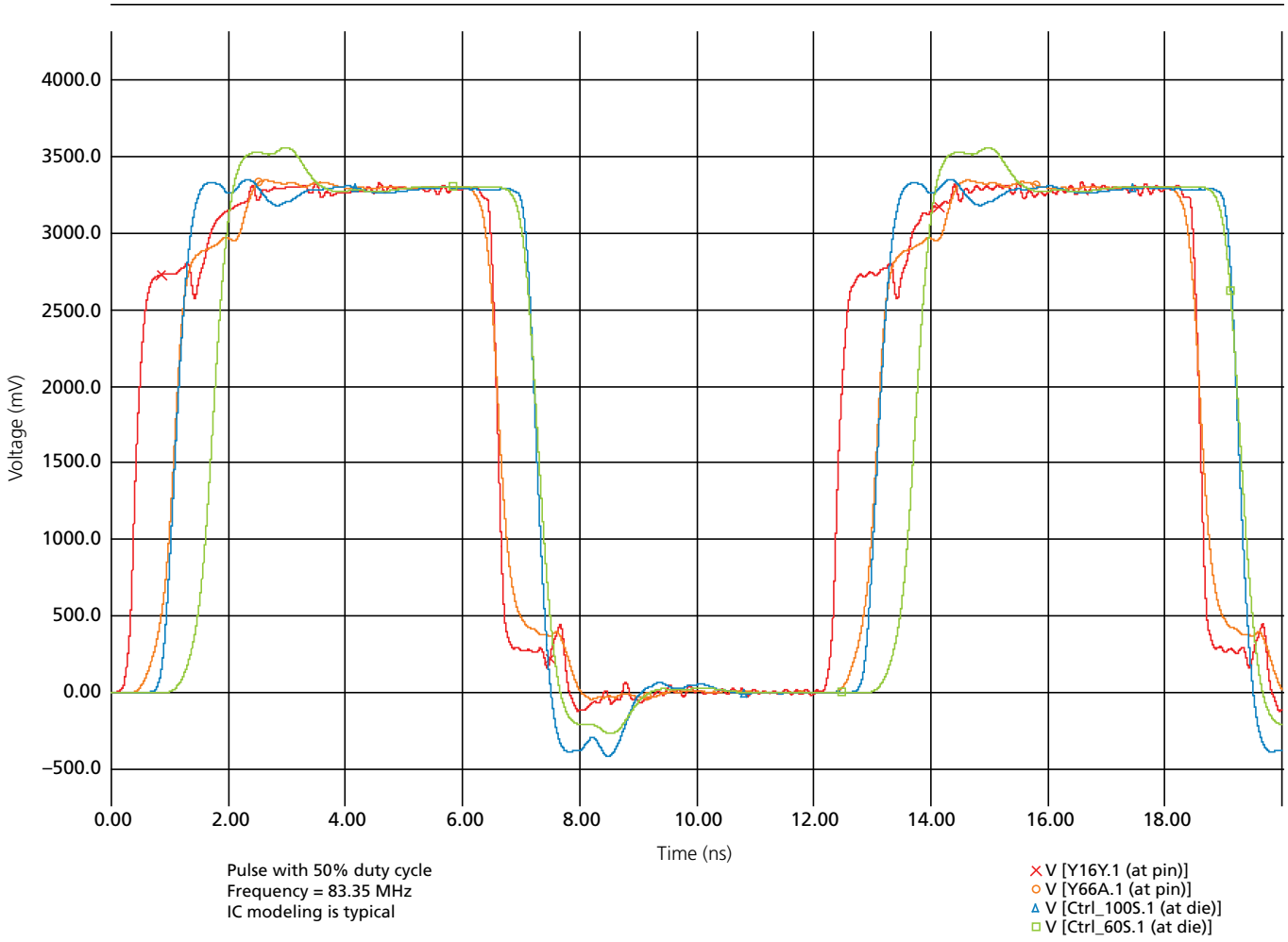


Figure 17: Transient Analysis 2 – 64Mb 54nm/130nm (Y64A/Y14W)

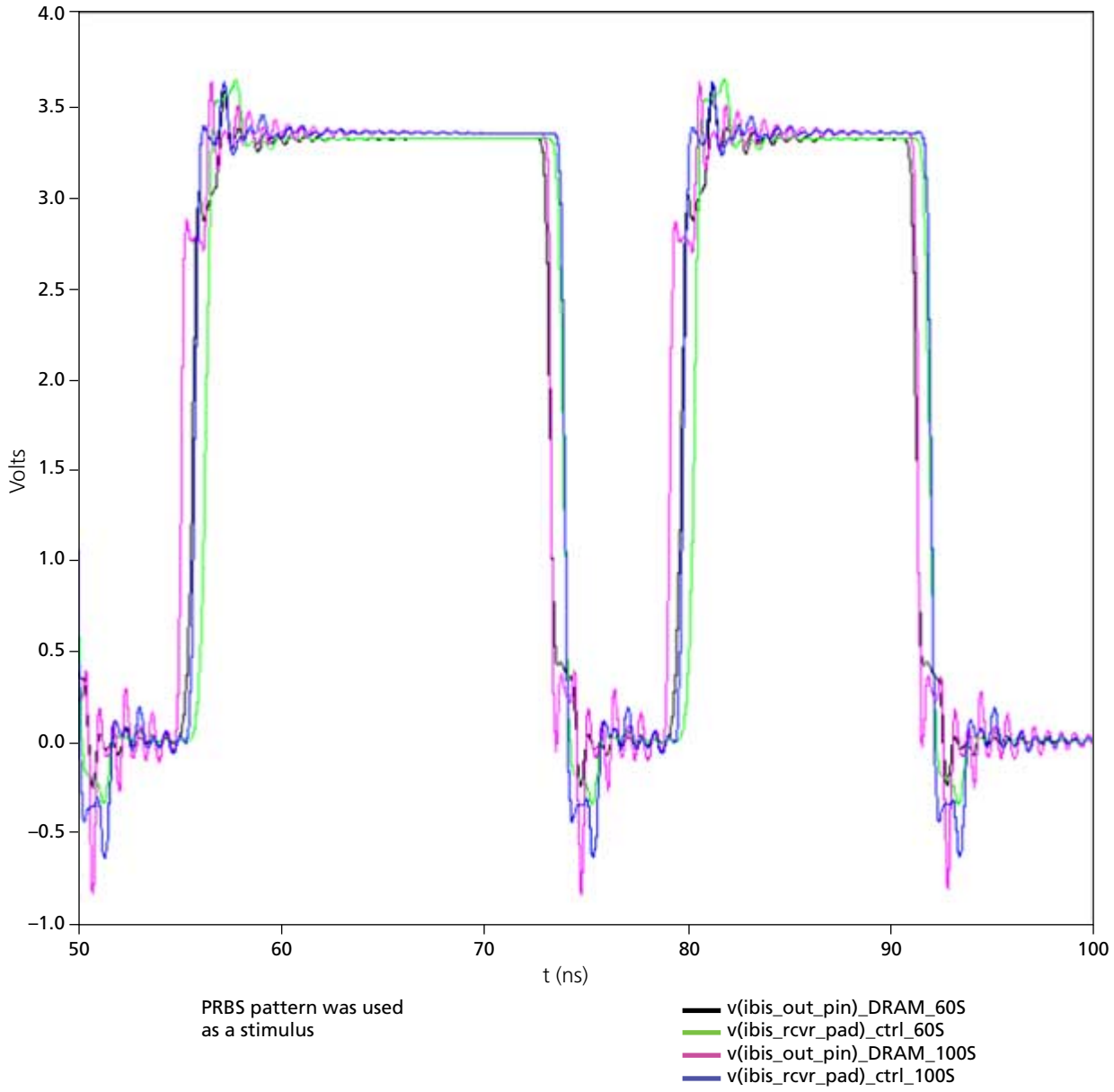
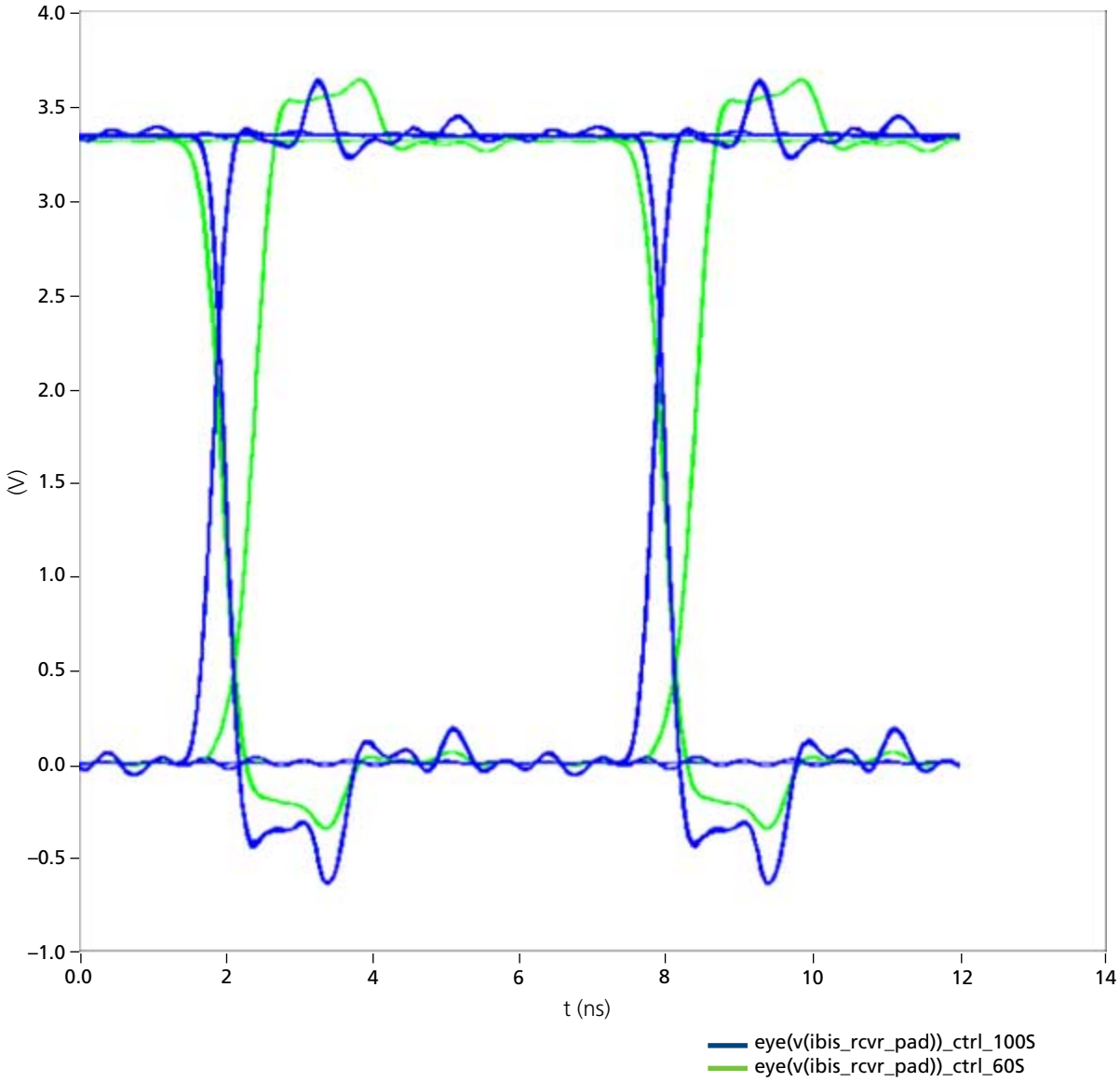


Figure 18: Eye Diagram – 64Mb 54nm/130nm (Y64A/Y14W)



Conclusion

It is important for system designers to understand the difference in I/O characteristics between 130nm and 54nm die. Micron strongly recommends that customers simulate the memory interface of their system in order to ensure that signal integrity will be maintained as 54nm SDRAM are introduced into their systems.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.