TECHNICAL NOTE

Low Power Function of Mobile RAM™
Deep Power Down (DPD)

CAUTION

This document describes Deep Power Down (DPD), one of low power functions that have been adapted to Mobile RAM.
All related operations and numerical values in this technical note are examples for reference only.
For detail characteristic features of DPD, please refer to the corresponding data sheet.

1. Deep Power Down Mode of Mobile RAM

When the device was not accessed (read/write) for a long period, power consumption can be reduced by activating a power down mode. Under the power down mode, all input buffers are turned off except the clock and the clock enable.

2. Overview of Deep Power Down

The deep power down mode can minimize memory power consumption by shutting down the internal power supply generator and suspending refresh operations. However, the data in the memory cell array aren't retained.
Deep power down is especially effective to the DQ bus when Mobile RAM is not being accessed and data retention is not necessary while power is being supplied from the mounted system.

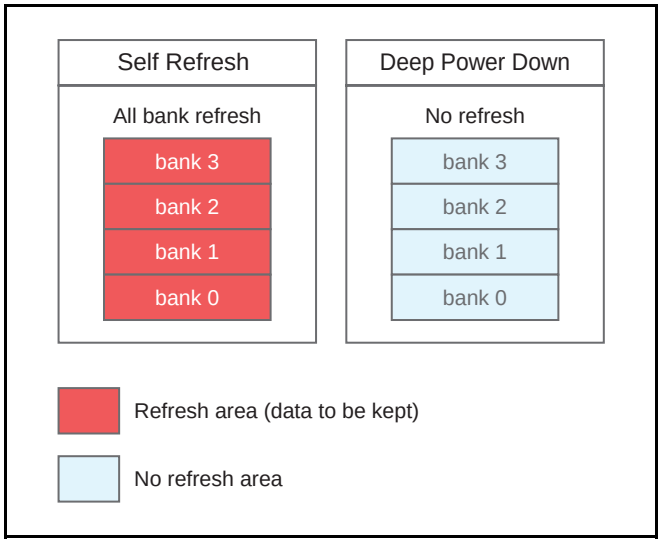

Figure 2-1. Overview of Deep Power Down

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3. Deep Power Down Timing

3.1 Deep Power Down Mode Entry

Executing the deep power down mode entry command (CKE, /CS, /WE = low level, /RAS, /CAS = high level) will enable the device to enter the deep power down mode. Under the deep power down mode, CKE is set at the low level. Before executing the deep power down entry command, all banks must be precharged.

Figure 3-1 shows the entry timing for the deep power down mode.

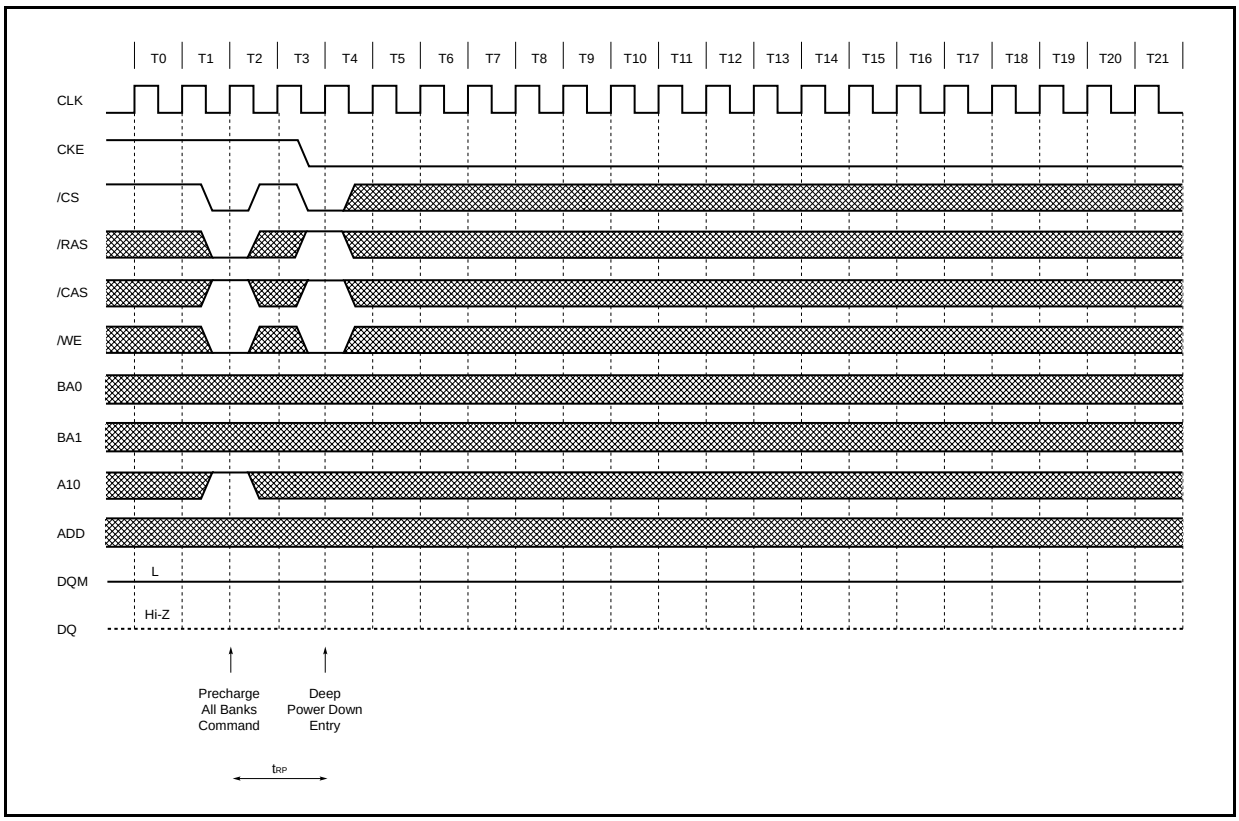

Figure 3-1. Deep Power Down Mode Entry Timing

3.2 Deep Power Down Mode Exit

When CKE reaches the high level under the deep power down mode, the Mobile RAM will exit the deep power down mode. After exiting the deep power down mode, it is necessary for Mobile RAM to perform initialization before resuming normal operations.

Figure 3-2 shows the exit timing for the deep power down mode.

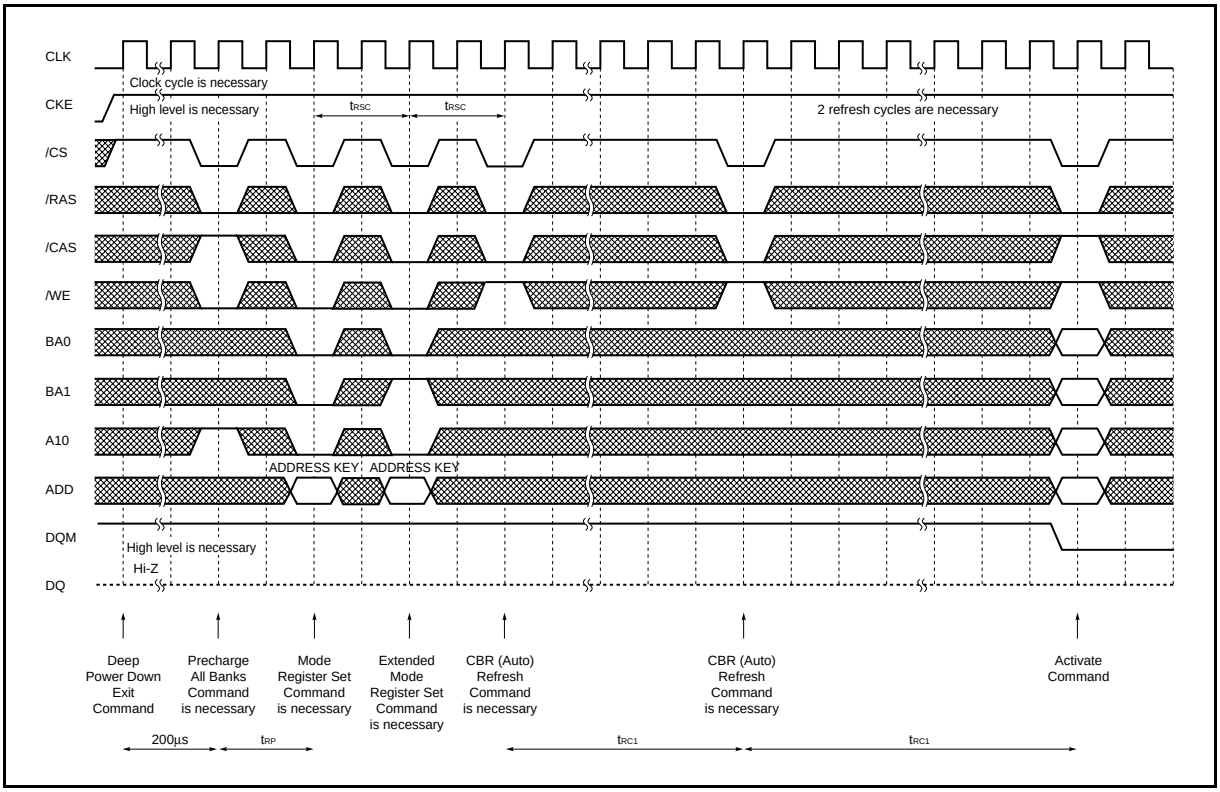

Figure 3-2. Deep Power Down Mode Exit Timing

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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