TECHNICAL NOTE

Low Power Function of Mobile RAM™
Partial Array Self Refresh (PASR)

CAUTION

This document describes Partial Array Self Refresh (PASR), one of low power functions that have been adapted to Mobile RAM.
All related operations and numerical values in this technical note are examples for reference only.
For detail characteristic features of PASR, please refer to the corresponding data sheet.

1. Refresh Operation of DRAM

Each DRAM memory cell consists of one MOS transistor and one capacitor to store one bit (binary data) using an external electronic charge. Because electrical current will leak from the capacitor over time, capacitors must be refreshed periodically to maintain data integrity.
The self-refresh operation, which deactivates the clock to reduce device power consumption, is automatically executed at certain intervals. Self-refresh mode will be effective to maintain data integrity when the DRAM memory cell was not accessed (read/write) for a long period.

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2. Partial Array Self Refresh

2.1 Overview of Partial Array Self Refresh

Partial Array Self Refresh (PASR) is the specific mode that Mobile RAM commonly consists of four banks as the full memory cell arrays. Refresh operations are not performed across the full memory cell arrays but only to specific banks where data retention is required, such as one or two banks. Data storaged outside the defined refresh area will not to be retained. This PASR can help to reduce the self-refresh current to achieve lower power consumption function.

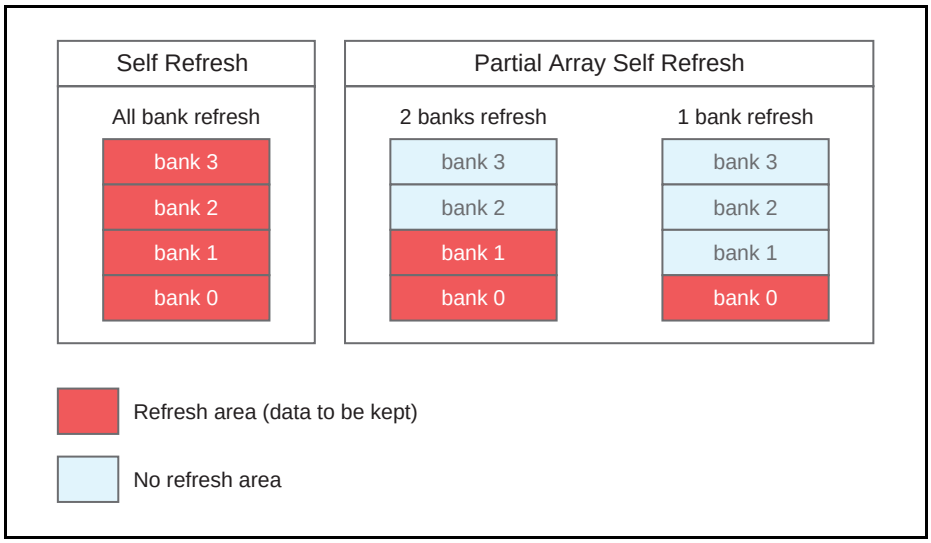


Figure 2-1. Overview of Partial Array Self Refresh

2.2 Advantages of Partial Array Self Refresh

Table 2-1 shows self-refresh current (IDD6) of Mobile RAM with partial array self refresh mode.

Table 2-1. Comparison of Self-Refresh Current (examples)

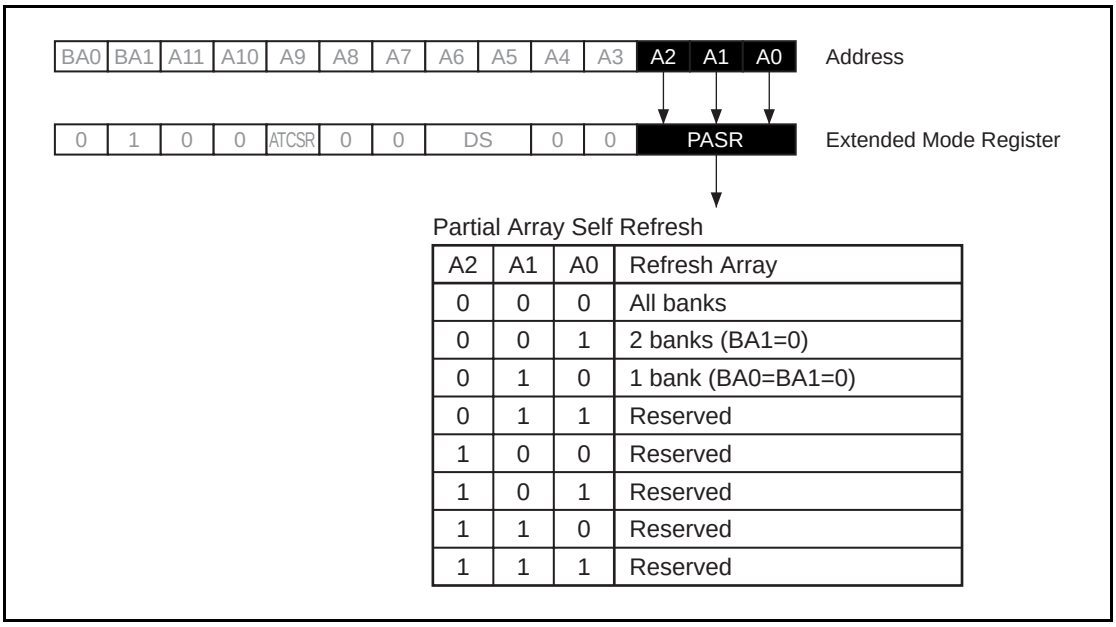
Density	IDD6 (max.) All banks	IDD6 (max.) 2 banks	IDD6 (max.) 1 bank
64Mb	250μA	180μA	140μA
128Mb	200μA	170μA	150μA
256Mb	400μA	300μA	250μA

3. Partial Array Self Refresh Settings

The specific memory bank to be refreshed can be set by Extended Mode Registers Set (EMRS).

Three bits (A0 to A2) of EMRS are used to define the refresh area.

Once the refresh area is set, the setting is retained until another setting is entered or the power is turned off.



A2	A1	A0	Refresh Array
0	0	0	All banks
0	0	1	2 banks (BA1=0)
0	1	0	1 bank (BA0=BA1=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Figure 3-1. Partial Array Self Refresh Settings Using Extended Mode Register Set

4. Partial Array Self Refresh Timing

The entry/exit timing of the partial array self refresh is the same as the self-refresh timing of conventional DRAM. Figure 4-1 shows the entry/exit timing for self-refresh.

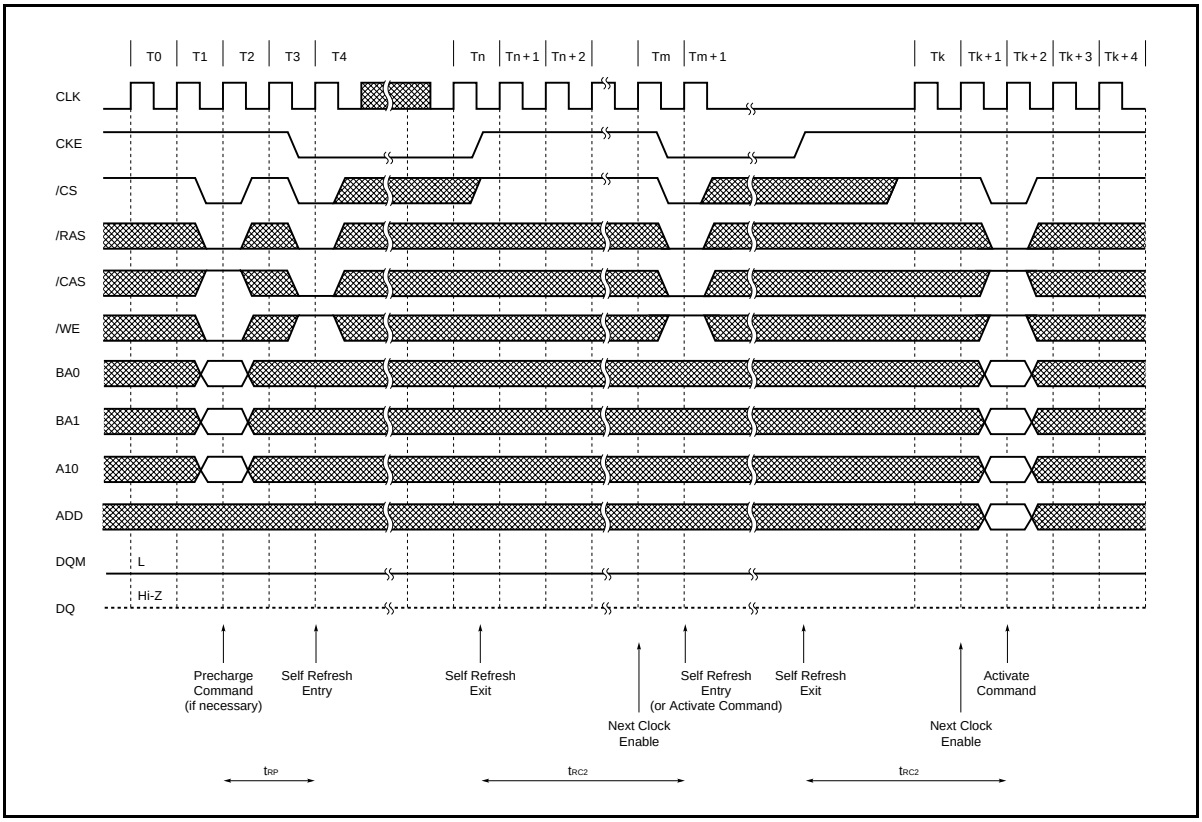


Figure 4-1. Self-Refresh Entry/Exit Timing

Mobile RAM is a trademark of Elpida Memory, Inc.

The information in this document is current as November, 2005. The information is subject to change without notice.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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