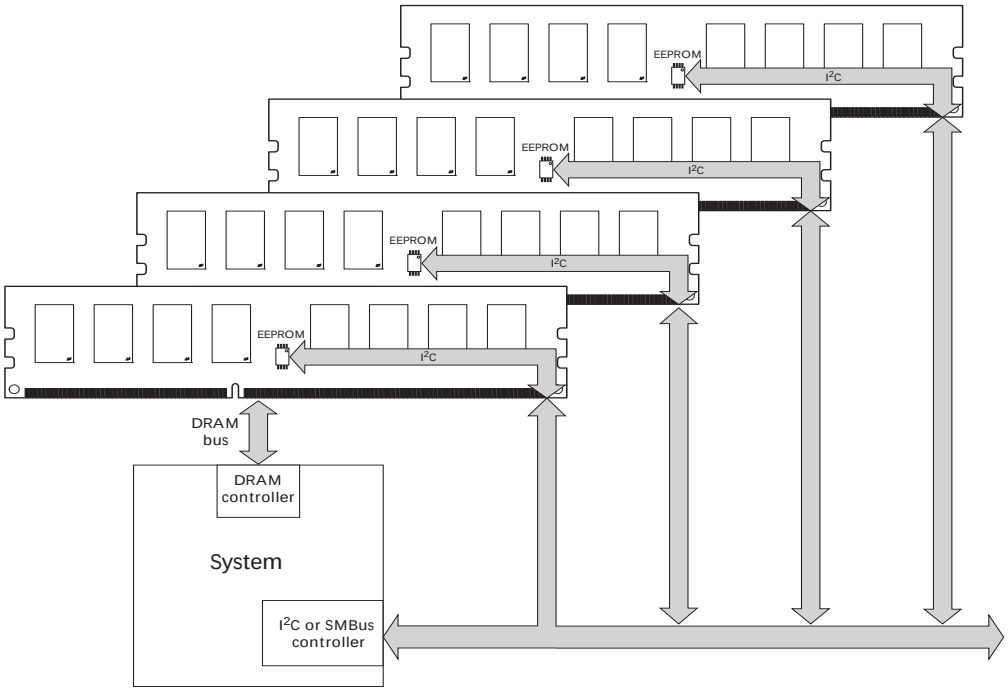
Technical Note

Memory Module Serial Presence-Detect

Introduction

This technical note describes how SPD is essential in helping to standardize the configuration, timing, and manufacturing information of any given memory module. SPD information is written to a single EEPROM that resides on the DIMM. The pins of the EEPROM are routed to the edge connector of the module so that it may be accessed by the system through the I^2C or SMBus. In this manner, the DIMM's configuration information stays with the module and is accessible by the system the module is installed in.

Figure 1: I^2C Bus Interface



JEDEC Standards

SPD has two basic parts: the hardware, which consists of the EEPROM and the I^2C bus on which it resides and the module configuration information that is stored on the EEPROM. JEDEC has defined both the hardware and the data and has documented it in seperate sections of JEDEC Standard JESD21-C.

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EEPROM

JEDEC Standard JESD21-C also contains two sections that define the EEPROMs used on memory modules. Section 4.1.3, "Definition of the EE1002 and EE1002A Serial-Presence Detect (SPD) EEPROMs" defines the 256-byte EEPROMs. Section 4.1 "Definition of the TSE2002av, Serial Presence-Detect with Temperature Sensor" defines the temperature sensor/EEPROM combination devices (pending JEDEC approval at the time of publication).

Combination devices consist of two I^2C devices, a temperature sensor, and an EEPROM in one 8-pin package. Combination devices were implemented into Micron's product line starting with 72-bit-wide DDR3 modules. Standard EEPROM devices are also in 8-pin packages and have been in use on SDRAM, DDR, DDR2, and 64-bit DDR3 modules.

Serial Presence-Detect

JEDEC has created a General Standard Serial Presence-Detect Standard (section 4.1.2) that is contained in JEDEC Standard JESD21-C. In addition to the general standard, appendices specific to different technologies have been created to provide for that technology. These appendices define the format and the configuration information of any given module and make up the SPD data that is stored within the EEPROM on every module. Micron uses the appendices listed below to automatically generate SPD data for every module manufactured. These appendices are available at www.jedec.org.

- Serial Presence-Detect Standard, General Standard – 4.1.2
- Appendix E: SDRAM Modules – 4.1.2.5
- Appendix D: DDR Modules – 4.1.2.4
- Appendix J: DDR2 Modules – 4.1.2.10
- Appendix X: Fully Buffered Modules – 4.1.2.7
- DDR3 Modules – 4.1.2 (pending JEDEC approval at the time of publication)

EEPROM

All SPD EEPROMs used on Micron memory modules are 256 bytes in size and are manufactured by qualified vendors. This technical note highlights the main features of the EEPROM, but is not intended to be a complete reference. The EEPROM in combination devices operates identical to the standard EEPROMs, except where noted. Refer to the JEDEC specifications for complete details.

EEPROM Function

The module edge-connector pins used to operate the EEPROM consist of the following:

- Serial clock (SCL)
- Serial data (SDA)
- Write protect (WP)
- Address inputs (SA[2:0])

Serial Clock (SCL)

This input is used to clock all data into the device on the positive edge of the clock and out of the device on the negative edge.

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Serial Data (SDA)

This bidirectional signal is used to transfer data into and out of the device. It is an open drain output and may be wired as logic "OR" with any number of other SDA pins.

Write Protect (WP)

This input signal is used for protecting the entire contents of the EEPROM from inadvertent WRITE operations. WP is used to enable (when LOW) or disable (when HIGH) write instructions to the entire memory area or to the protection register. This pin is tied HIGH on Micron memory modules, except where noted otherwise, permanently disabling write protection functionality.

Address Inputs (SA[0:2])

These input signals are used to set the physical address of the EEPROMs on the I^2C bus. By hardwiring these pins to Vss or Vdd through the module edge connector, up to eight unique addresses can be achieved.

Many SDR, DDR, and DDR2 modules have SA2 hardwired to Vss on the module PCB. This is due to the fact that most systems that utilize these memory technologies cannot support more than four modules.

Table 1: EEPROM Pin Description

Pin	Symbol	Type	Description
1	SA0	Input	Address inputs
2	SA1	Input	Address inputs
3	SA2	Input	Address inputs
4	Vssspd	Supply	Power
5	SDA	I/O	Serial data
6	SCL	Input	Serial clock
7	WP	Input	Write protect
7[1]	Event#	Output (open drain)	Teperature event
8	VDDSPD	Supply	Ground

Notes: 1. Only applies to combination temperature sensor/EEPROM devices used with some modules, beginning with modules.

Device Operation

For memory modules, the I²C bus specification/protocol developed by Philips® is used as the communication protocol between the system and the SPD EEPROM. This two-wire protocol is designed to minimize the EEPROM pin count to an 8-pin footprint and to simplify the module printed circuit board (PCB) layout. In many mainstream computers, the SPD EEPROM is connected to the system's SMBus. SMBus is a subset of the I^2C bus/protocol and was developed by Intel®.

Each module's SPD EEPROM behaves as a slave device in the I²C bus protocol (as seen in Figure 2 on page 4), with all SPD memory operations synchronized by the serial clock. All communications must be initiated by the bus master; in most cases, this is the I^2C or SMBus controller.

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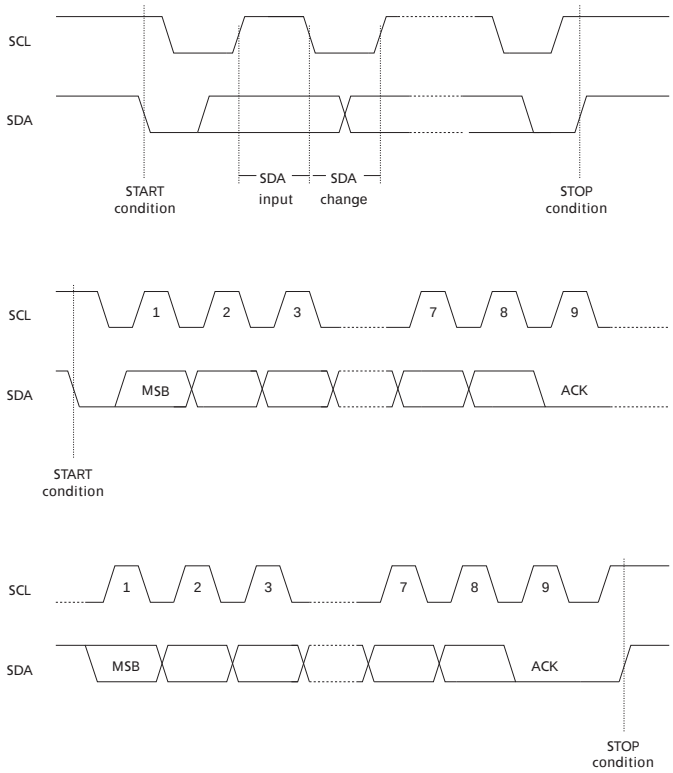
Figure 2: I^2C Bus Protocol



Clock and Data Conventions

Data states on the SDA line can only change during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating stop and start conditions.

Start/Stop Conditions

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The SPD continuously monitors the SDA and SCL lines for start conditions and will not respond to any command until this condition is met.

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the SPD to place the device in standby power-down mode.

Acknowledge

Acknowledge (Ack) is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the 8 bits of data.

The SPD will always respond with an Ack after recognition of a start condition and its slave address. If both the device and WRITE operation are selected, the SPD will respond with an Ack after the receipt of each subsequent 8-bit word.

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Data Input

During data input, the device samples serial data (SDA) on the rising edge of the serial clock (SCL). To ensure proper operation of the device, SDA must be stable during the rising edge of SCL, and the SDA signal must change only when SCL is driven LOW.

Table 2: Device Select Codes

Memory Area Function	Device Type Identifier				Chip Enable			R/W
	b7[1]	b6	b5	b4	b3	b2	b1	b0
READ/WRITE SPD memory	1	0	1	0	SA2	SA1	SA0	R/W#
SET WRITE PROTECTION (SWP)	0	1	1	0	0	0	1	0
CLEAR WRITE PROTECTION (CWP)					0	1	1	0
PERMANENTLY SET WRITE PROTECTION (PSWP)[2]					SA2	SA1	SA0	0
READ SWP					0	0	1	1
READ PSWP[2]					SA2	SA1	SA0	1
READ/WRITE temperature registers[3]	0	0	1	1	SA2	SA1	SA0	R/W#

Notes:
1. The most significant bit is sent first.
2. SA0, SA1, and SA2 are compared against the respective external pins on the EEPROM.
3. Only applies to combination temperature sensor/EEPROM devices used with some modules, beginning with DDR3.

Device Select Codes

Device select codes are 8-bit seqences that can be sent on the SDA line to initiate specific functions and access registers within the SPD EEPROM. As specified by the I²C memory standard, each SPD contains built-in 4-bit device type identifiers. These 4-bit identifiers are used to address the following functions:

- EEPROM memory array (1010)
- Write protect settings (0110)
- Temperature sensor (0011)

These codes are used together with one of three addressing methods to select a specific memory module's SPD EEPROM attached to the I²C bus. For more information, refer to Table 2 on page 5.

Write Protection

Software write protect, once enabled, protects only the first half of the EEPROM memory array, bytes 0–127 (0x00–0x7F), from inadvertant writes. This leaves the user-programmable area of the EEPROM, bytes 128–255 (0x80–0xFF), permanently unprotected. Software write protect features do not apply to this half of the EEPROM's memory array.

Hardware Write Protection

The WP pin, if pulled LOW, would protect the entire array; however, to facilitate flexibility in production, Micron modules have pin WP tied to Vdd on the module PCB. This permanently disables the hardware write protect feature leaving the software write protection features available to be utilized by customers as they see fit.

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Some Micron modules use a seperate EEPROM and temperature sensor configuration. These modules have WP connected to Vss through a pull-down resistor enabling the EVENT# pin on the temperature sensor and the WP pin on the EEPROM to share a module edge connection.

The WP pin on temperature sensor/EEPROM combination devices is not an external connection. It is tied HIGH internal to the device. On combination devices, the EVENT# pin is located where the external WP pin would be on a standard EEPROM.

Permanent Software Protection

Permanent software write protection is enabled by sending a PERMANENTLY SET WRITE PROTECTION (PSWP) instruction to device address 0110. This feature enables the lower half of the array (bytes 0–127) to be permanently write protected. The EEPROM will no longer acknowledge the 0110 control byte after the write protect register has been programmed. Permanent software write protection cannot be reversed by powering down the device or attempting to drive WP to Vdd.

Reversible Software Write Protection

Reversible software write protection is enabled by sending a SET WRITE PROTECTION (SWP) instruction to device address 0110. This feature enables the lower half of the array (bytes 0–127) to be write protected temporarily. To reverse temporary write protection, a clear write protection (CWP) instruction must be sent to the same device address.

When Micron modules leave Micron's production facilities, the modules have had neither a PSWP nor an SWP instruction exectuted.

SPD EEPROM Addressing and System Design

The SPD addressing can be incorporated into a system design in three ways:

- Common clock/common data
- Common clock/separate data
- Common data/separate clock

Designers will find that for systems using eight or fewer DIMM devices, implementing a common clock/common data configuration will be to their advantage. For systems requiring more than eight DIMM devices, the common clock/separate data and common data/separate clock configurations are illustrated. Although these are viable solutions, they require a significant increase in overhead.

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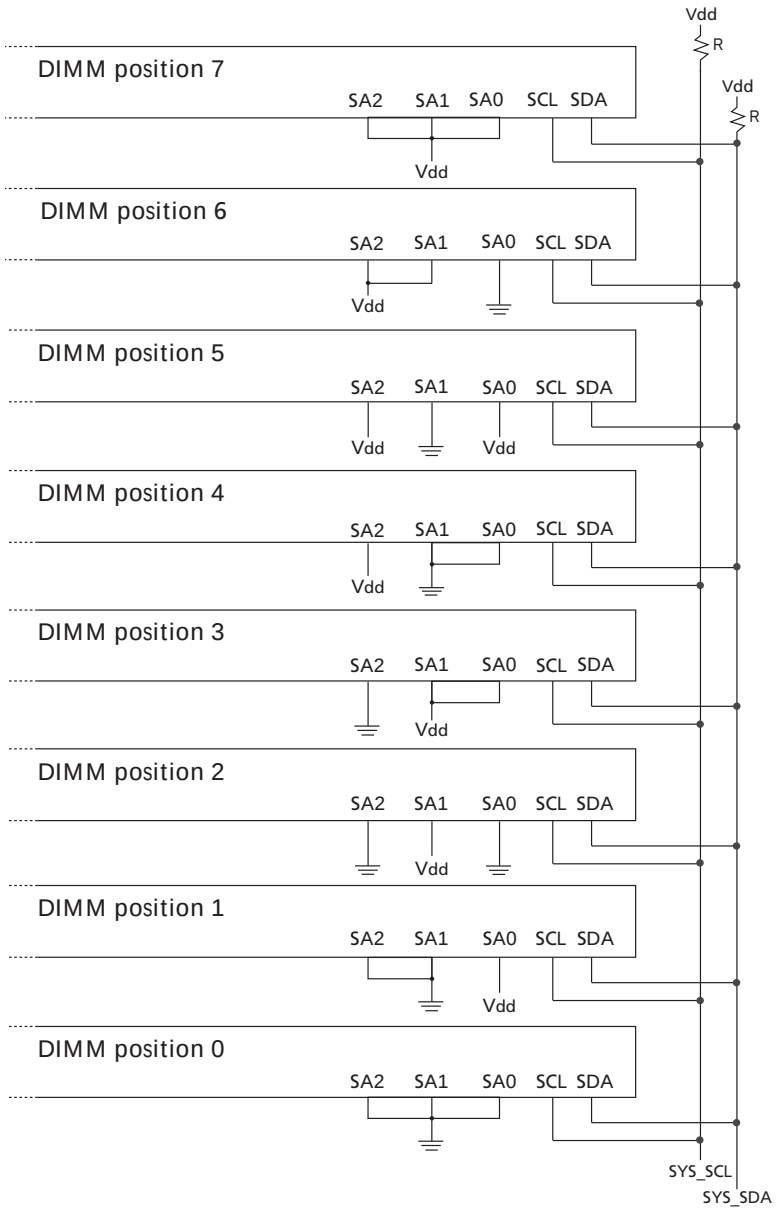
Common Clock/Common Data

The common clock/common data configuration is likely the most common implementation. SA0–SA2 are wired in a binary sequence at each DIMM socket for a maximum of eight modules, as shown in Figure 3. All eight modules share a common clock and common data line. Pull-up resistors (4.7K typical) are required on all SCL and SDA signals because of their open drain interface.

Figure 3: SPD Block Diagram for Common Clock/Common Data



Notes: 1. SODIMM modules have SA2 hardwired to Vss on the module PCB. This is because most systems that use these memory technologies cannot support more than four modules.

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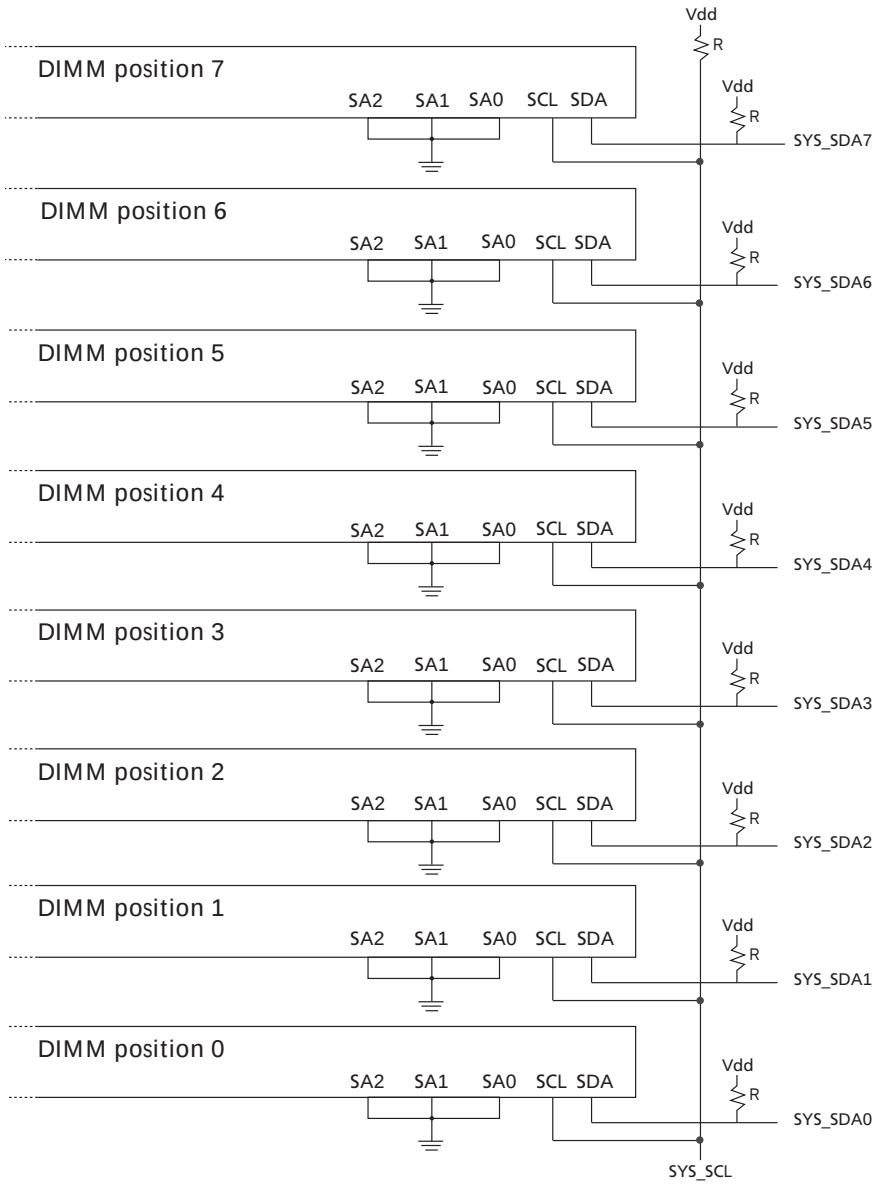
Common Clock/Separate Data

In the common clock/separate data configuration, SA0–SA2 are wired to the same address at each DIMM socket (typically all to Vss), as shown in Figure 4. The SCL is wired to all positions. The SDA is unique for each position, enabling more than 8 positions, but not permitting CMAX to exceed 400pf. Because the data pins are separate, 8 positions could provide parallel data paths of one byte (8x speed improvement).

Figure 4: SPD Block Diagram for Common Clock/Separate Data



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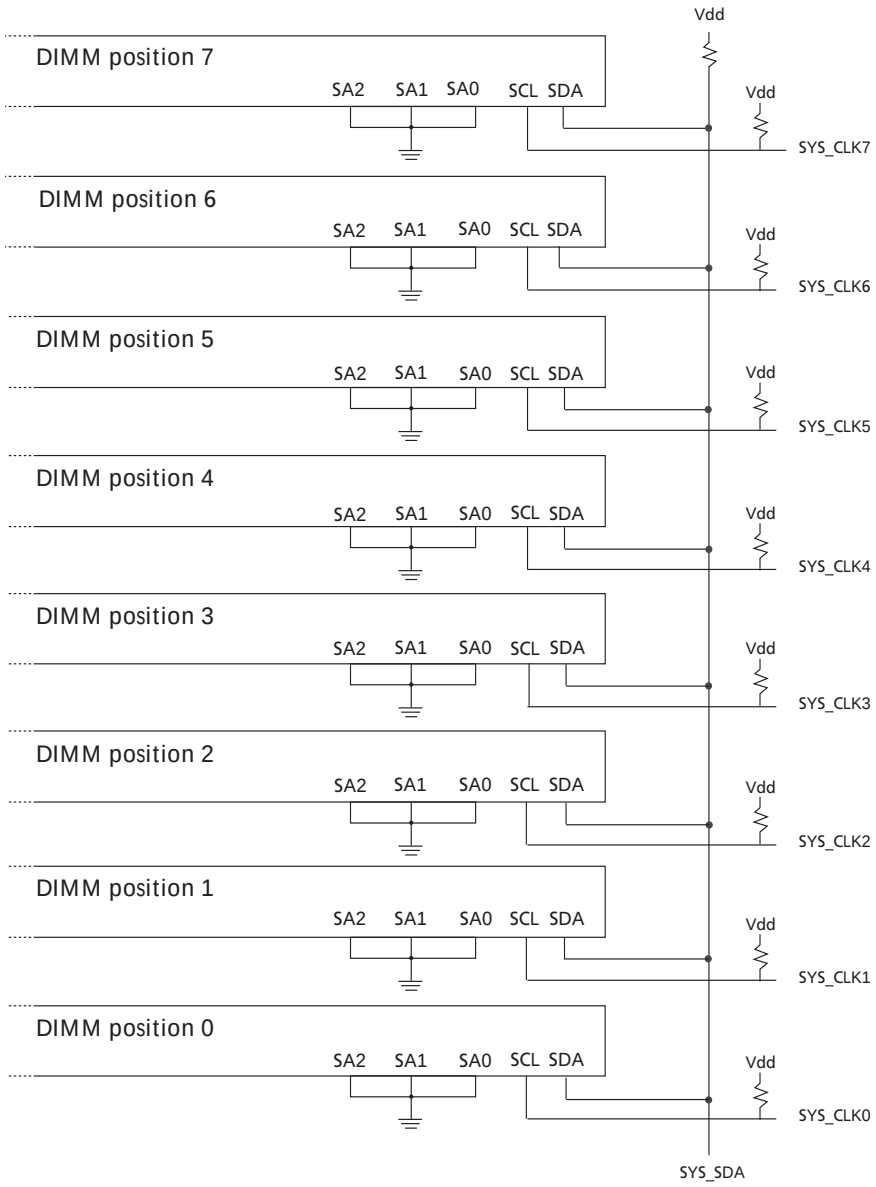
Common Data/Separate Clock

In the common data/separate clock configuration, SA0–SA2 are wired at each DIMM to the same address, as shown in Figure 5. The SDA is wired to all positions. The SCL is unique for each position, enabling more than 8 positions, but not permitting CMAX to exceed 400pF.

Figure 5: SPD Block Diagram for Common Data/Separate Clock



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Decimal to Binary to Hex Conversions

Table 3 shows how to place a decimal value in a binary (0/1) format and then create a hex value from that binary value.

In the hexadecimal system, the 8 bits of each byte are split into 2 sets of 4 nibbles each. The value generated from the bits in the upper nibble create the first hex character, while the bit values in the lower nibble generate the second hex character. Each nibble can have a maximum decimal value of 15. Hex values include 00 through 09, 10 = 0A, 11 = 0B, 12 = 0C, 13 = 0D, 14 = 0E, and 15 = 0F. Following this sequence, adding 1 to 0x0F results in 0x10, or 16 in decimal.

As shown in Table 3, the binary value of 45 results in a 2 in the upper hex nibble and 13 (or D) in the lower hex nibble. Thus, the hex value for 45 is 2D, usually displayed as 0x2D. If this looks familiar, it is because ASCII is based in the hexadecimal numbering system.

Table 3: Decimal to Binary to Hex Conversions

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Decimal Output
Binary values	128	64	32	16	8	4	2	1	
	0	0	1	0	1	1	0	1	45
Hex values	8	4	2	1	8	4	2	1	
	0	0	1	0	1	1	0	1	
	2				D				45

Serial Presence-Detect Tables

All serial presence-detect tables have the same basic format. Bytes are numbered sequentially from 0 to 255, and each byte consists of 8 data bits. These 8 bits, either with 0 or 1 values, generate a byte's hex value. Each SPD byte has an associated data or lookup table, showing which module parameter is represented. In some instances, the hex value directly represents a parameter. For example, SPD byte 0 has a hex value of 0x80, or decimal 128. Byte 0 represents the number of SPD bytes used by the module manufacturer; Micron uses the first 128 SPD bytes.

The majority of SPD bytes are associated with lookup tables that define parameters associated to that specific module. A byte's hex number will represent the parameters listed in the table, not just the numeric hex value. SPD data tables for Micron module part numbers can be viewed online in the SPD Lookup tool at www.micron.com/spd.

Step 1 - Identifying and Analyzing Bytes

The process for analyzing a specific SPD byte is shown in Table 4 on page 11 using bytes 14 and 15 from the DDR3 module SPD definitions (pending JEDEC approval at the time of publication). For more information about a particular byte's purpose and function, refer to the appropriate appendix listed in the section,"Serial Presence-Detect" on page 2.

Table 4 on page 11 is an example of a serial presence detect table for a DDR3 module. Each byte defines a specific feature or parameter of the module. For this example, we will verify the information held in bytes 14 and 15 against the JEDEC specification. Micron-specific SPD values can be seen by typing a Micron® module part number in the SPD Lookup tool at www.micron.com/spd.

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Table 4: DDR3 SDRAM Serial Presence-Detect Table

Hex values shown are examples and will differ depending on the configuration of the module

Byte Number	Function Described	SPD Hex Values
0	DDR3-CRC RANGE, EEPROM BYTES, BYTES USED	92
1	DDR3-SPD REVISON	05
2	DDR3-DRAM DEVICE TYPE	0B
3	DDR3-MODULE TYPE (FORM FACTOR)	01
4	DDR3-SDRAM DEVICE DENSITY & BANKS	02
5	DDR3-SDRAM DEVICE ROW & COLUMN COUNT	12
6	DDR3-BYTE 6 RESERVED	00
7	DDR3-MODULE RANKS & DEVICE DQ COUNT	00
8	DDR3-ECC TAG & MODULE MEMORY BUS WIDTH	0B
9	DDR3-FINE TIMEBASE DIVIDEND/DIVISOR	52
10	DDR3-MEDIUM TIMEBASE DIVIDEND	01
11	DDR3-MEDIUM TIMEBASE DIVISOR	08
12	DDR3-MIN SDRAM CYCLE TIME (TCKMIN)	0C
13	DDR3-BYTE 13 RESERVED	00
14	DDR3-CAS LATENCIES SUPPORTED (CL4 => CL11) (LSB)	7C
15	DDR3-CAS LATENCIES SUPPORTED (CL12 => CL18) (MSB)	00
16	DDR3-MIN CAS LATENCY TIME (TAAMIN)	6C
17	DDR3-MIN WRITE RECOVERY TIME (TWRMIN)	78
18	DDR3-MIN RAS# TO CAS# DELAY (TRCDMIN)	6C
19	DDR3-MIN ROW ACTIVE TO ROW ACTIVE DELAY (TRRDMIN)	30
20	DDR3-MIN ROW PRECHARGE DELAY (TRPMIN)	6C
21	DDR3-UPPER NIBBLE FOR TRAS & TRC	11
22	DDR3-MIN ACTIVE TO PRECHARGE DELAY (TRASMIN)	20
23	DDR3-MIN ACTIVE TO ACTIVE/REFRESH DELAY (TRCMIN)	8C
24	DDR3-MIN REFRESH RECOVERY DELAY (TRFCMIN) LSB	70
25	DDR3-MIN REFRESH RECOVERY DELAY (TRFCMIN) MSB	03
26	DDR3-MIN INTERNAL WRITE TO READ CMD DELAY (TWTRMIN)	3C
27	DDR3-MIN INTERNAL READ TO PRECHARGE CMD DELAY (TRTPMIN)	3C
28	DDR3-MIN FOUR ACTIVE WINDOW DELAY (TFAWMIN) MSB	00
29	DDR3-MIN FOUR ACTIVE WINDOW DELAY (TFAWMIN) LSB	F0
30	DDR3-SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	82
31	DDR3-SDRAM DEVICE THERMAL & REFRESH OPTIONS	05
32	DDR3-MODULE THERMAL SENSOR	80
33	DDR3-SDRAM DEVICE TYPE	00
34–59	DDR3-RESERVED BYTES 34–59	00
60	DDR3-MODULE HEIGHT (NOMINAL)	03
61	DDR3-MODULE THICKNESS (MAX)	11
62	DDR3-REFERENCE RAW CARD ID	0B
63	DDR3-ADDRESS MAPPING EDGE CONNECTOR TO DRAM	00
64	DDR3-HEAT SPREADER SOLUTION	00
65	DDR3-REGISTER VENDOR ID (LSB)	04
66	DDR3-REGISTER VENDOR ID (MSB)	B3

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Table 4: DDR3 SDRAM Serial Presence-Detect Table (continued)
Hex values shown are examples and will differ depending on the configuration of the module

Byte Number	Function Described	SPD Hex Values
67	DDR3-REGISTER REVISON NUMBER	03
68	DDR3-REGISTER TYPE	00
69	DDR3-REG CTRL WORDS 1 AND ZERO	00
70	DDR3-REG CTRL WORDS 3 AND 2	50
71	DDR3-REG CTRL WORDS 5 AND 4	55
72	DDR3-REG CTRL WORDS 7 AND 6	00
73	DDR3-REG CTRL WORDS 9 AND 8	00
74	DDR3-REG CTRL WORDS 11 AND 10	00
75	DDR3-REG CTRL WORDS 13 AND 12	00
76	DDR3-REG CTRL WORDS 15 AND 14	00
77–116	DDR3-RESERVED BYTES 77–116	00
117	DDR3-MODULE MFR ID (LSB)	80
118	DDR3-MODULE MFR ID (MSB)	2C
119	DDR3-MODULE MFR LOCATION ID	Variable
120	DDR3-MODULE MFR YEAR	Variable
121	DDR3-MODULE MFR WEEK	Variable
122–125	DDR3-MODULE SERIAL NUMBER	Variable
126–127	DDR3-CRC	Variable
128–145	DDR3-MODULE PART NUMBER	18JBF25672PY-1G4DZ
146	DDR3-MODULE DIE REV	44
147	DDR3-MODULE PCB REV	5A
148	DDR3-DRAM DEVICE MFR ID (LSB)	80
149	DDR3-DRAM DEVICE MFR (MSB)	2C
150–175	DDR3-MFR RESERVED BYTES 150–175	00
176–255	DDR3-CUSTOMER RESERVED BYTES 176–255	FF

Step 2 - Comparing Bytes Against JEDEC Specifications

Bytes 14 and 15 have values of 7Ch and 00h, respectively. Converting 07h to an 8-bit binary word yields 00000111. Converting 00h to an 8-bit binary word yields 00000000. Cross-referencing the 8-bit word against the lookup table for bytes 14 and 15 from the DDR3 module SPD definitions (pending JEDEC approval at the time of publication) shows that this module supports CAS latencies 6 through 10 (see Table 5 on page 13). In this manner, the hexidecimal value of any byte can be translated into common terms.

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Supported CAS Latencies Defined by Bytes 14 and 15

Bytes 14 and 15 define which CAS Latency (CL) values are supported. The range is from CL = 4 through CL = 18, with 1 bit per possible CAS latency. A 1 in a bit position means that CL is supported; a 0 in that bit position means it is not supported. Because CL = 6 is required for all DDR3 speed bins, bit 2 of SPD byte 14 is always 1. These values are found in the DDR3 SDRAM data sheet.

Table 5: Byte 14: CAS Latencies Supported, Least Significant Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5	CL = 4
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	1	0 or 1	0 or 1

Notes: 1. For each bit position, 1 means this CAS latency is supported; 0 means this CAS latency is not supported.

Table 6: Byte 15: CAS Latencies Supported, Most Significant Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	CL = 18	CL = 17	CL = 16	CL = 15	CL = 14	CL = 13	CL = 12
0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Notes: 1. For each bit position, 1 means this CAS latency is supported; 0 means this CAS latency is not supported.

Conclusion

Timing parameters, operating frequencies, and other electrical attributes, as well as many different physical and mechanical attributes, have been defined for memory modules. SPD is essential to ensure the standardization of this information, making the information usable for designers, manufacturers, and users.

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