Hybrid Memory Cube

Webinar July 2017

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Agenda

HMC Introduction and Status

– The Memory Wall
– What is the Hybrid Memory Cube
– Enabling Technologies
– Target Applications
– HMC Production Status and Design Wins
– HMCC, the HMC Consortium
– Ecosystem Update

Technical Overview

– Technical Collateral
– HMC Architectural Overview
– HMC Topologies and Chaining
– HMC Protocol
– RAS Features
– Sideband Access
– Distribution Network

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Hybrid Memory Cube

Introduction and Status

Stephan von Appen, Sr. Marketing Manager
Compute & Networking Business Unit
July 2017
System Memory Bandwidth Gap
MEMORY SYSTEMS ARE NOT SCALING AND DRIVE EXPONENTIAL COMPLEXITY

Bandwidth Per Memory Channel
2012–2017 CAGR: 12.3%

- DDR
  1-2 Memory Channels
  Up to 6.4GB/s
  3 Speed Bins
  85 page specification
  <3 Yrs to Standardize

- DDR2
  2 Memory Channels
  Up to 10.7GB/s
  5 Speed Bins

- DDR3
  3-4 Memory Channels
  240 Pins Per DIMM
  Up to 59.7GB/s
  6+ yrs to Standardize

- DDR4
  4-6 Memory Channels
  284 Pins Per DIMM
  Up to 85GB/s
  12 Speed Bins
  6+ yrs to Standardize
The Memory Wall

• WE STARTED TALKING ABOUT THE MEMORY WALL IN THE ‘90S
  – Evolutionary standards do **NOT** address The Memory Wall
  – Bandwidth **AND** power must be addressed

• SYSTEM POWER LIMITS CONSTRAIN PERFORMANCE; PERFORMANCE CAN GROW IF POWER IS ADDRESSED

• THE HYBRID MEMORY CUBE (HMC) IS A SOLUTION FOR **BANDWIDTH, POWER AND SCALABILITY**. HMC ENABLES CPU SYSTEM PERFORMANCE GROWTH.
Hybrid Memory Cube

- **Hybrid**
  - *Stack* of advanced **DRAM plus logic**
  - Combined into a single **advanced BGA package**
  - *Serially attached to host via 15Gb/s SERDES lanes*

- **Memory**
  - Current designs are **DRAM-based memory**

- **Cube**
  - *Combines logic and DRAM layers* into a **performance optimized, 3D package** leveraging state of the art **through-silicon via (TSV) technology**
Hybrid Memory Cube

Micron Innovation
We’ve combined fast logic process technology and advanced DRAM designs to create an entirely new category we’re calling Hybrid Memory Cube (HMC).

The end result is a high-bandwidth, low-energy, high-density memory system that’s unlike anything on the market today.

Unprecedented Performance
HMC provides a revolutionary performance enriching next-generation networking and computing platforms.

- **Explosive Bandwidth**
  Up to 8x the performance of DDR4

- **Reduced Footprint**
  90% of the space of RDIMM solution

- **Lower Power**
  Highly efficient energy per bit
Enabling Technologies

Abstracted Memory Management

Memory Vaults Versus DRAM Arrays
• Significantly improved bandwidth, quality and reliability versus traditional DRAM technologies

Logic Base Controller
• Reduced memory complexity and significantly increased performance
• Allows memory to scale with CPU performance

Through-Silicon Via (TSV) Assembly

Innovative Design & Process Flow
• Incorporation of thousands of TSV sites per die reduces signal lengths and reduces power
• Enables memory scalability through parallelism

Sophisticated Package Assembly
• Higher component density and significantly improved signal integrity
Where does this fit?

- **Primarily**
  - Networking
    - HMC’s impressive 160 GB/s bandwidth boosts networking systems’ capabilities to match line speed performance in the face of ever-increasing global demand for mobility and the impact of cloud services
  - High Performance Compute
    - HMC’s high bandwidth, low energy/bit, pin savings, and smaller form factor are game changers for high-performance computing (HPC) applications
- **Others**
  - Bandwidth is critical
  - Board space / pin count is critical
  - $/Gbps (BW)
Leading with New Innovations: HMC

Revolutionary Approach to Break Through the “Memory Wall”
- Evolutionary DRAM roadmaps hit limitations of bandwidth and power efficiency
- Micron introduces a new class of memory: Hybrid Memory Cube
- Unique combination of DRAMs on Logic smashes through the memory wall

Unparalleled Performance
- Provides 15X the bandwidth of a DDR3 module
- Uses 70% less energy per bit than existing memory technologies
- Reduces the memory footprint by nearly 90% compared to today’s RDIMMs

Key Applications
- Data packet processing, data packet buffering, and storage applications
- Enterprise and computing applications

How did we do it?
- Micron-designed logic controller
- High speed link to CPU
- Massively parallel “Through Silicon Via” connection to DRAM
HMC in Mass Production

- **HMC SR-15 (Gen2)**
  - 160GB/s Bandwidth
  - 10Gbs, 12.5Gbs, 15Gbs SerDes
  - 31mm x31mm 4 link package
  - 2GB density

- **Commercial Update**
  - Production volume available now
  - Over 3 Mio cubes shipped to date
  - +250 leads to date in EMEA

- **Production Part Number:**

<table>
<thead>
<tr>
<th>Density</th>
<th>Links</th>
<th>MPN</th>
<th>Package Size</th>
<th>Ball Count</th>
<th>Ball Pitch</th>
<th>DRAM per Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>2GB</td>
<td>4</td>
<td>MT43A4G40200NFA-S15:A</td>
<td>31x31x4.2</td>
<td>896</td>
<td>1.00</td>
<td>4</td>
</tr>
</tbody>
</table>

31x31mm 1mm pitch
896 balls

2GB 4 DRAM die
HMC Design Wins, Examples

South Africa’s MeerKAT array uses advanced Micron memory to explore deep space.
Networking Example - 400Gb/s Buffering

**DDR4**

- # of Memory Devices: 72
- Total # of Pins: 1,896
- Host PHY+ Memory Power: 49W
- Memory Surface Area: 8,532mm²

**HMC**

- # of Memory Devices: 1
- Total # of Pins: 276
- Host PHY+ Memory Power: 32W
- Memory Surface Area: 961mm²

**System Level Savings**

- 85% fewer pins
- 35% lower power
- 89% smaller footprint
HMCC, Hybrid Memory Cube Consortium

http://www.hybridmemorycube.org/

Hybrid Memory Cube Consortium (HMCC)

8 Developers and 150+ Adopters

HMCC Consortium Specifications

Rev 1.0: >2,700 downloads since May’13
Rev 2.0: >2,600 downloads since Nov’14

OpenHMC Controller (Open Source)

>7500* website accesses
>1600* HMC package downloads

Next Generation FPGA Support

Altera (Intel) Arria10 and Stratix10
Xilinx Ultrascale and Ultrascale+
Altera HMC Support

**Stratix V**
- HMC Controller Card
- ATX Form Factor
- ATX Power Supply connector
- 10G/100G/1000G Ethernet connectors
- Hybrid Memory Cube

**Arria 10**
- HMC Daughter Card
- HMC Device
- HMC Gen2 Controller IP Development Kit User Guide Reference Design

**Stratix 10**
- HMC 15G-SR Capable

- Industry First HMC Demo!
- Stratix V FPGA 4 x FPGA Total 1 x HMC Device Single FPGA “Master”
- Available Now

- 2013
- 2015
- 2017

Contact Intel PSG for more information
Altera Arria 10
COMPREHENSIVE PRODUCTION HMC SUPPORT

- **Arria 10 HMC IP**
  - Supports HMC Specification 1.1
  - High quality, internally developed HMC controller IP
  - Fast simulation support, real time error statistics, hardware reset control
  - Available today with Quartus Prime 17.0 from Download Center

- **Designed for Maximum Performance**
  - Simple full width x16 (512b) client interface
  - Demonstrated at 10, 12.5 and 15Gb/s rates
  - Minimizes logic footprint using response open loop for Rx flow control
  - Support for 16B, 32B, 64B & 128B payloads

### Xilinx Now Offering HMC IP

<table>
<thead>
<tr>
<th>Benefit</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Excellent Performance</td>
<td>• 240 Gb/s bandwidth per HMC link (Gen2, full duplex, x16 lanes)</td>
</tr>
<tr>
<td></td>
<td>• 85% reduced board space</td>
</tr>
<tr>
<td>Fully HMC Gen2 Compliant</td>
<td>Optimized &amp; Verified Ultrascale &amp; Ultrascale+ Controller IP</td>
</tr>
<tr>
<td>Flexible &amp; Parameterizable</td>
<td>• AXI Memory-Mapped interface</td>
</tr>
<tr>
<td>Controller</td>
<td>• All packet sizes supported (16 to 128 Byte)</td>
</tr>
<tr>
<td></td>
<td>• Variable data path width</td>
</tr>
<tr>
<td>High Throughput Efficiency</td>
<td>10G, 12.5G, and 15G half width (x8), and full width (x16)</td>
</tr>
<tr>
<td>Complete Xilinx Solution</td>
<td>• Evaluation boards and IP available now</td>
</tr>
<tr>
<td></td>
<td>• IP solution fully integrated since Vivado 2016.1 (currently 201.7.1)</td>
</tr>
</tbody>
</table>

**VCU110 HMC Evaluation Board**
- Virtex UltraScale 190 (-2 speed grade)
- HMC (32 GTHs, 2 full links
  Bandwidth = 42 + 42 =64 GB/s

**HMC Controller IP**
- AXI-MM or Native Interface
- Variable data path width
- Variable packet size

**XHMC Core**
- Transaction Layer
  - Master
  - Slave
- Link Layer
  - Master
  - Slave
- Physical Layer
  - TX
  - RX
- Power State Management

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VCU110
400+ GBPS AND 28 GBPS BACKPLANE DEVELOPMENT

- 4 CPF4 Optical Interfaces
- 28 Gbps Backplane Interface
- 20 GTY Interlaken Interface
- 2 FMC HPC Interfaces
- Micron HMC
- Dual 512MB Quad-SPI flash
- Micron 576Mb x18 RLDRAM 3
- Micron 576Mb x36 RLDRAM 3
OpenHMC
OPEN SOURCE HMC CONTROLLER

- Developed by the Computer Architecture Group (CAG) at the University of Heidelberg
  - Configurable
  - Vendor-agnostic
  - AXI-4 compliant
  - Flexible data-widths/lane widths and clock speeds depending on area requirements
  - Test environment to evaluate capabilities
  - Lower barrier for HMC evaluation

http://ra.ziti.uni-heidelberg.de/cag/research/recent-research-projects/openhmc
Micron Advanced Computing Solutions

**Hardware**
- FPGA modules, boards, and systems targeted at HPC applications, all of which integrate the latest memory technologies from Micron technology

**Firmware & Software**
- Fully-integrated solution
- Host drivers (Linux), APIs, etc..
- Memory controllers, PCIe interface, DMA engine

**Development Environment**
- Traditional HDL Flow (Verilog/VHDL)
- OpenCL (Xilinx's SDA or Altera's OpenCL). Board Support Packages Provided
- Convey HT Flow (for certain boards)

**Customer Support**
- Example applications and documentation
- Includes 20 hours of support
- Support provided by Seattle engineering.
Hardware Overview

**AC-Series:** FPGA Compute Modules

- AC-505: 8GB DDR3 SODIMM, Kintex 7
- AC-506: 8GB DDR3 SODIMM, Stratix V
- AC-510: 4GB HMC, Kintex UltraScale
- AC-520: 2GB HMC, DDR4, Arria 10 (Q1 17)

**EX-Series:** Backplanes for AC-Series

- EX-700: 6 AC Modules
- EX-750: 4 AC Modules

**SB-Series:** Single Board HMC Boards

- SB-801: 4GB HMC, 4 Stratix V
Up to 6 Modules Populated on a Single PCIe Board
Hardware Roadmap

Modules

- AC-520
  - Arria 10
  - HMC
  - DDR4
- AC-511
  - VU7P
  - HMC
  - DDR4
- AC-521
  - Stratix 10
  - HMC
  - DDR4
- AC-512
  - Xilinx
  - HMC
  - DDR4

Single-board Computers

SB-851
- Virtex UltraScale+
- VU7P / VU9P
- HMC or DDR4
- 72MB SRAM
- HH/HL

SB-852
- Virtex UltraScale+
- VU7P / VU9P
- 2 x 2GB HMC
- 4 x 32GB DDR4
- FH/3/4L

SB-803
- Stratix 10
- HMC
- DDR4
- 72MB SRAM
- HH/3/4L

Specifications subject to change at any time

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HMC Plug-and-Play System

- Fully HMC specification 1.1 compliant & validated/tested
  - Complete development system = Controller, Linux, Pico Framework, all hardware
  - Documentation, getting started guides, simulations, GUPS, test apps
  - Memory controllers, DMA engine, PCIe, APIs, Linux drivers, test apps
  - Design examples
HMC Technical Collateral
HMC Technical Collateral

- All HMC technical documents can be found from Micron.com using HMC as the search keyword
- HMC Datasheet and User Guide available without NDA, however Micron.com account is needed

<table>
<thead>
<tr>
<th>Documentation &amp; Tools</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>HMC Datasheet</td>
<td>NOW</td>
</tr>
<tr>
<td>HMC User Guide</td>
<td>NOW</td>
</tr>
<tr>
<td>Power Calculator Spreadsheet</td>
<td>NOW</td>
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<tr>
<td>2-in-1 model (performance+BFM model)</td>
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<tr>
<td>IBIS-AMI SERDES Simulation Model</td>
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<tr>
<td>S-Parameter SERDES Model</td>
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<tr>
<td>IBIS Model For Low Speed IO</td>
<td>NOW</td>
</tr>
<tr>
<td>Power Delivery Network (PDN) Simulation Kit</td>
<td>NOW</td>
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<tr>
<td>HMC Frequently Asked Questions (FAQ)</td>
<td>NOW</td>
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<tr>
<td>(RAS) Reliability, Availability, and Serviceability</td>
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<tr>
<td>Pin Map Files (ease of symbol creation)</td>
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<tr>
<td>FloTHERM Thermal Models</td>
<td>NOW</td>
</tr>
<tr>
<td>HMC200 board schematic+BOM</td>
<td>NOW</td>
</tr>
</tbody>
</table>
HMC Architecture Overview
Hybrid Memory Cube

*TSV, HETEROGENEOUS SILICON LAYERS AND ADVANCED PACKAGING*

Memory Density

4H = 2GB

Memory Bandwidth

Wide Bus

160GB/s

Processor

High-Speed Serial Links

10, 12.5, 15Gbps

Logic Layer

Link Bandwidth

4x(16x2)x15Gbps = 240GB/s

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HMC Step By Step - Lane

- A lane is a single transceiver i.e. a TX and an RX combined
- Transmitter differential pair and serializer + Receiver differential pair and de-serializer
- Together, often referred to as a SERDES or Transceiver
HMC Step By Step - Link

- **A Link** is defined as a collection of 16 Transceiver pairs (SERDES Tx and Rx) which are used to send and receive data.

- A ½ link is therefore simply a collection of 8 Transceiver pairs (SERDES Tx and Rx) which are used to send and receive data.

- Each Link of the HMC device (up to four in total) is connected to a Quadrant.
A Quadrant is defined as a single link (16 transceiver pairs), four vault controllers and four Memory Interface Controllers.

All Links can access all Quadrants using the internal HMC Crossbar Switch for “remote” quadrants.
Every vault is functionally independent from every other vault.

Access and control of each vault is through a local vault controller in the logic.

A vault supports from 16 Byte to 128 Byte data transfers per access.

There are 16 vaults per HMC.
Each Link has 16 Lanes (RX/TX pairs)

HMC Gen2 has Four Available Links

Link Interface Example

4 Link Example (160GB/s)
- 10Gb/s per lane
- 32 lanes per link (320Gb/s = 40GB/s)
- 16 TX and 16 RX
- 4 Links (40GB/s x 4) = 160GB/s

10, 12.5 & 15Gbps SERDES Options
HMC Single Link Bandwidth

- As one link has 16 Rx and 16 Tx transceivers the maximum bandwidth for a single link is 60GB/s

\[
\text{Max single link BW when 15Gb/s lane speed is used} = 16 \times 2 \times 15\text{Gb/s} = 60\text{GB/s}
\]
HMC Summary

- **A lane is a single transceiver** i.e. a TX and an RX combined. Supports data rates of **10.0 Gb/s**, **12.5 Gb/s**, and **15.0 Gb/s** (duplex)

- **A Link is defined as a collection of 16 Transceiver pairs** (SERDES Tx and Rx) which are used to send and receive data

- **A ½ link is a collection of 8 Transceiver pairs** (SERDES Tx and Rx) which are used to send and receive data

- A single HMC consists of **4 links** which mean that there are **4 x 16 = 64 lanes** in total

- The **maximum link bandwidth of HMC** is **4 x (16 x 2) x 15Gb/s = 240GB/s** if all four links are used at maximum speed (15Gb/s)
HMC Topologies and Chaining
HMC System Topologies

- **Near Memory**
  - All links between host and HMC
  - Maximum BW per GB density

- **Applications**
  - HPC/Server
  - Networking
  - Test Equipment
  - Graphics

- **Far Memory**
  - HMC links connect to host or other cubes
  - Links form networks of cubes
  - Scalable to meet system requirements
HMC Topologies

CHAINED, STAR, OR HOST TO CUBE
MULTI-HOST OPERATION SUPPORTED
HMC Protocol
Packet Layout

- **Host issues requests** and the **HMC issues responses**
- Packets are comprised of **128-bit (16B) FLITs**
- Each **Packet Contains 64b (8B) Header and 64b (8B) Tail**

**Note 1:** Data only included in packet if applicable to a request or response
Protocol Overhead

<table>
<thead>
<tr>
<th>Access size</th>
<th># of FLITs</th>
<th>Protocol Overhead</th>
</tr>
</thead>
<tbody>
<tr>
<td>16B</td>
<td>2</td>
<td>50%</td>
</tr>
<tr>
<td>32B</td>
<td>3</td>
<td>33%</td>
</tr>
<tr>
<td>48B</td>
<td>4</td>
<td>25%</td>
</tr>
<tr>
<td>64B</td>
<td>5</td>
<td>20%</td>
</tr>
<tr>
<td>80B</td>
<td>6</td>
<td>17%</td>
</tr>
<tr>
<td>96B</td>
<td>7</td>
<td>14%</td>
</tr>
<tr>
<td>112B</td>
<td>8</td>
<td>13%</td>
</tr>
<tr>
<td>128B</td>
<td>9</td>
<td>11%</td>
</tr>
</tbody>
</table>
Which SERDES rate makes the most sense?

**Example:**
- 90GB of Bandwidth needed
- 64B packets
  - 108GB of SERDES BW required due to Protocol overhead.

**Options:**
- 3 links @ 10Gbps \[BW = \frac{32 \times 3 \times 10}{8} = 120\text{GB}\]
- 3 links @ 12.5Gbps \[BW = \frac{32 \times 3 \times 12.5}{8} = 150\text{GB}\]
- 2 links @ 15Gbps \[BW = \frac{32 \times 2 \times 15}{8} = 120\text{GB}\]

**Pro’s & Con’s:**
- Design Complexity (number of routes, board layers, frequency challenges)
- Power/Thermals
- Access pattern (BW limitations [Power calculator/BW calculator])
End-to-End Error Protection

Figure 8: End-to-End Error Protection

- DRAM/TSVs
  - Data ECC coverage
  - Command/Address parity
  - DRAM/TSV repair
  - Data scrubbing

- Core/Crossbar
  - 32-bit CRC coverage

- Interface/PHY
  - 32-bit CRC coverage
  - Sequence field
  - Length field
  - Error and warning reporting

Host processor

Vault control

Crossbar switch

Link interface controller

Rx, Tx

High-speed links

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Sideband Access

- HMC includes support for JTAG and I2C
  - Both can be used to program and monitor configuration and status registers

- JTAG
  - Test access port compliant to IEEE 1149.1-2001 & 1149.6
  - Including boundary scan support
  - Operates up to 100 MHz clock

- I2C
  - Operates up to 400Kb/s (fast mode)
  - Complies with UM-10204 I2C bus specification
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