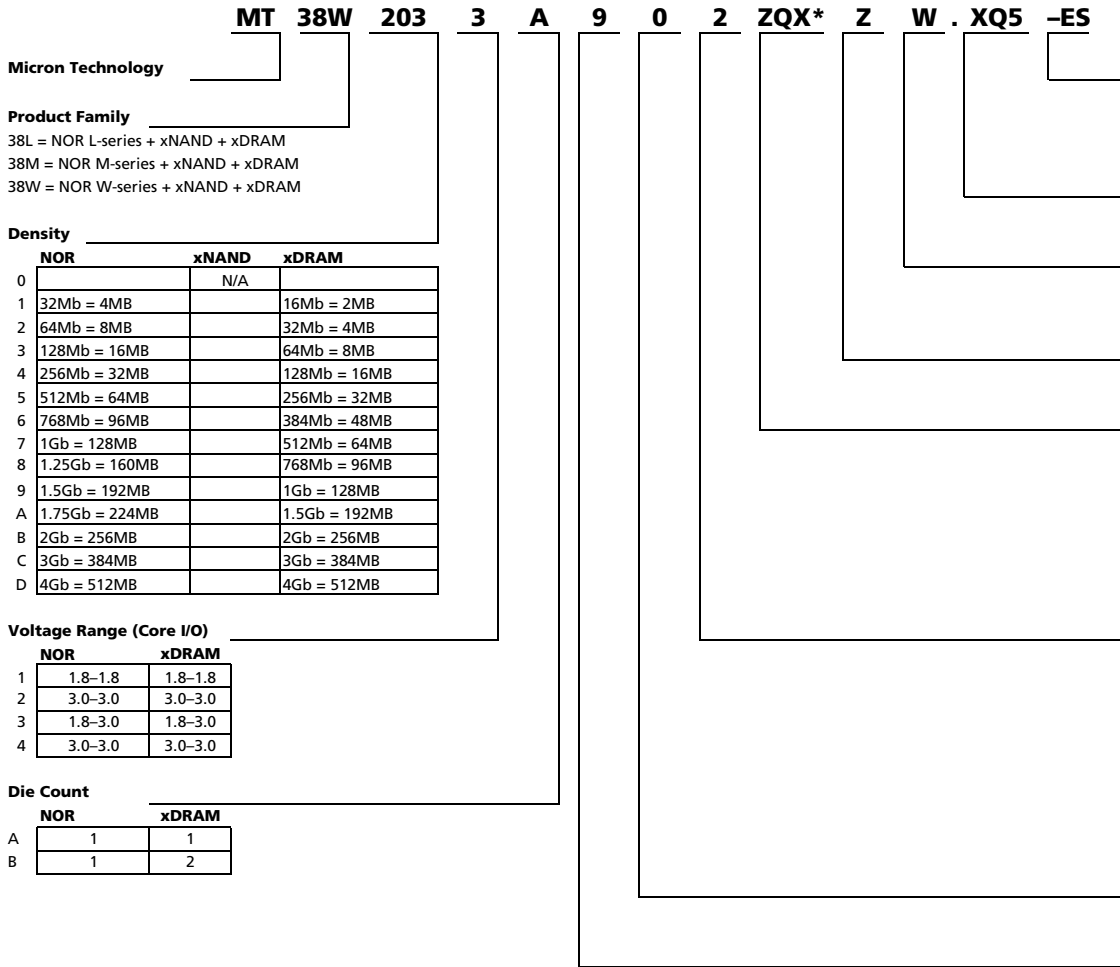


# NOR MCP Part Numbering System

Micron's part numbering system is available at [www.micron.com/numbering](http://www.micron.com/numbering)

## Multichip Packages



**Micron Technology**

**Product Family**

38L = NOR L-series + xNAND + xDRAM  
 38M = NOR M-series + xNAND + xDRAM  
 38W = NOR W-series + xNAND + xDRAM

**Density**

	NOR	xNAND	xDRAM
0		N/A	
1	32Mb = 4MB		16Mb = 2MB
2	64Mb = 8MB		32Mb = 4MB
3	128Mb = 16MB		64Mb = 8MB
4	256Mb = 32MB		128Mb = 16MB
5	512Mb = 64MB		256Mb = 32MB
6	768Mb = 96MB		384Mb = 48MB
7	1Gb = 128MB		512Mb = 64MB
8	1.25Gb = 160MB		768Mb = 96MB
9	1.5Gb = 192MB		1Gb = 128MB
A	1.75Gb = 224MB		1.5Gb = 192MB
B	2Gb = 256MB		2Gb = 256MB
C	3Gb = 384MB		3Gb = 384MB
D	4Gb = 512MB		4Gb = 512MB

**Voltage Range (Core I/O)**

	NOR	xDRAM
1	1.8-1.8	1.8-1.8
2	3.0-3.0	3.0-3.0
3	1.8-3.0	1.8-3.0
4	3.0-3.0	3.0-3.0

**Die Count**

	NOR	xDRAM
A	1	1
B	1	2

**Production Status**

Blank = Production  
 ES = Engineering samples  
 MS = Mechanical samples

**Die Revision Code**

Contact factory

**Operating Temperature Range**

I = Industrial (-40°C to +85°C)  
 W = Wireless (-25°C to +85°C)

**Special Options**

Contact factory

**Package Code**

ZA = VBGA 7.5x5x1 44 F10X4+4 O.5  
 19Z = VBGA 7.7x9x1 64 F10X6+4 P.5 B.3  
 ZQ = TFBGA 8X10X1.2 88 F8X10+8 0.8  
 ZS = VFBGA 8X6X156 10x6-8+4 .5 B.3  
 3RZ = VFBGA 8X8X1 133 3R14X14+1 0.5  
 \*X = a null character used as a placeholder.

**xDRAM Description**

0 = N/A  
 1 = ASYNC PSRAM  
 2 = SYNC PSRAM No Mux  
 3 = SYNC PSRAM AD Mux  
 4 = SYNC PSRAM AAD Mux  
 5 = x16 DDR1 1KB Page  
 6 = x16 DDR1 2KB Page  
 7 = x16 DDR1 4KB Page  
 8 = x32 DDR1 4KB Page

**NAND Description**

0 = N/A

**NOR Configuration**

	Boot	Mux
1	Uniform	NO
2	Uniform	AD
3	Uniform	AD/AAD**
4	Uniform	AAD
5	Bottom	NO
6	Bottom	AD
7	Bottom	AD/AAD**
8	Bottom	AAD
9	Top	NO
A	Top	AD
B	Top	AD/AAD**
C	Top	AAD

\*\*AAD interface configurable through register.

Rev. 9/12/2012

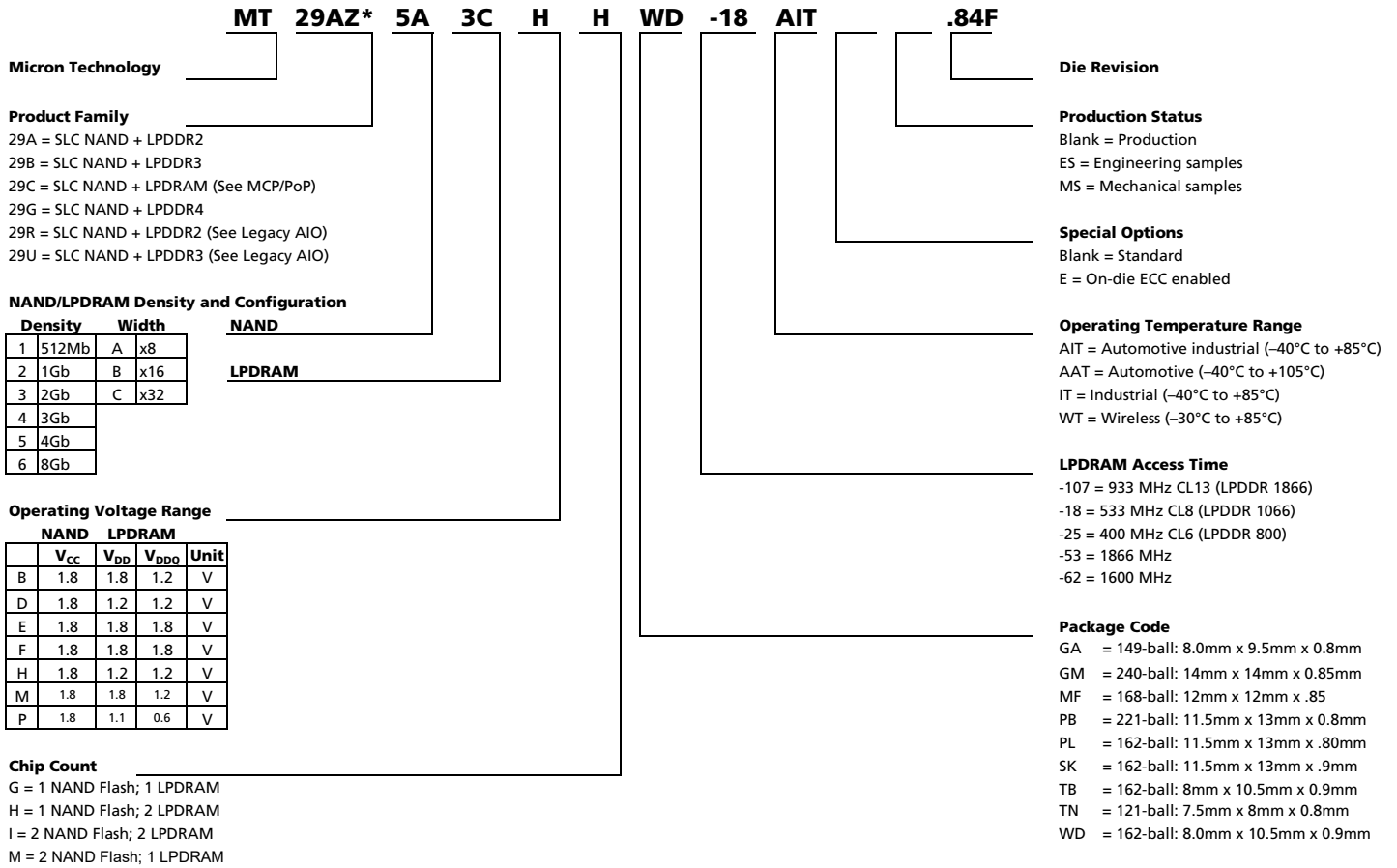
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# NAND MCP Part Numbering System

Micron's part numbering system is available at [www.micron.com/numbering](http://www.micron.com/numbering)

## Multichip Packages



\*Z = a null character used as a placeholder.

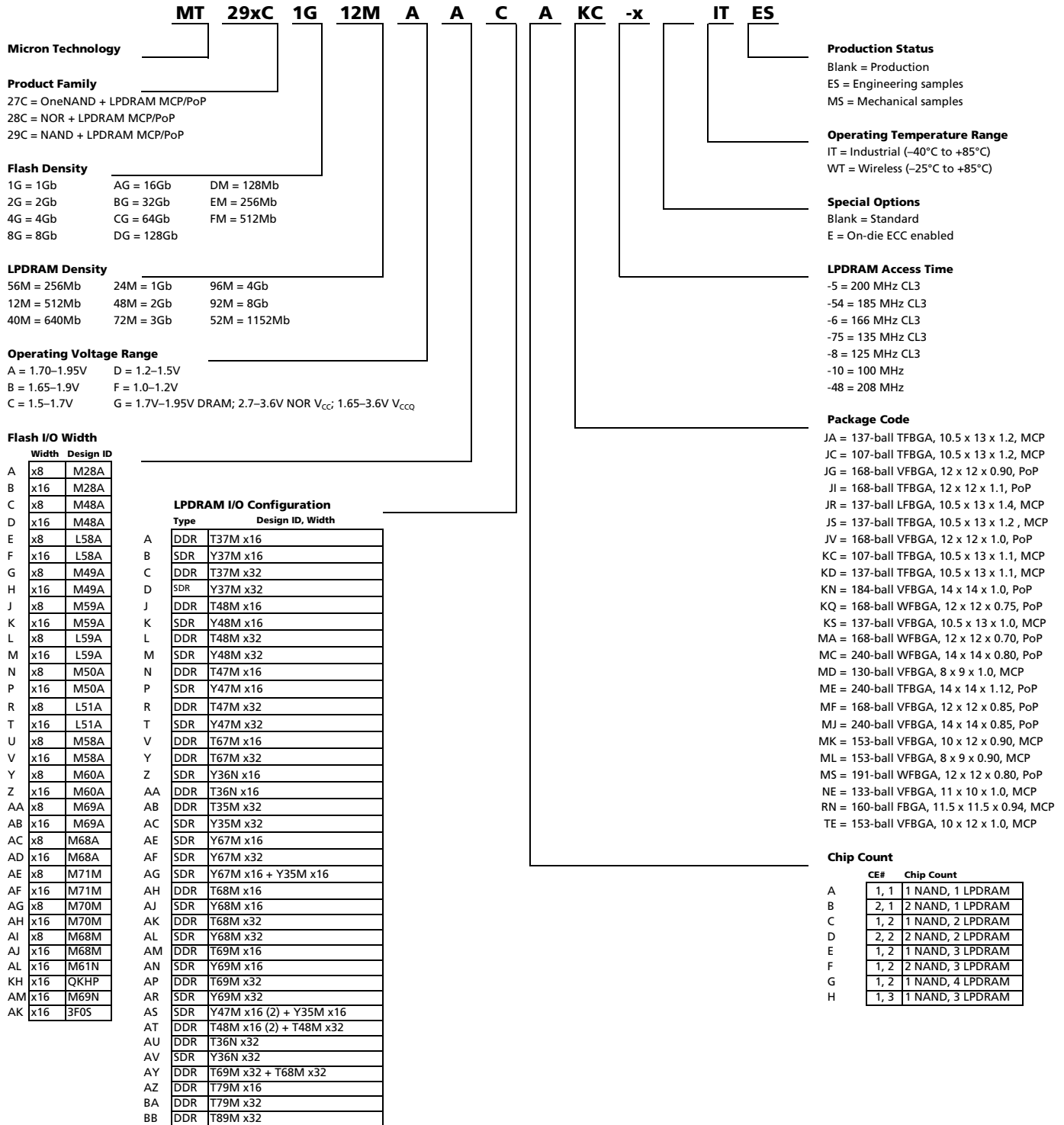
Rev. 11/14/2017



# MCP/PoP Part Numbering System

Micron's part numbering system is available at [www.micron.com/numbering](http://www.micron.com/numbering)

## Multichip Packages



Rev. 5/18/2016

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# All-in-One Part Numbering System

Micron's part numbering system is available at [www.micron.com/numbering](http://www.micron.com/numbering)

## AiO Packages

**Micron Technology**

**Product Family**

29C = SLC NAND + LPDDR (See MCP/POP)  
 29D = SLC NAND + LPDDR + MLC e.MMC (See MCP/POP)  
 29J = LPDDR + SLC e.MMC  
 29K = LPDDR + MLC e.MMC  
 29M = LPDDR2-S4 + SLC e.MMC  
 29P = LPDDR2-S4 + MLC e.MMC  
 29Q = SLC e.MMC + MLC e.MMC (See MCP/POP)  
 29R = LPDDR2-S4 + SLC NAND  
 29T = LPDDR3-S4 + MLC e.MMC  
 29U = LPDDR3-S4 + SLC NAND  
 29V = LPDDR4-S4 + MLC/TLC e.MMC/UFS

**NAND/LPDRAM Density/Configuration Code**

Density	Width	
T 768Mb	A x4	NAND Flash
U 640Mb	B x8	
V 512Mb	C x16	LPDRAM
W 256Mb	D x32	
X 128Mb	E x64	
Y 64Mb	F x96	
1 1Gb		
2 2Gb		
3 3Gb		
4 4Gb		
6 6Gb		
7 24Gb		
8 8Gb		
9 12Gb		
A 16Gb		
B 48Gb		
C 64Gb		

**e.MMC Density and Controller Code**

Density	Controller Version	Int	Controller Name
V 512MB		A	e.MMC version 4.41 PL_REG
W 256MB		B	e.MMC version 4.51 DC_PL_REG
X 128MB		C	e.MMC version 4.41 DC_PL_REG
1 1GB		D	e.MMC
2 2GB		E	e.MMC version 5.1
4 4GB		F	e.MMC version 1.3
5 8GB		H	e.MMC version 1.8
6 16GB		J	e.MMC version 5.0
7 32GB		K	e.MMC version 4.2
8 64GB		L	e.MMC version 4.2/4.3
9 128GB		M	e.MMC version 4.2/4.3
A 256GB		N	e.MMC version 4.4
B 512GB		P	e.MMC version 4.4
		Q	e.MMC version 4.4
		R	e.MMC version 4.41
		S	e.MMC version 4.41
		T	e.MMC version 4.41
		U	e.MMC version 4.41
		V	e.MMC version 4.5
		W	e.MMC version 4.5
		X	e.MMC version 4.41
		Y	e.MMC version 5.0

**Die Revision Code**  
Contact factory

**Production Status**  
Blank = Production  
ES = Engineering samples  
MS = Mechanical samples

**Special Options**  
Blank = Standard  
A = Customer variant  
B = 2MB boot area/2MB RPMB  
E = On-die ECC enabled  
F = SEC COUNT/custom boot area/custom RPMB

**Operating Temperature Range**  
A = Automotive (-40°C to +105°C)  
I = Industrial (-40°C to +85°C)  
W = Wireless (-25°C to +85°C)

**LPDRAM Speed Grade**  
-046 = 2133 MHz (LPDDR 4266)  
-062 = 1600 MHz (LPDDR 3200)  
-107 = 933 MHz CL13 (LPDDR 1866)  
-125 = 800 MHz CL12 (LPDDR 1600)  
-18 = 533 MHz CL8 (LPDDR 1066)  
-25 = 400 MHz CL6 (LPDDR 800)  
-3 = 333 MHz CL5 (LPDDR 667)  
-37 = 266 MHz CL4 (LPDDR 533)  
-5 = 200 MHz CL3 (LPDDR 400)  
-53 = 1866 MHz (LPDDR 3732)  
-54 = 185 MHz CL3 (LPDDR 1)  
-6 = 166 MHz CL3 (LPDDR 333)  
-75 = 133 MHz CL3 (LPDDR 266)

**Package Code**

**Chip Count**  
A = 1 NAND Flash (CEO); 1 LPDRAM; 1 e.MMC  
B = 2 NAND Flash (CEO); 1 LPDRAM; 1 e.MMC  
C = 1 NAND Flash (CEO); 2 LPDRAM (CS0#/CS1#); 1 e.MMC  
D = 2 NAND Flash (CEO); 2 LPDRAM (CS0#/CS1#); 1 e.MMC  
E = 0 NAND Flash; 1 LPDRAM; 1 e.MMC  
F = 0 NAND Flash; 2 LPDRAM (CS0#/CS1#); 1 e.MMC  
G = 1 NAND Flash; 1 LPDRAM; 0 e.MMC  
H = 1 NAND Flash; 2 LPDRAM; 0 e.MMC  
I = 2 NAND Flash; 2 LPDRAM; 0 e.MMC  
J = 0 NAND Flash; 0 LPDRAM; 2 e.MMC  
K = 0 NAND Flash; 4 LPDRAM; 1 e.MMC  
L = 0 NAND Flash; 3 LPDRAM; 1 e.MMC  
M = 2 NAND Flash; 1 LPDRAM; 0 e.MMC  
N = 4 NAND Flash; 4 LPDRAM; 0 e.MMC  
O = 0 NAND Flash; 6 LPDRAM; 1 e.MMC

**Operating Voltage Range**

	NAND		LPDRAM		e.MMC		Unit
	V <sub>CC</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>CCM</sub>	V <sub>CCQM</sub>		
A	N/A	1.8	1.8	1.8	1.8		V
B	1.8	1.8	1.2	1.8	1.8		V
C	1.8	1.35	1.2	1.8	1.8		V
D	1.8	1.2	1.2	1.8	1.8		V
E	1.8	1.8	1.8	3.3	1.8/3.3		V
F	1.8	1.8	1.8	1.8	1.8		V
G	N/A	1.8	1.8	3.3	1.8/3.3		V
H	1.8	1.2	1.2	N/A	N/A		V
J	N/A	1.2	1.2	1.8	1.8		V
K	N/A	1.2	1.2	3.3	1.8/3.3		V
L	N/A	N/A	N/A	3.3	1.8/3.3		V
M	1.8	1.8	1.2	1.8	N/A		V
N	3.3	1.2	1.2	N/A	N/A		V
P	N/A	1.1	1.1	3.3	1.8		V
Q	N/A	1.1	0.6	3.3	1.8		V
R	N/A	1.1	0.4	3.3	1.8		V

\*Z = a null character used as a placeholder.

Rev. 11/15/2017

