Data Sheet Addendum: LPDDR2 SDRAM

EDB8132B4PB-8D-F-R, EDB8132B4PB-8D-F-D

Features

This addendum documents features of the Micron® 4Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) device.

This addendum does not provide detailed device information. The standard density-specific device data sheet provides a complete description of device functionality, operating modes, and specifications unless specified herein.

Information provided here is in addition to or supersedes information in the device data sheet.

- Ultra-low-voltage core and I/O power supplies
- Frequency range
  - 400 MHz (data rate: 800 Mb/s/pin)
- 4*n* prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK_t/CK_c edge
- Bidirectional/differential data strobe per byte of data (DQS_t/DQS_c)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 4, 8, and 16
- Per-bank refresh for concurrent operation
- Auto temperature-compensated self refresh (ATCSR) by built-in temperature sensor
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- Lead-free (RoHS-compliant) and halogen-free packaging

Options

- $V_{DD1}/V_{DD2}/V_{DDQ}$: 1.8V/1.2V/1.2V
- Array configuration
  - 256 Meg x 32 (DDP)
- Packaging
  - 12mm x 12mm, 168-ball PoP FBGA package
- Operating temperature range
  - From –30°C to +85°C

Table 1: Configuration Addressing – Single-Channel Package

Architecture	256 Meg x 32
Density per package	8Gb
Die per package	2
Ranks per channel	1
Die per rank	2
Configuration	32 Meg x 16 x 8 banks x 2

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‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

Table 1: Configuration Addressing – Single-Channel Package (Continued)

Architecture	256 Meg x 32
Row addressing	16K A[13:0]
Column addressing	2K A[10:0]

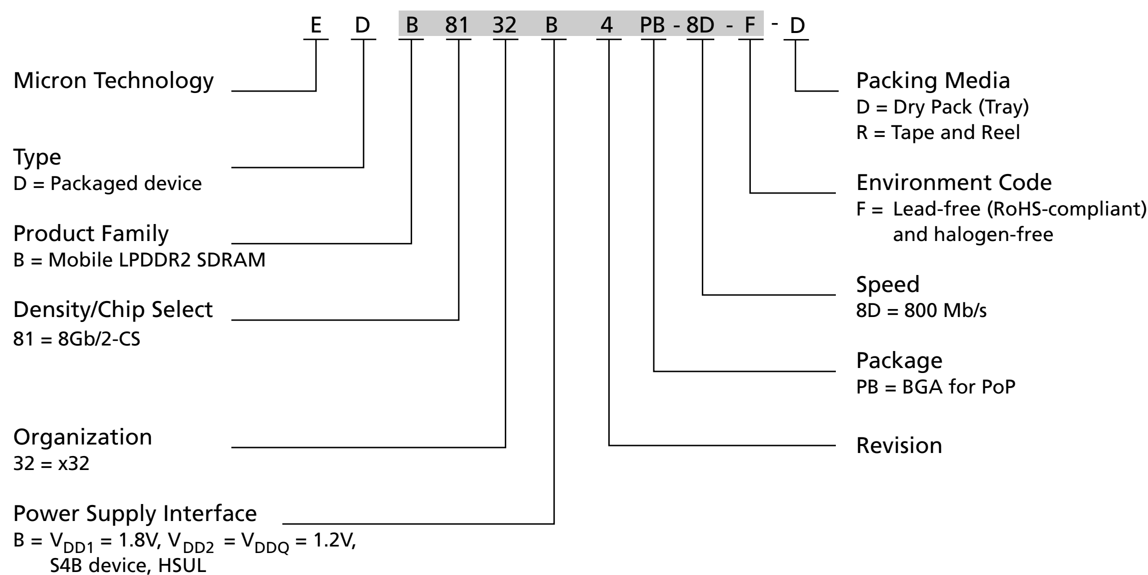
Table 2: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency	READ Latency
8D	400	800	3	6

Table 3: Part Number Description

Part Number	Total Density	Configuration	Ranks	Channels	Package Size	Ball Pitch
EDB8132B4PB-8D-F-R, EDB8132B4PB-8D-F-D	8Gb	256 Meg x 32	1	1	12mm x 12mm (0.80mm MAX height)	0.50mm

Figure 1: Marketing Part Number Chart



Note: 1. The characters highlighted in gray indicate the physical part marking found on the device.

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Ball Assignments

Figure 2: 168-Ball PoP Single-Channel FBGA – 2 x 4Gb Die, 12mm x 12mm

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	V_{SS}	DQ30	DQ29	V_{SS}	DQ26	DQ25	V_{SS}	DQS3_c	V_{DD1}	V_{SS}	NC	NC
B	NC	NC	V_{DD1}	NC	V_{SS}	NC	NC	V_{SS}	NC	V_{SS}	V_{DD2}	DQ31	V_{DDQ}	DQ28	DQ27	V_{DDQ}	DQ24	DQS3_t	V_{DDQ}	DM3	V_{DD2}	NC	NC
C	V_{SS}	V_{DD2}																				DQ15	V_{SS}
D	NC	NC																				V_{DDQ}	DQ14
E	NC	NC																				DQ12	DQ13
F	NC	V_{SS}																				DQ11	V_{SS}
G	NC	NC																				V_{DDQ}	DQ10
H	NC	NC																				DQ8	DQ9
J	NC	V_{SS}																				DQS1_t	V_{SS}
K	NC	NC																				V_{DDQ}	DQS1_c
L	NC	NC																				V_{DD2}	DM1
M	NC	V_{SS}																				V_{REFDQ}	V_{SS}
N	NC	V_{DD1}																				NC	DM0
P	ZQ0	V_{REFCA}																				DQS0_c	V_{SS}
R	V_{SS}	V_{DD2}																				V_{DDQ}	DQS0_t
T	CA9	CA8																				DQ6	DQ7
U	CA7	NC																				DQ5	V_{SS}
V	V_{SS}	CA6																				V_{DDQ}	DQ4
W	CA5	NC																				DQ2	DQ3
Y	CK_c	CK_t																				DQ1	V_{SS}
AA	V_{SS}	V_{DD2}																				V_{DDQ}	DQ0
AB	NC	NC	CS_n	NC	V_{DD1}	CA1	V_{SS}	CA3	CA4	V_{DD2}	V_{SS}	DQ16	V_{DDQ}	DQ18	DQ20	V_{DDQ}	DQ22	DQS2_t	V_{DDQ}	DM2	V_{DD2}	NC	NC
AC	NC	NC	CKE	NC	V_{SS}	CA0	CA2	NC	V_{SS}	NC	ZQ1	V_{SS}	DQ17	DQ19	V_{SS}	DQ21	DQ23	V_{SS}	DQS2_c	V_{DD1}	V_{SS}	NC	NC

Top View (ball down)

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Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

Table 4: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK.
CS_n	Input	**Chip select:** Considered part of the command code and is sampled on the rising edge of CK.
DM[3:0]	Input	**Input data mask:** Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0]_t, DQS[3:0]_c	I/O	**Data strobe:** Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground.**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ[1:0]	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NU	–	**Not usable:** Do not connect.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects; however, they could be connected together internally.

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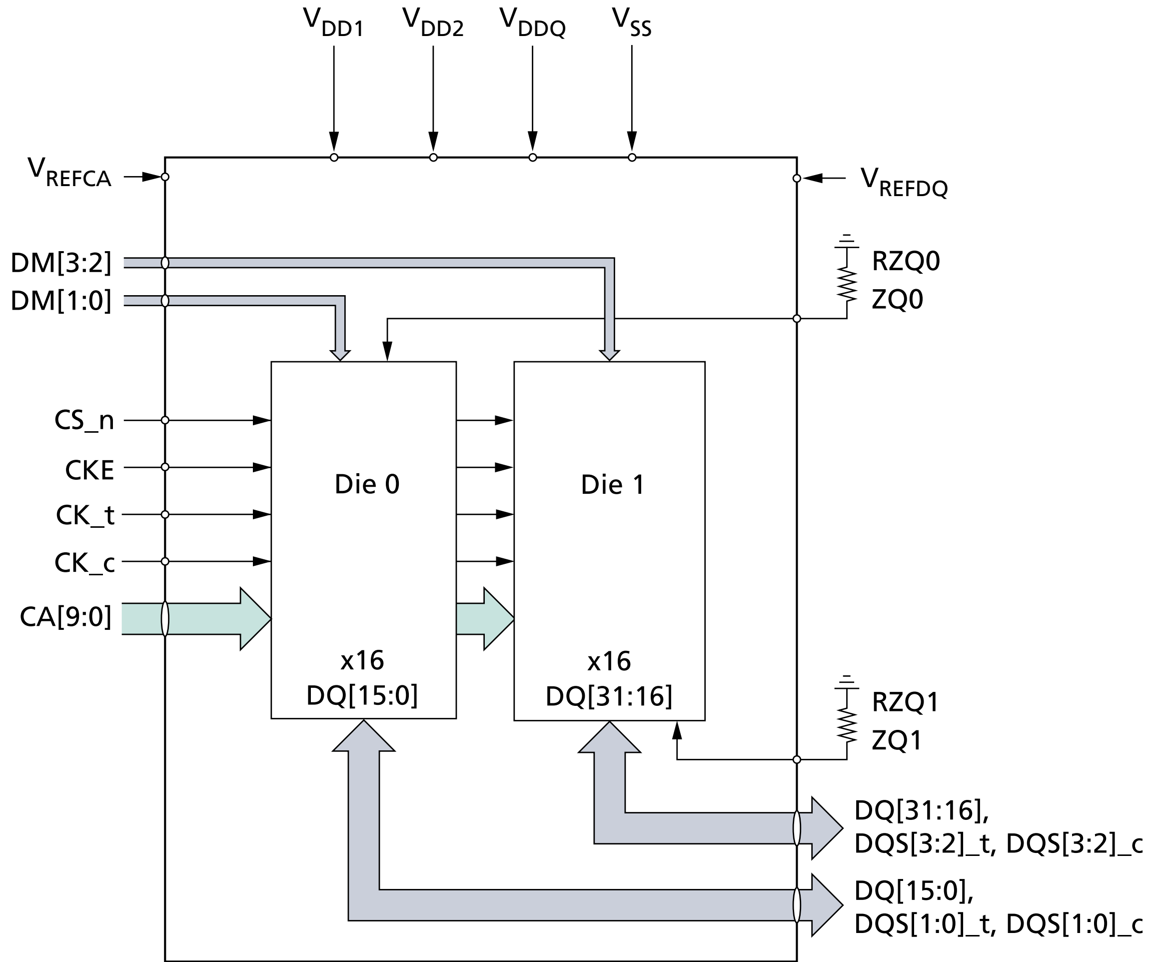
Package Block Diagrams

Figure 3: Single-Rank, Dual-Die, Single-Channel Package Block Diagram



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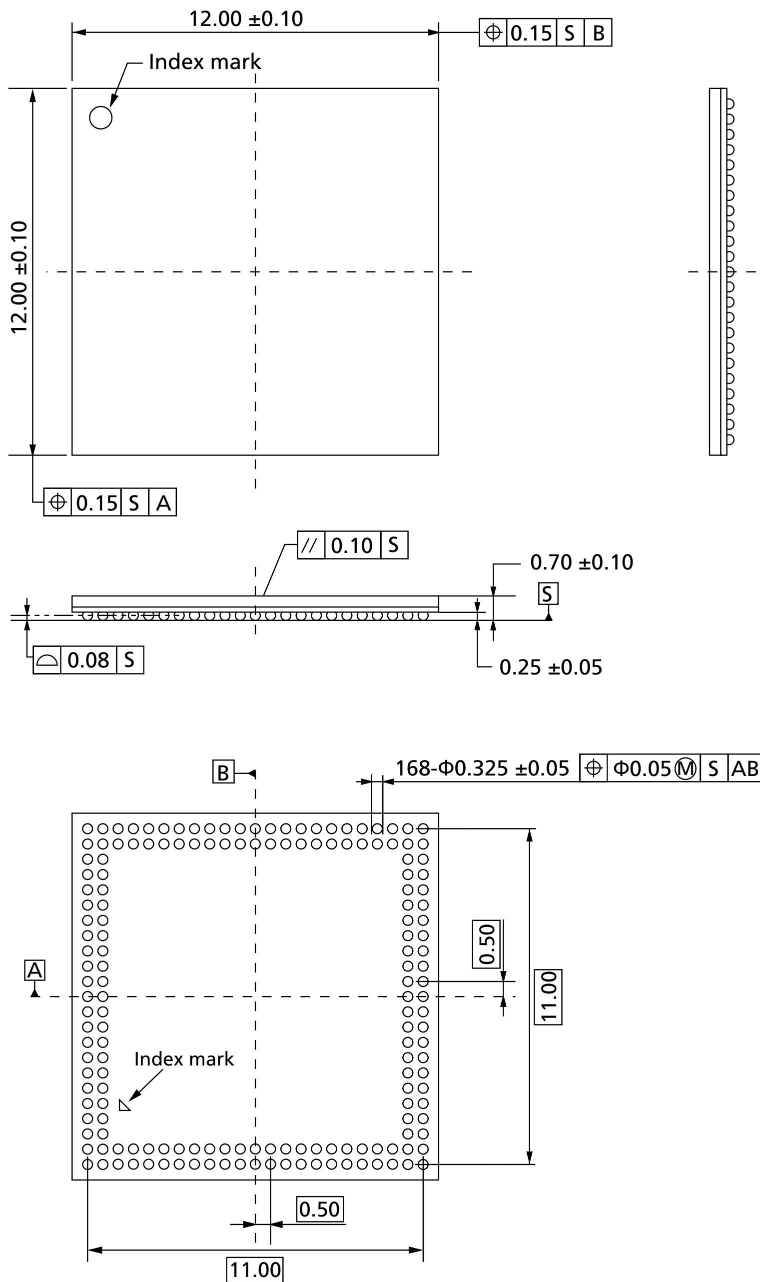
Package Dimensions

Figure 4: 168-Ball PoP FBGA (12mm x 12mm) – EDB8132B4PB-8D-F-D/R



Notes:
1. Package drawing: ECA-TS2-0515-02.
2. All dimensions are in millimeters.

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Revision History

Rev. B – 7/14

- Updated resistors in Package Block Diagram

Rev. A – 4/14

- Initial release

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This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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