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Intro to Memory Packaging

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Table of Contents

Introduction to Packaging - Goal and Objectives

Participants will learn the role packaging plays in semiconductor manufacturing, the diverse ecosystem and knowledge base required for a successful packaging team, and industry trends in packaging.

Objectives:

1. Describe the different types of packaging technology used in semiconductor memory
2. Explain the purpose of packaging in semiconductor memory technology
3. Explain challenges in semiconductor packaging as technology scales
4. Describe lab testing performed on packaging
5. Understand the importance of a diverse ecosystem and knowledge base for a successful packaging team

Target Audience

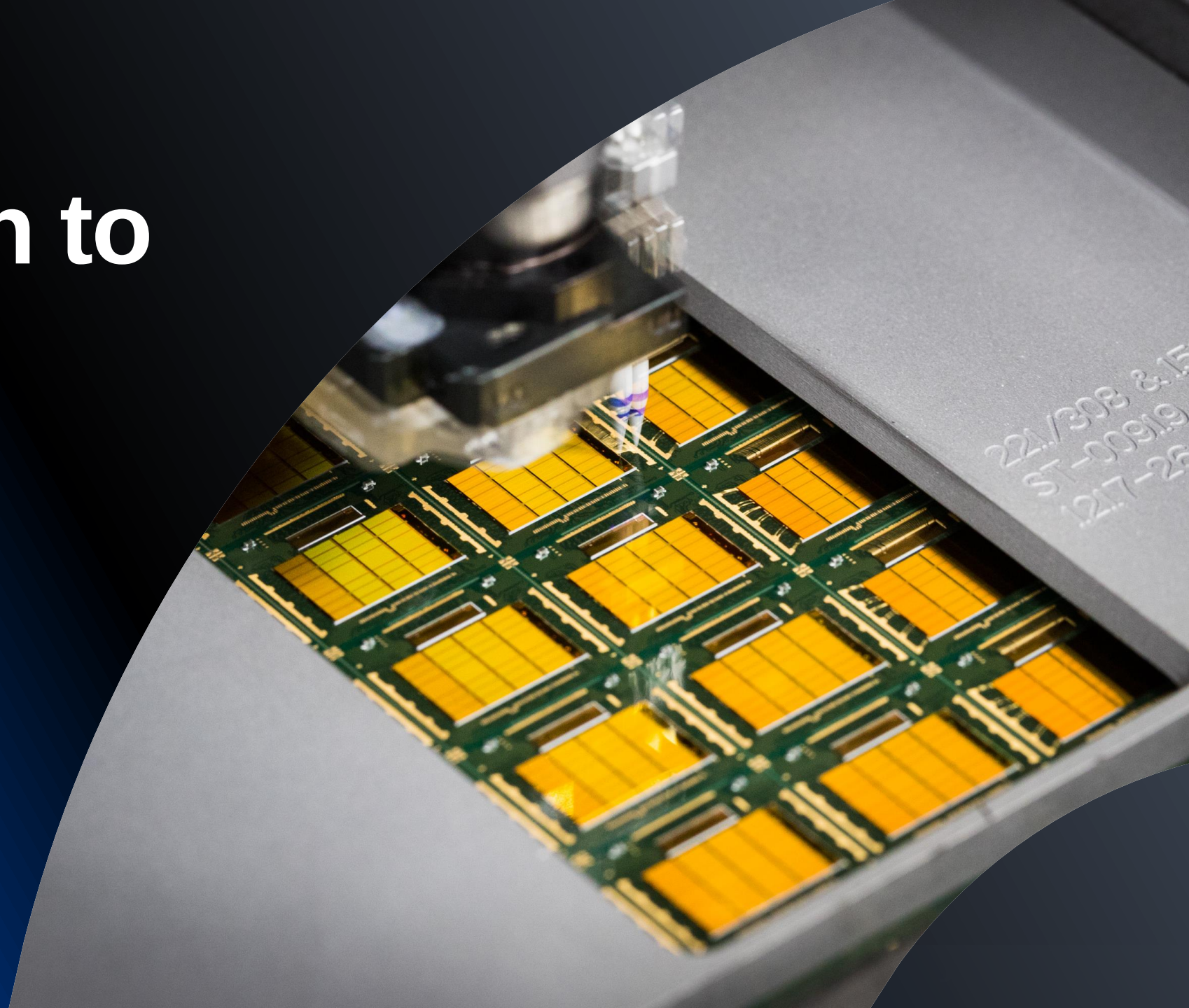
- This Introduction to Packaging module covers the basics of Semiconductor packaging.
- Interns, NCGs (New College Grads), and new employees in technical roles need to understand these concepts
- Examples of critical target audience roles at Micron that utilize these concepts:
  - Packaging Engineer
  - Packaging Integration Engineer
  - Packaging Operations Engineer
  - Packaging Equipment Engineer
  - Process Technicians
  - Equipment Technicians
  - Process Engineer
  - Equipment Engineer
  - Process Integration Engineer
  - Product Engineer
  - Characterization Engineer
  - Yield Enhancement Engineer
  - Test Engineer
  - Probe Engineer
  - Reliability Engineer
  - Quality Engineer
  - Design Engineer
  - Verification Engineer

Pro tip

Everyone interviewing at Micron can use this presentation to prepare for the interview by learning foundational information about memory. Check out the candidate guides for Engineering, Technician and Business roles.

- Micron engineering candidate guide
- Micron technician candidate guide
- Micron business candidate guide

Introduction to Memory Packaging



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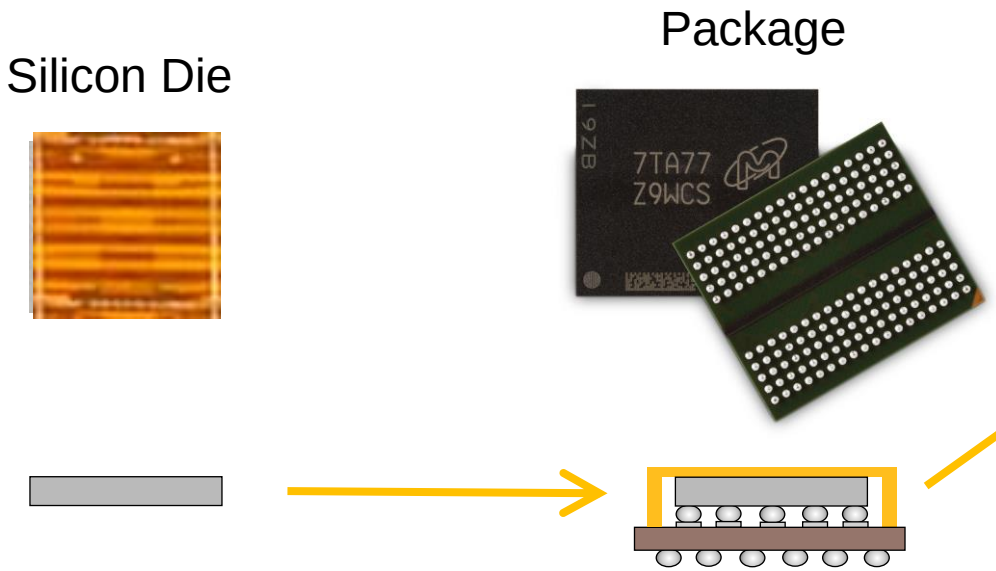
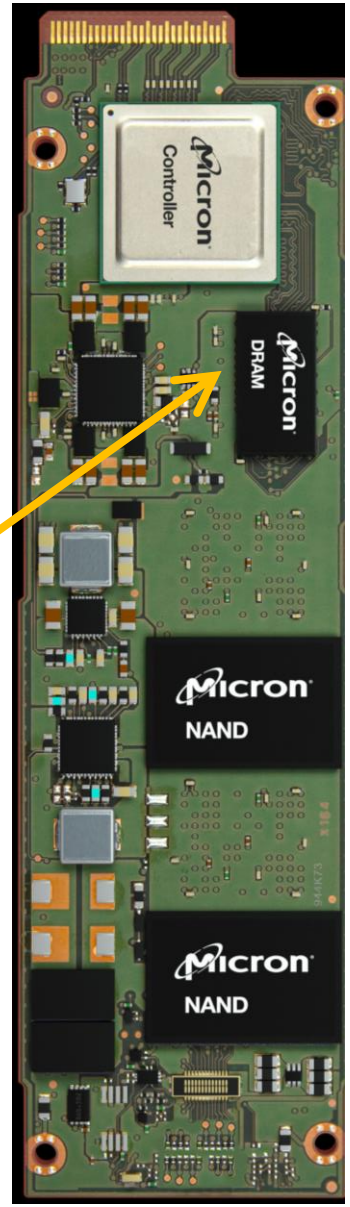
Introduction to Packaging

The semiconductor package is the components surrounding a memory die that enables its use in circuitry.





Circuit Board

Semiconductor Memory Manufacturing Flow

Start Material: Silicon is purified and formed into wafers (outside Micron).

Wafer-Level Fabrication: Electronic devices (transistors, resistors, capacitors, etc.) are fabricated on the silicon wafers, and are then interconnected together into complete circuits.

Probe: Each die is tested for functionality, failing die are flagged. Failure data (bins) is collected for yield improvement.
Param: Wafer-level electrical data is collected to characterize and improve the process.

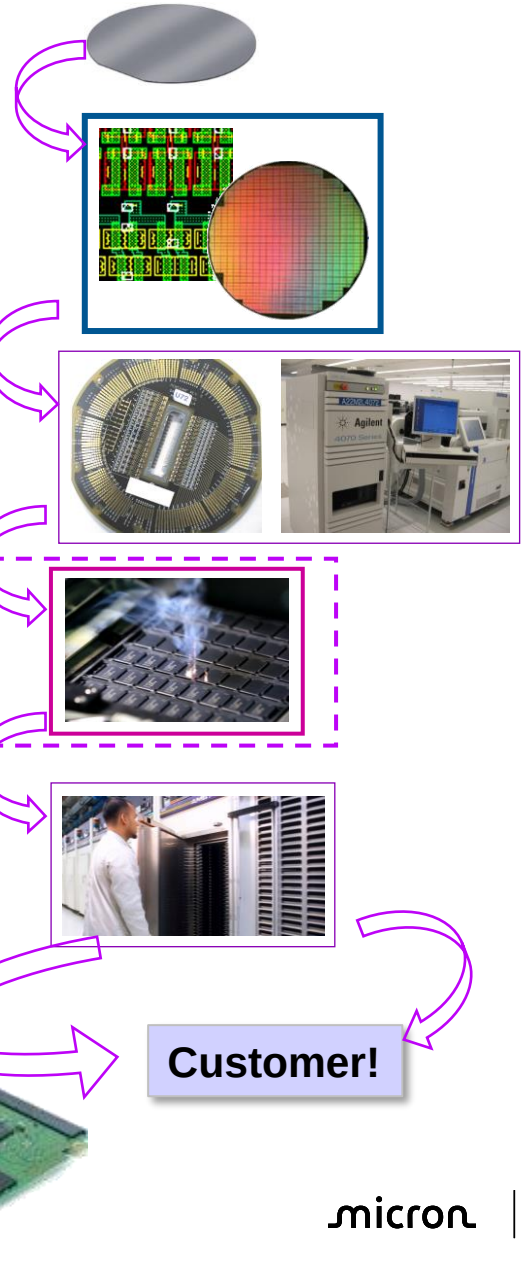
This document focuses on this part

Packaging: Die that pass Probe are separated from the wafer and assembled into packages.

Final Test and Burn-In: Packaged parts are tested for functionality. Some parts are given additional tests under harsh conditions to verify

Module Assembly and Testing: Some DRAM packaged parts are placed into modules and further tested for functionality and reliability.

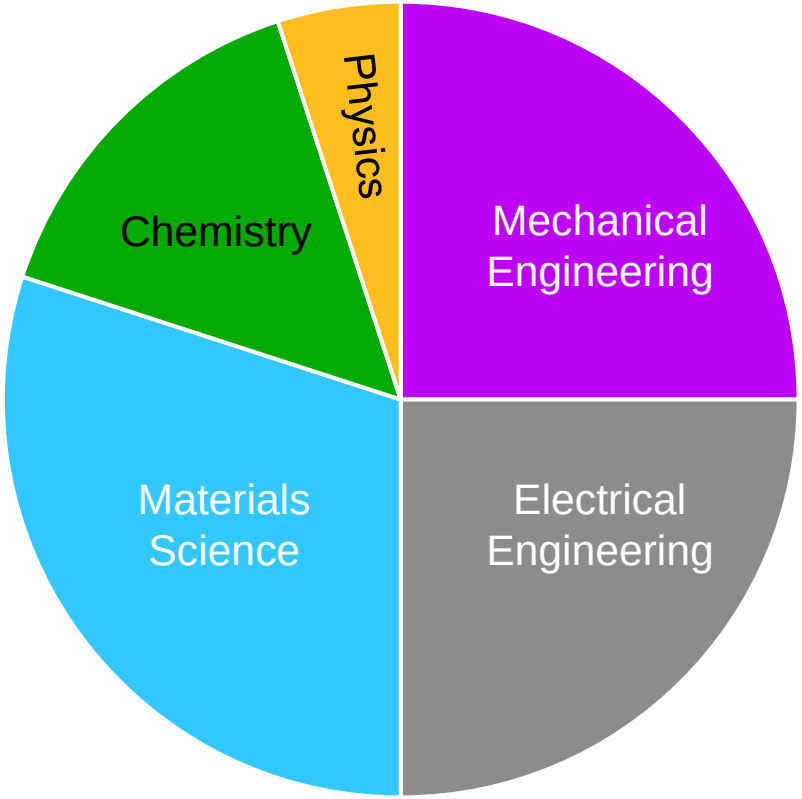
System/SSD Testing: NAND packaged parts may be placed into SSDs or Composite drives and further tested for performance.



What goes into making Semiconductor Packages?

Silicon integrated circuits

Metal plated contacts



Underfill mold compounds and epoxies

Bonding physics and chemistry

Solder bumps

Additional Tasks

Very diverse ecosystem and knowledge base to develop and deploy semiconductor packaging!

Engineering Disciplines in Packaging

Tackling challenges in packaging requires a diverse educational background

- Mechanical Engineering: Evaluate package warpage, mechanical integrity, thermal characterization.
- Electrical Engineering: Design and evaluate electrical routing of die and interposers in the package.
- Materials Science: Chemistry, metallurgy, and innovations in material science drive many of the advancements in semiconductor technology.
- Industrial Engineering: Evaluating, procuring, and integrating new tools and processes to enable tighter tolerance manufacturing at continually shrinking scales.

Introduction to Packaging

A) Silicon Die
- Semiconductor Memory

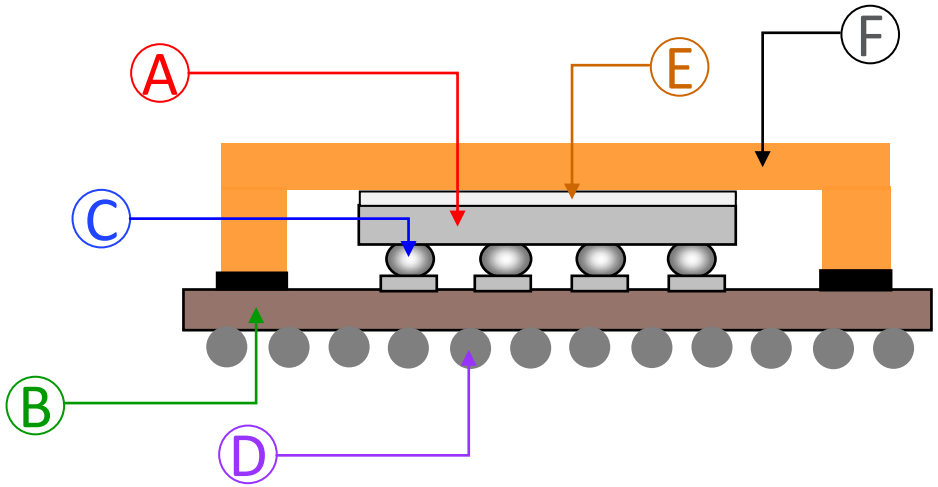
B) Interposer
- Die support
- Embedded interconnects

C) Secondary (die-to-package) Interconnects
- Wire bonds, bumps, or pillars

D) Primary (package-to-board) Interconnects
- Leads or solder balls

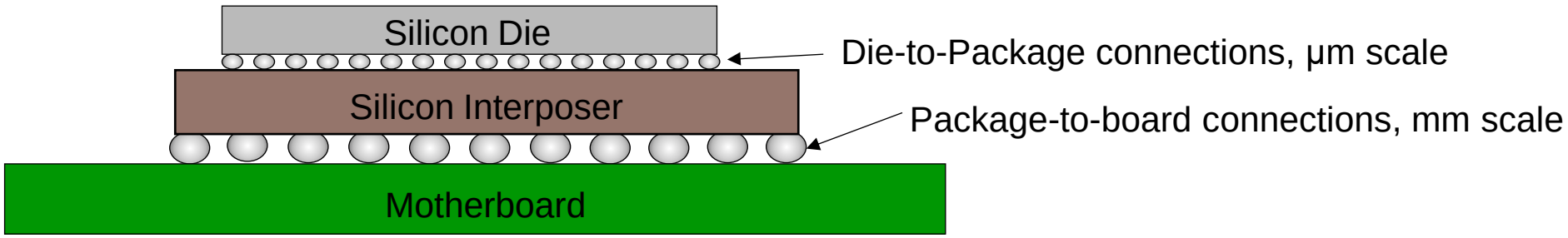
E) Heat Dissipation
- Heat sinks/spreaders
- Thermal Interface Materials

F) Environmental Protection
- Plastic/ epoxy seal
- Ceramic/ metal lid



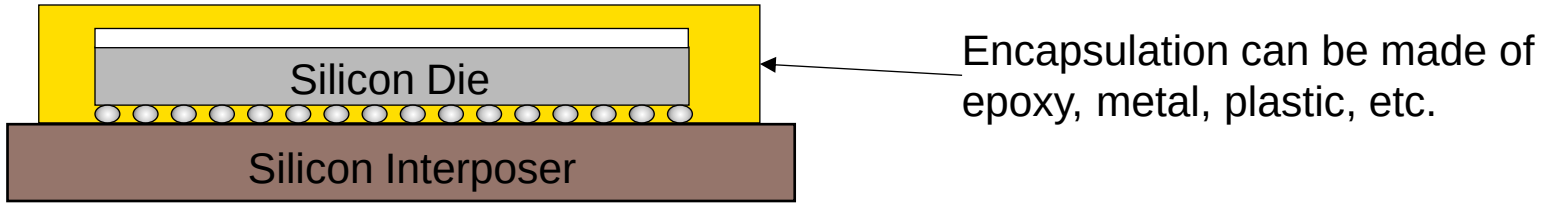
Purpose of Packaging

1. Electrical interface between the chip and outer circuitry:
    - Can “adapt” between the different scale size of metal connections on the die to wires on circuit.
    - Improves the quality of signal transmission.



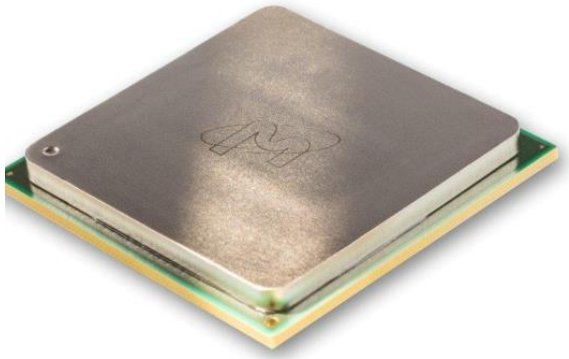
Purpose of Packaging

2. Physical protection of die:
   - Thinly diced silicon die are fragile and susceptible to mechanical stresses and environmental contamination.



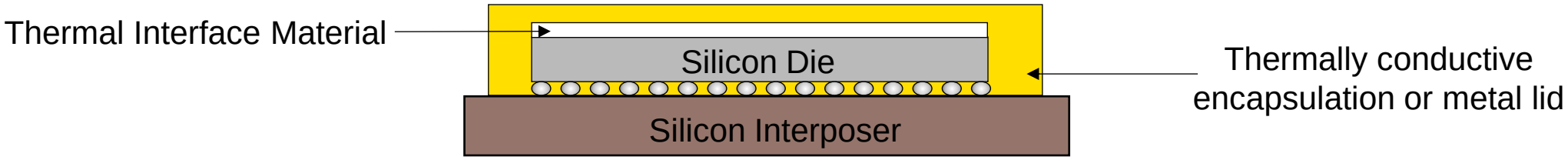
Plastic Encapsulation: Injection molding process encases the assembled die in rigid plastic.

Metal Lid: Assembled die is sealed under a metal lid.

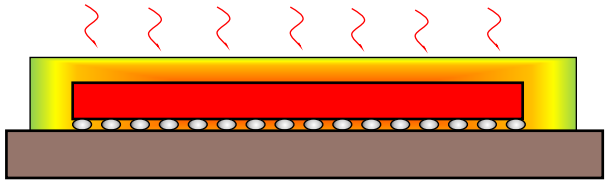


Purpose of Packaging

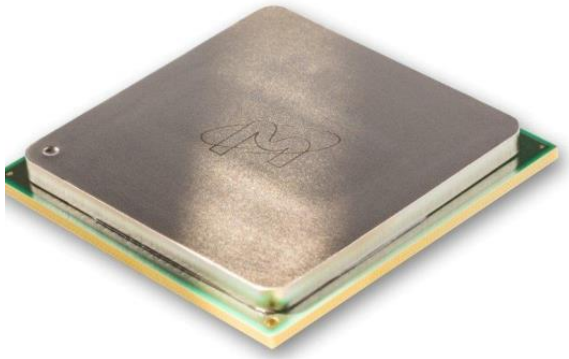
3. Heat dissipation:
   - Complex integrated circuits produce a lot of heat that can burn up a die without the heat dissipation of the package.



Thermally Conductive Fillers: Thermally conductive encapsulation materials can help conduct heat away from the die.



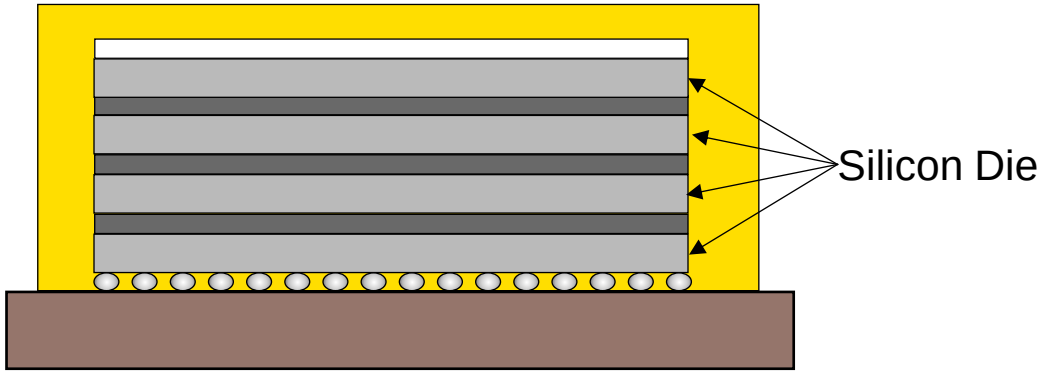
Heat Spreader: Metal lids can also effectively spread heat across a greater surface area.



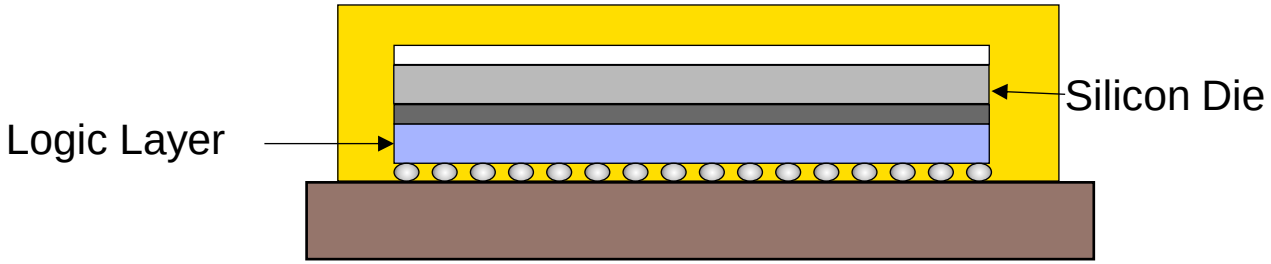
Purpose of Packaging

4. Expand functionality:
    - Stack die to multiply the available memory.
    - Increase functionality by including logic or different types of memory.

Multi-die Package

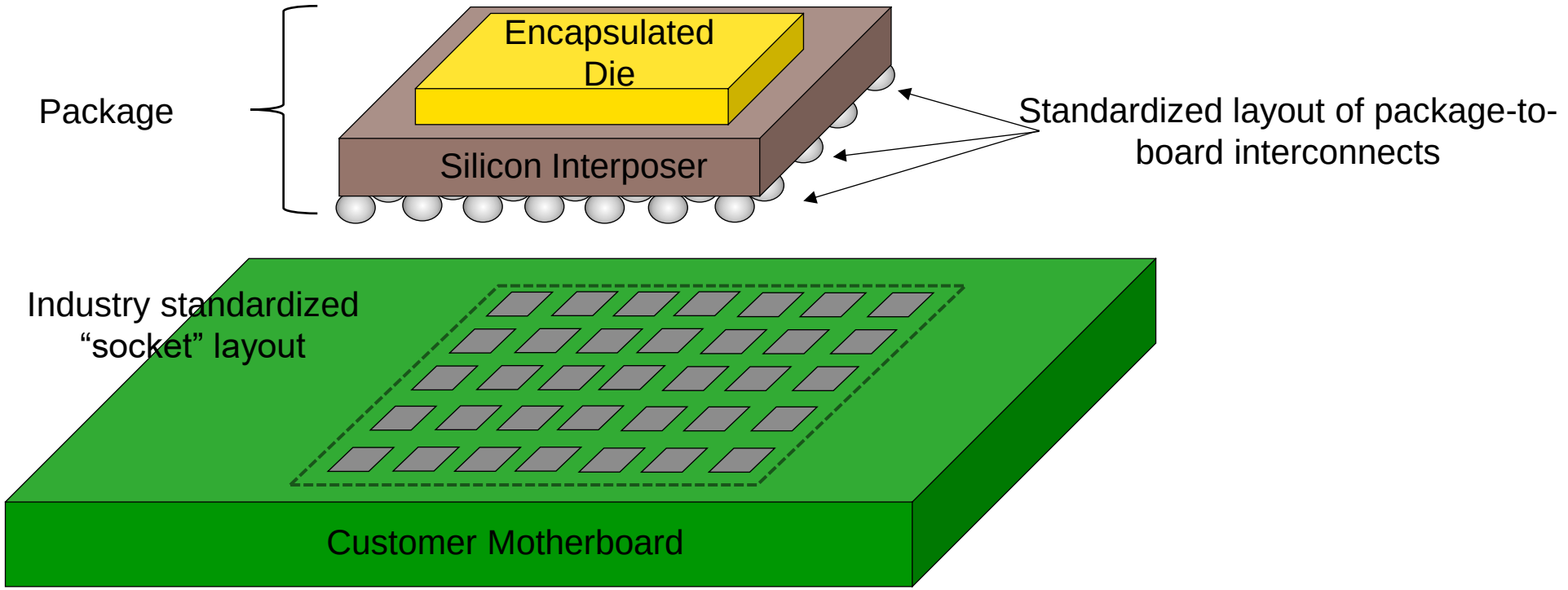


Hybrid Memory



Purpose of Packaging

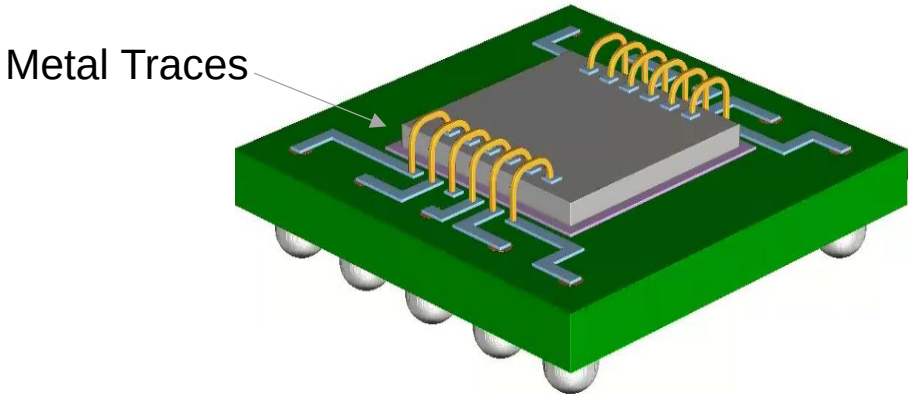
5. Customer ease of use:
    - Standardized sockets allow for quick attachment, replacement, or upgrade of products.



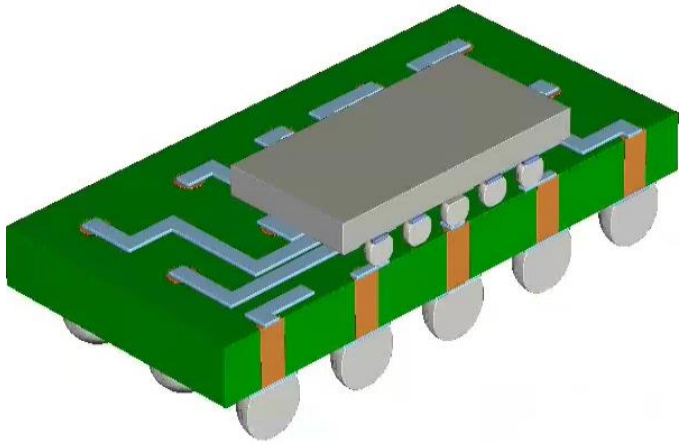
Introduction to Packaging

In the process of fabricating die, chemical and laser etchings expose connections on the top of die. To make an electrical connection, wires can be bonded to these connections on the top, or the die can be inverted (“flipped”) to apply bonds to the bottom.

Wire bond: Very thin wires (usually gold) connect bond pads on the die to metal traces on the interposer. Over 80% of integrated circuits use wire bond.



Flip Chip: Die is inverted. Solder balls on the die are directly bonded to metal pads on the package substrate.

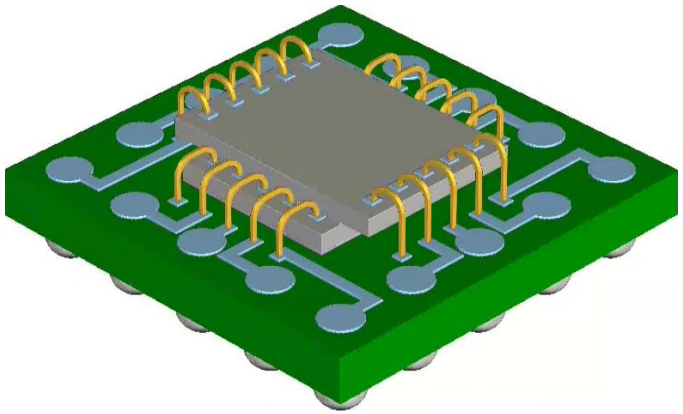


Wire bonded Package

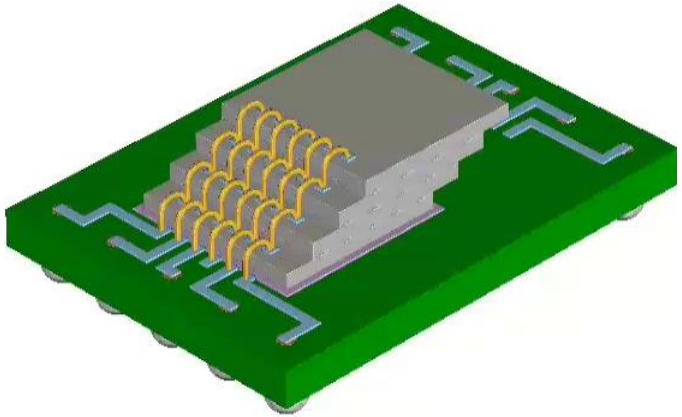
Utilize wires bonded to pads on the top of the die down to pads on the substrate.

- Cheaper, easier fabrication process.
- Adaptable to different chip sizes and other package design considerations.
- Requires a larger overall package.
- Long wires result in greater parasitic voltage loss, slower signal transmission.

Wire bond – Direct: Wire bond is used to connect each die directly to the assembly substrate.



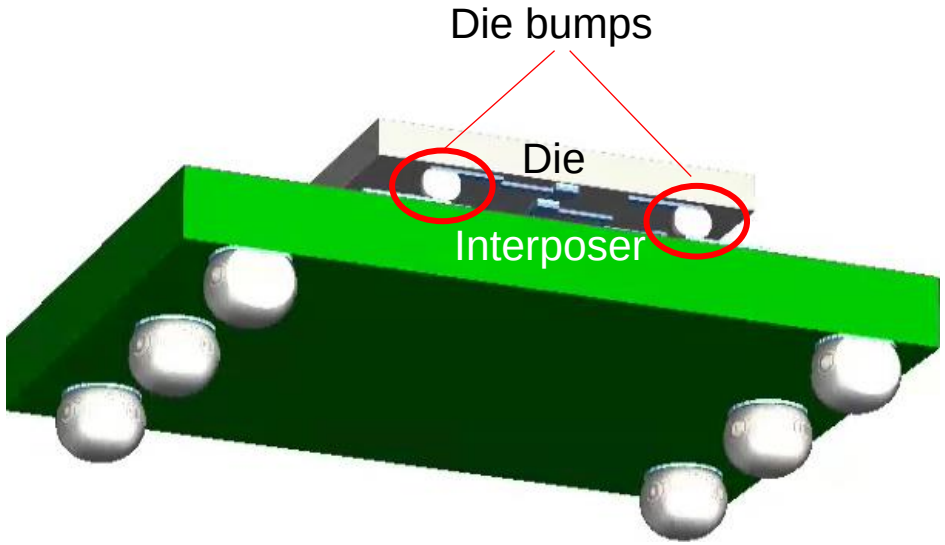
Wire bond - Cascading: Wire bonds cascade from one die to the next, ending at the substrate.

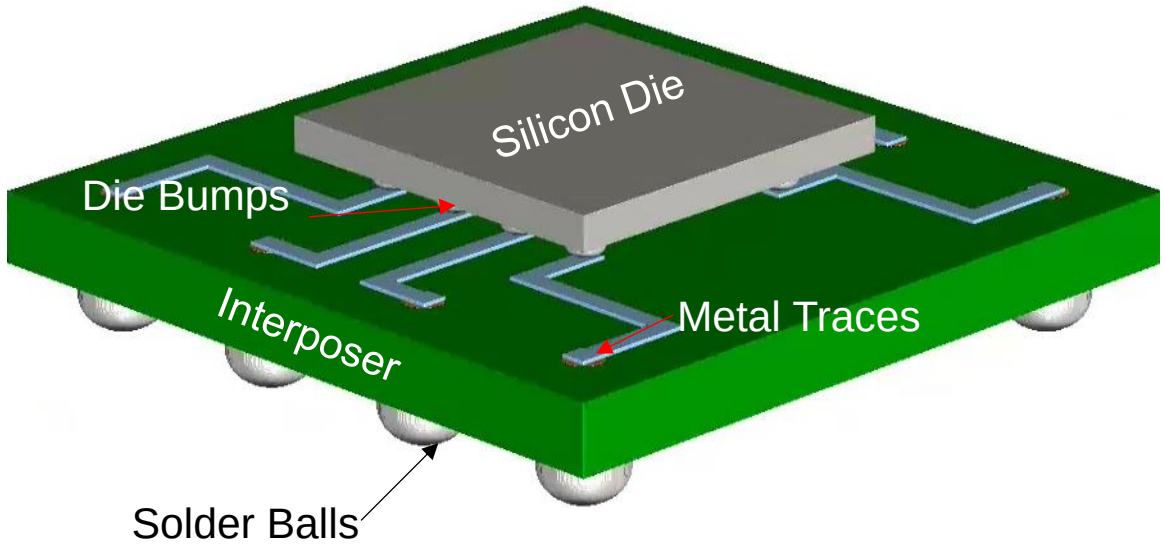


Bumped Package

Solder ball “bumps” make electrical connections between metal pads on bonding surfaces.

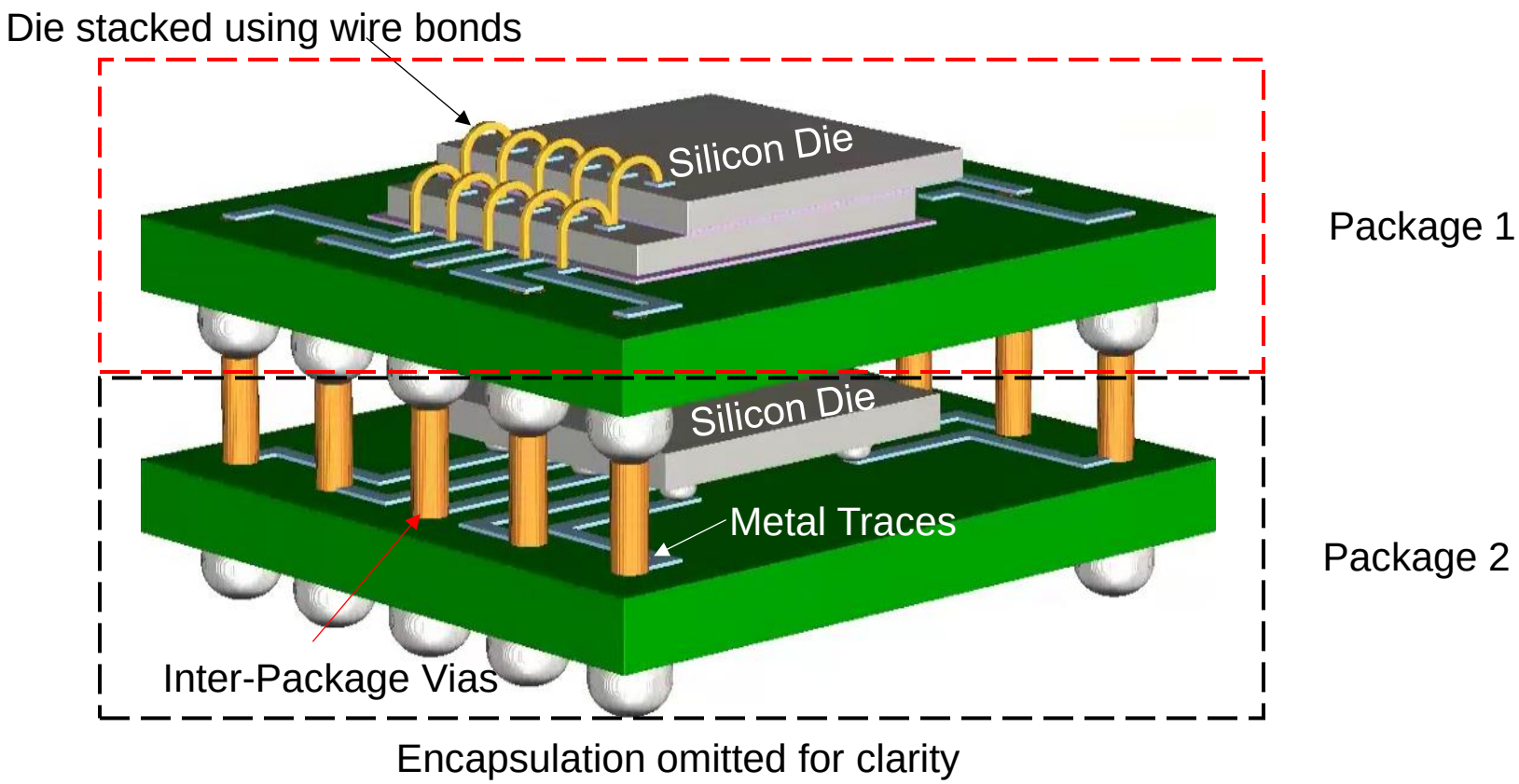
- More complex fabrication process, increased cost compared to wire bonds.
- Changes to chip size and other package designs often require re-designing the bonding pattern.
- Small electrical connections result in far lower parasitic voltage loss.
- Enables high density interconnects and shrinks overall package size.





Package-on-Package

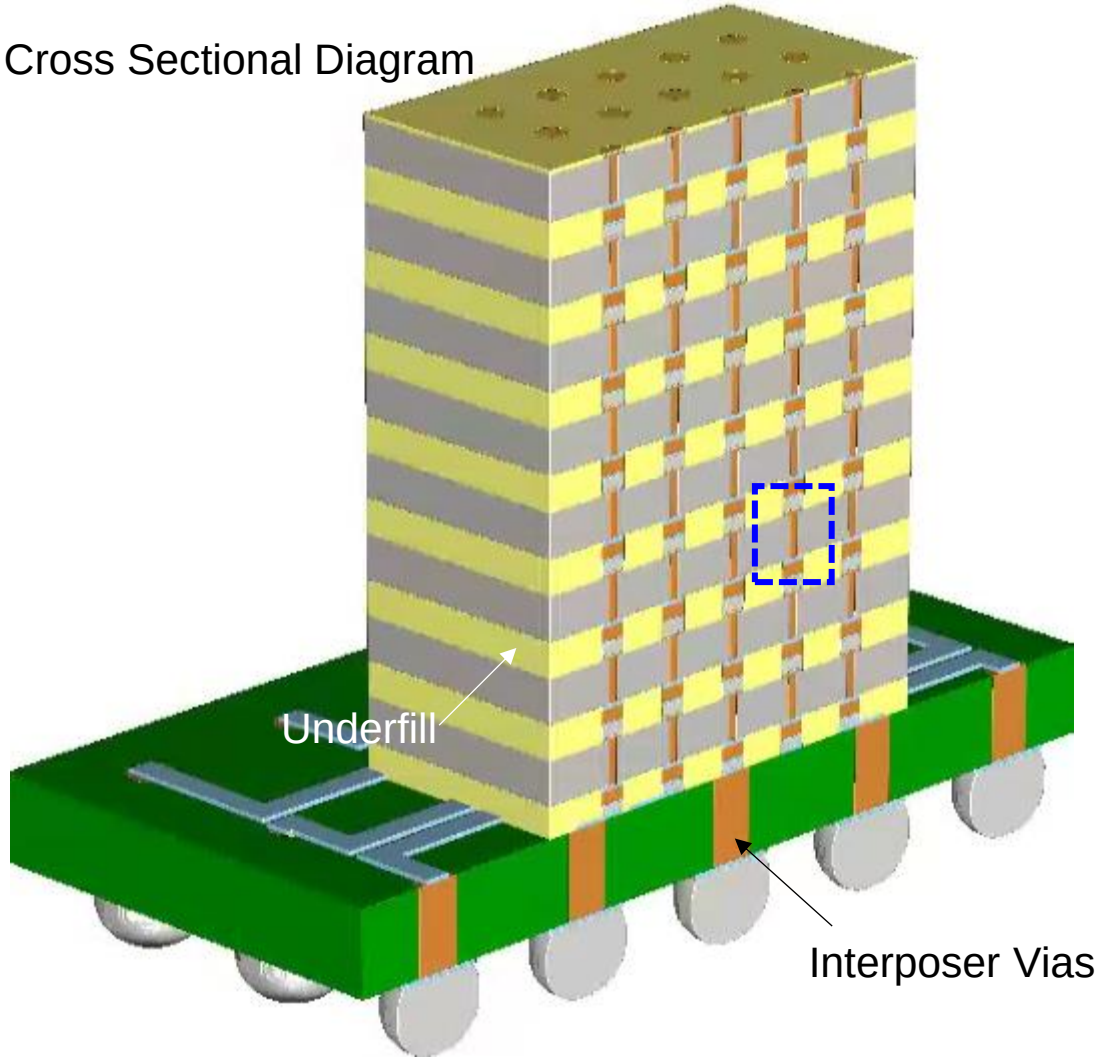
“Bumped” die are not easily stacked. Can expand memory then by stacking entire packages. Enables blended bonding types as well.

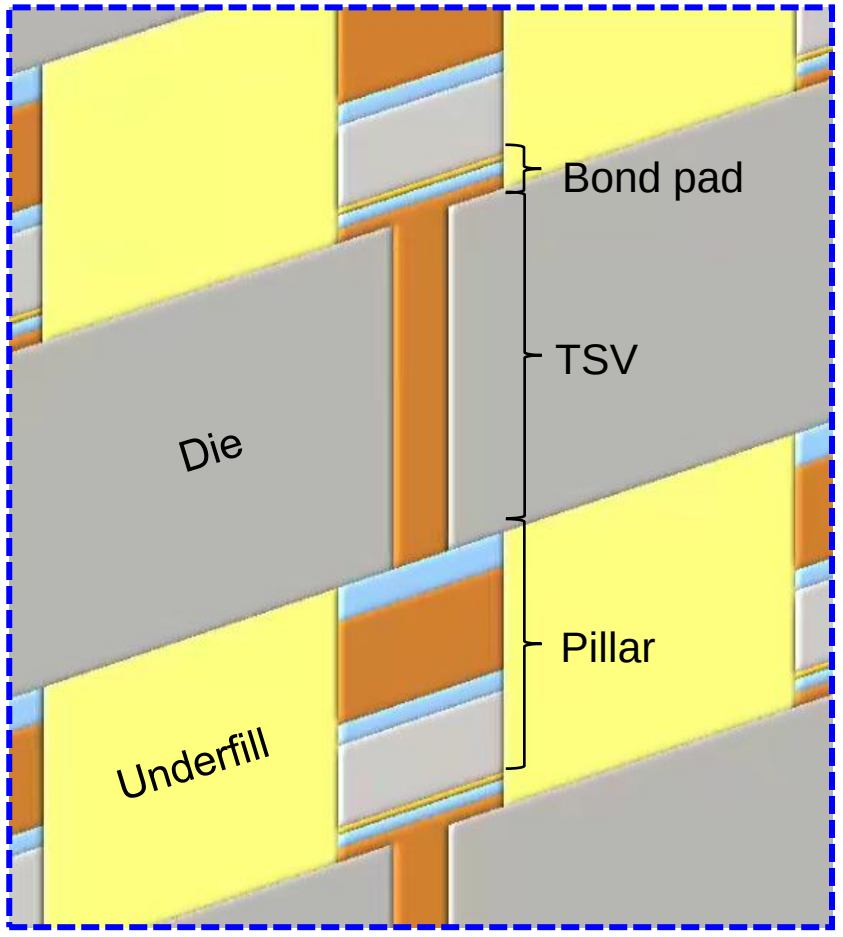


Through Silicon Vias (TSV's)

Newer fabrication technique runs metal pillars or "vias" through the thickness of the die. Electrically connects the die and bonds to the interposer.

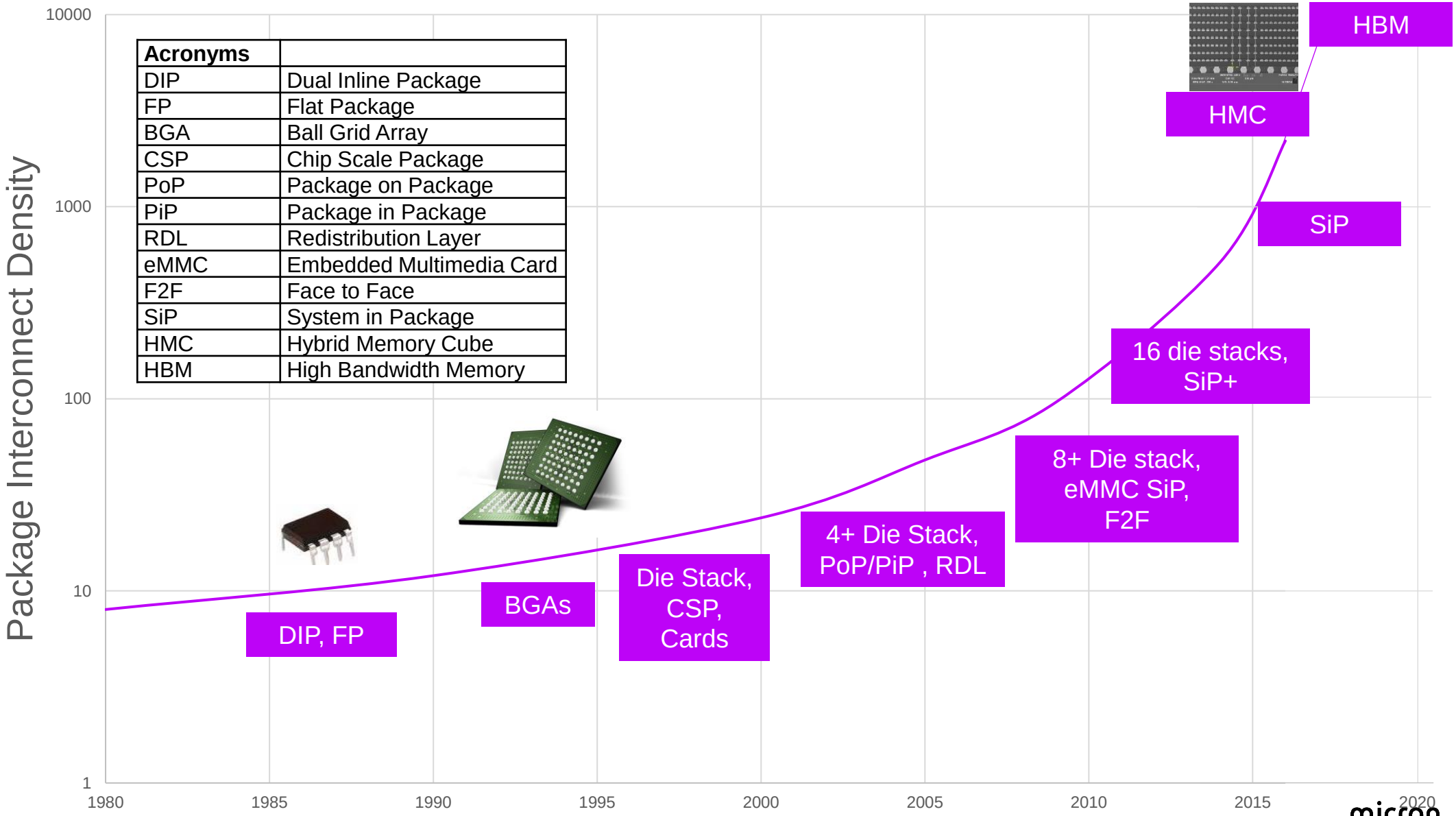
Cross Sectional Diagram





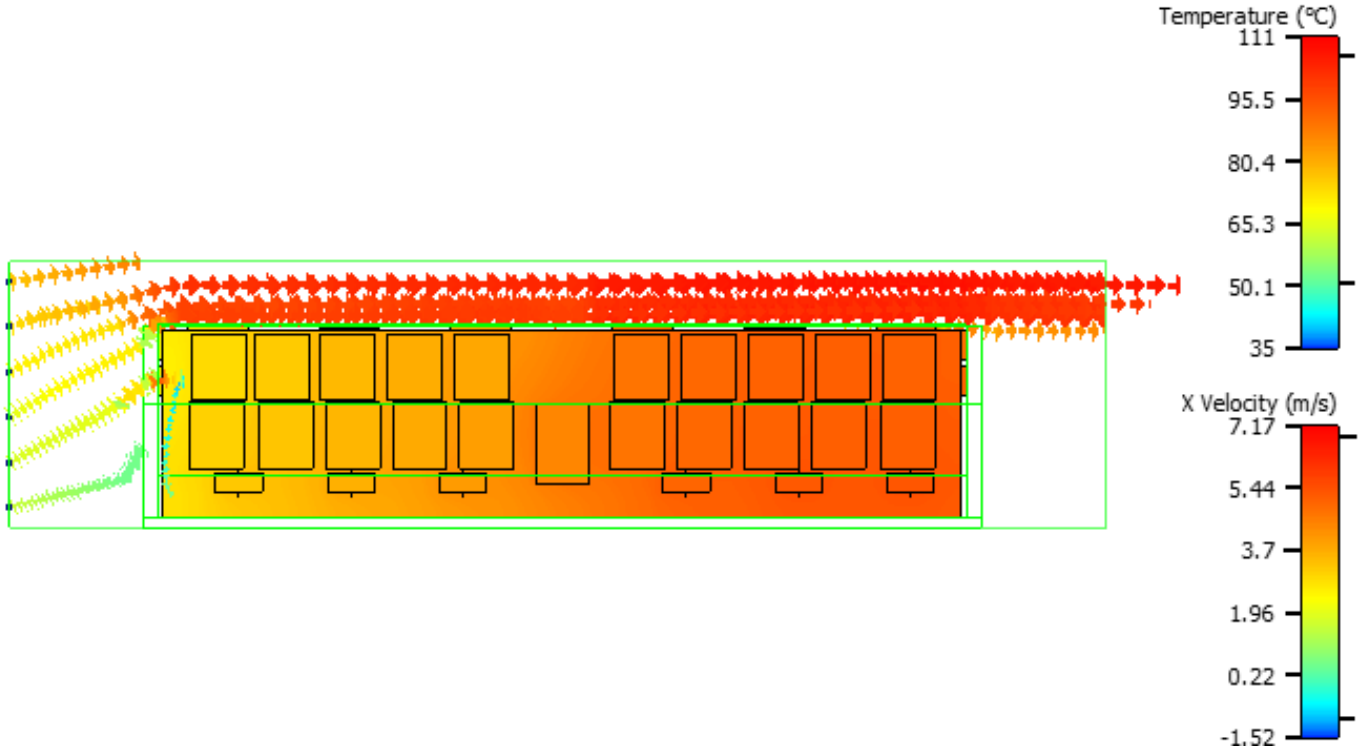
Challenges in Packaging: Scaling!

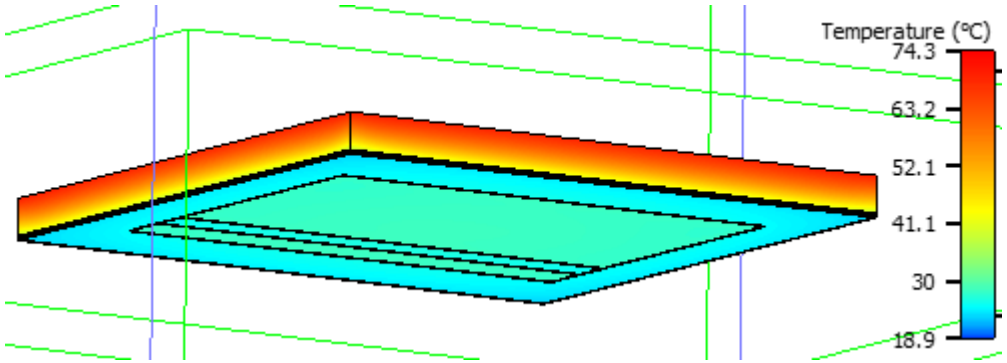
Acronyms	
DIP	Dual Inline Package
FP	Flat Package
BGA	Ball Grid Array
CSP	Chip Scale Package
PoP	Package on Package
PiP	Package in Package
RDL	Redistribution Layer
eMMC	Embedded Multimedia Card
F2F	Face to Face
SiP	System in Package
HMC	Hybrid Memory Cube
HBM	High Bandwidth Memory



Thermal Simulation

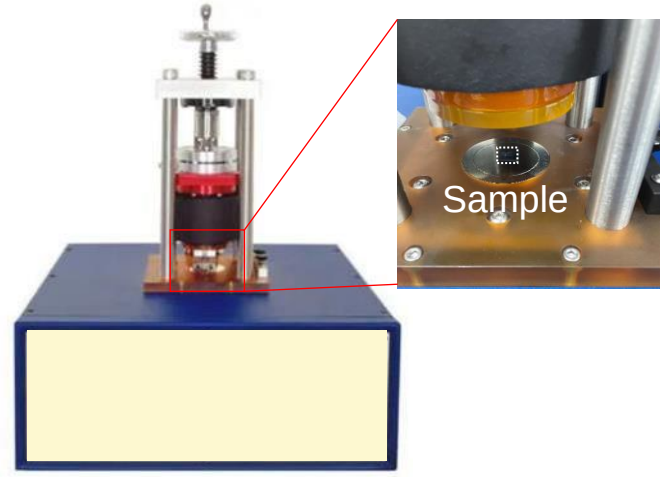
Thermal modeling is a powerful tool for predicting how packages will perform while in different situations.

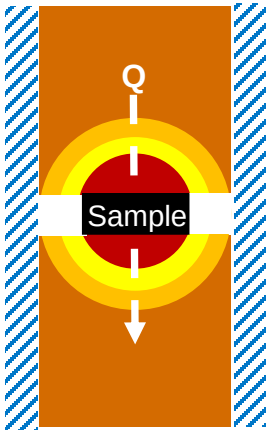




Laboratory Testing

Computer simulations require comparison to experimental data for validation.



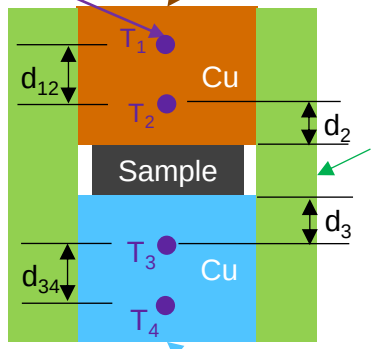


Four locations
In Cu blocks

Heat Source Power (P)

$$T_T = T_2 - \frac{d_2}{d_{12}}(T_1 - T_2)$$

$$T_B = T_3 + \frac{d_3}{d_{34}}(T_3 - T_4)$$



Insulators

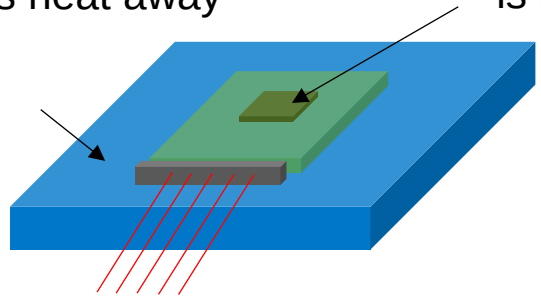
Isothermal
Heat sink: 0°C

$$\theta_{TB} = \frac{(T_T - T_B)}{P}$$

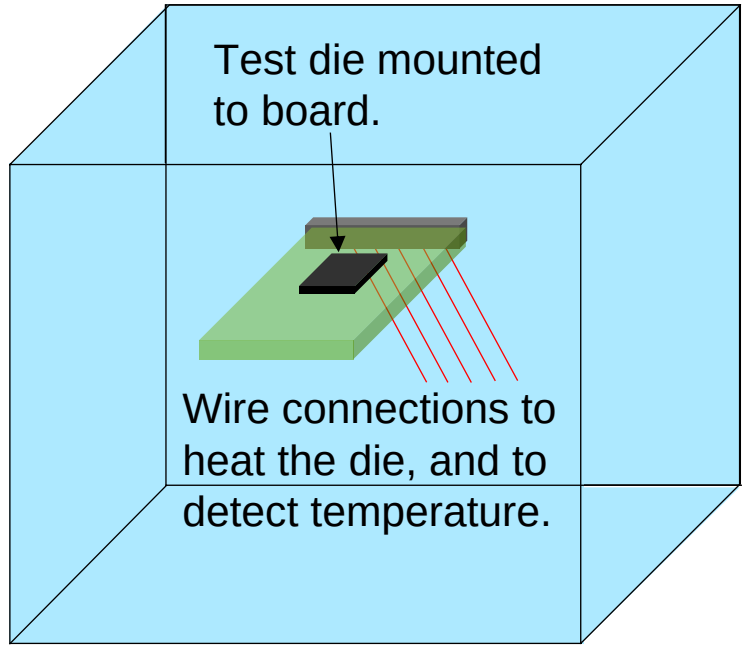
Laboratory Testing Environments

Cold plate (20 C). Conducts heat away from die.

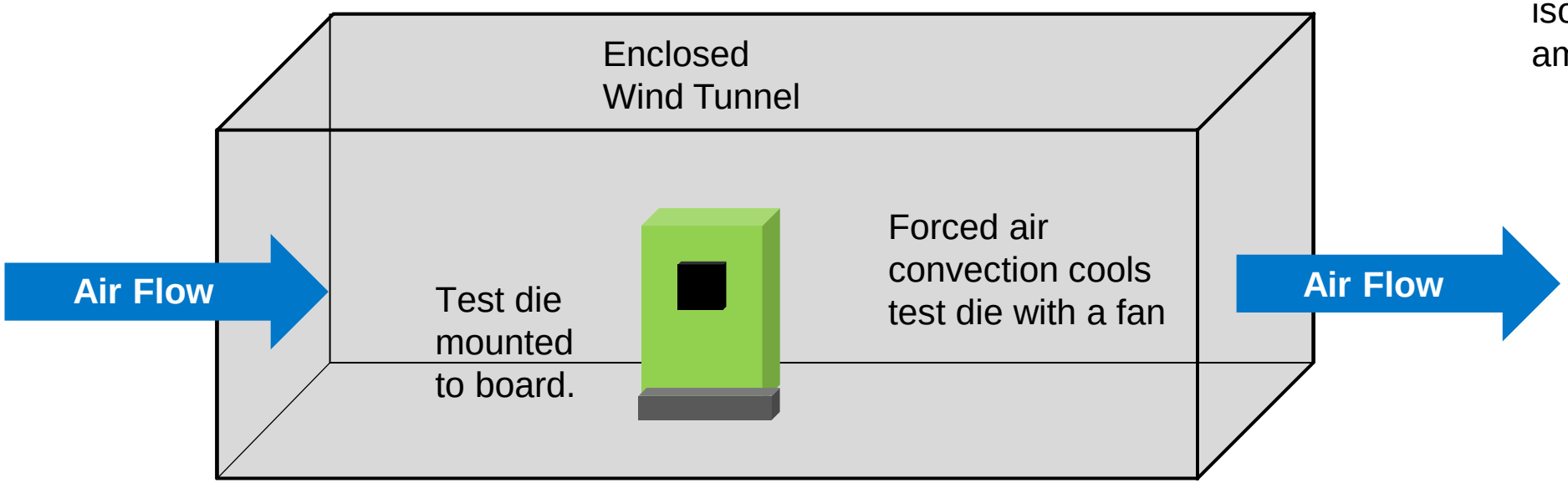
Test die mounted to board. Die is in contact with cold plate.



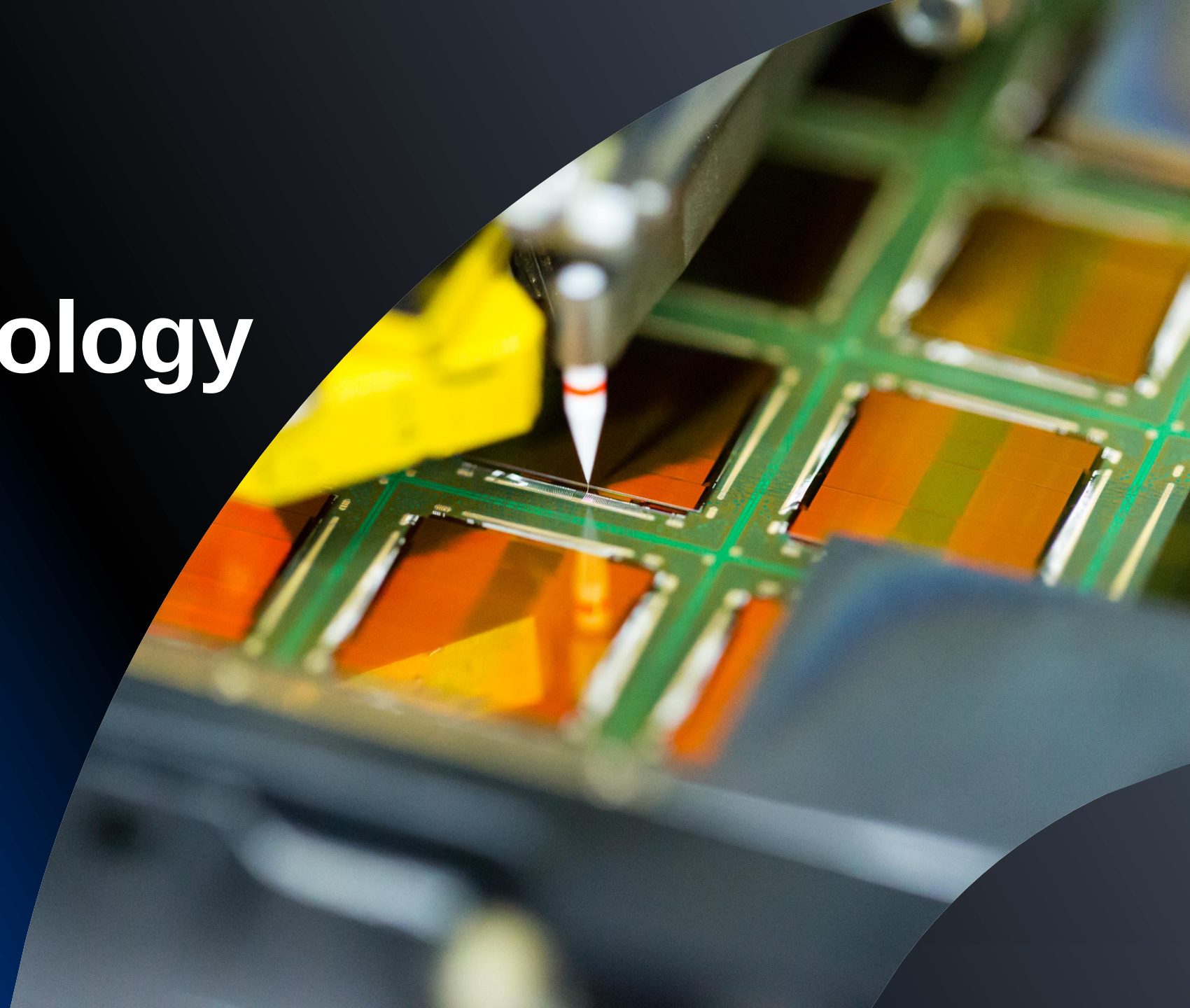
Wire connections to heat the die, and to detect temperature.



Acrylic chamber to isolate test die from ambient air flow.



Key Terminology Glossary



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Glossary

Term or acronym	Definition/description
BGA	Ball Grid Array. Package type that utilizes an array of solder balls for electrical connection.
Bumped Package	A package that uses solder ball "bumps" to make electrical connections between metal pads on bonding surfaces.
CSP	Chip Scale Package. Package type where the finished package is not more than 1.1x the die size (almost the same size as the die).
DIP	Dual Inline Package. Package type consisting of two parallel rows of pins.
eMMC	Managed Memory Chip. An MCP (Multi-Chip Package) that includes a logic controller and one or more memory die.
F2F	Face to Face. Package type consisting of two die mounted face to face and connected together via bumps.
FP	Flat Package. A package with leads parallel to base plane attached on two opposing sides of the package periphery.
HBM	High Bandwidth Memory. Multi DRAM memory package that uses 3D Stacking (vertical stacking of DRAM die utilizing TSVs and 3D Interconnects).
HMC	Hybrid Memory Cube. This is a type of high-performance memory that uses a 3D architecture. Multi-Chip Package (MCP) where two or more DRAM die are stacked directly on top of a logic chip.
Interposer	Base that the die is mounted to in the package. Usually includes die-package interconnects.

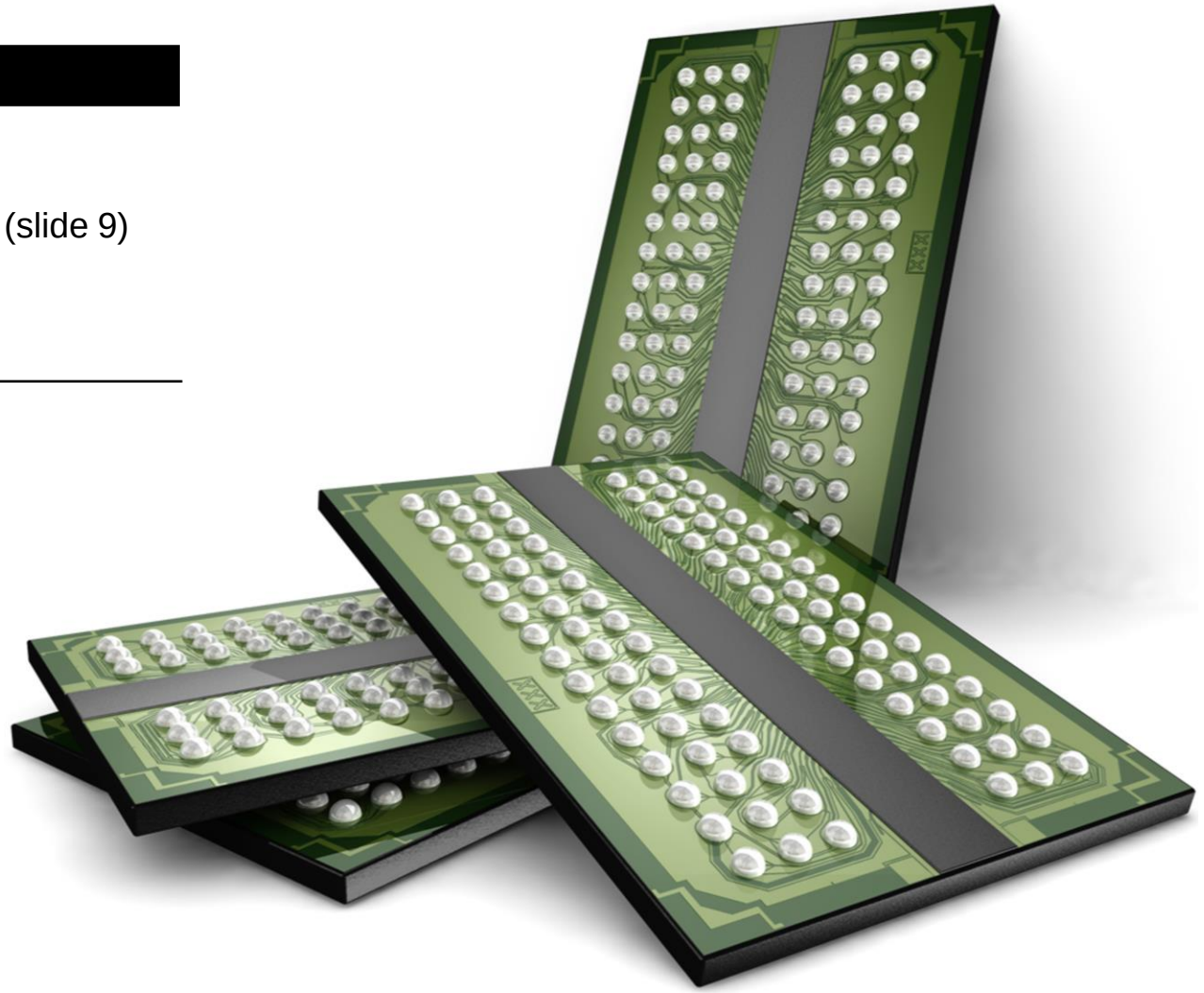
Glossary

Term or acronym	Definition/description
PiP	Package in Package. Two or more intermediate substrates, with die stacks on each, stacked and encapsulated into a single package
PoP	Package on Package. A method of stacking entire packages to expand memory. Two or more completed packages that are electrically connected together and behave as a single unit.
RDL	Redistribution Layer. Additional interconnect layer(s) that resolve a mismatch between die and package interconnects.
Silicon Die	The small piece of silicon that contains the integrated circuit. Silicon die is fragile and needs to be packaged.
SiP	System in a Package. A complete system of interconnected die in one package.
TSVs	Through Silicon Vias. Metal pillars or "vias" that run through the thickness of the silicon die to electrically connect the die and bonds to the interposer.
Wirebond	The packaging operation where very thin wires (usually gold) are used to make connections between the die bond pads and the package interconnects.

Document Updates

Document Updates

Date	Description
January 2025	• Added goals and objectives (slide 5) • Added target audience (slide 6) • Added semiconductor memory manufacturing flow (slide 9) • Added several new images • Added acronym legends • Added glossary section (slide 28-30)



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