Micron Educator Hub

Intro to Photolithography

Reviewed 2025

Copyright guidelines

By using any content provided by the Micron Educator Hub, you acknowledge that Micron Technology, Inc. ("Micron") is the sole owner of the content and agree that any use of the content provided by the Micron Educator Hub must comply with applicable laws and require strict compliance with these Guidelines:

1. Credit shall be expressly stated by you to Micron for use of the content, including any portion thereof, as follows:
    a. "*© 2009-2025 Micron Technology, Inc. All Rights Reserved. Used with permission.*"
2. You may not use the content in any way or manner other than for educational purposes.
3. You may not modify the content without approval by Micron.
4. You may not use the content in a manner which disparages or is critical of Micron, its employees, or Micron's products/services.
5. Permission to use the content may be canceled/terminated by Micron at any time upon written notice from Micron to You if You fail to comply with the terms herein.
6. You acknowledge and agree that the content is provided by Micron to You on an "as is" basis without any representations or warranties whatsoever, and that Micron shall have no liability whatsoever arising from Your use of the content. Micron shall ensure that the content does not violate any statutory provisions and that no rights of third parties are infringed by the content or its publication. Otherwise, liability of the parties shall be limited to intent and gross negligence.
7. You acknowledge and agree that the content is the copyrighted material of Micron and that the granting of permission by Micron to You as provided for herein constitutes the granting by Micron to You of a non-exclusive license to use the content strictly as provided for herein and shall in no way restrict or affect Micron's rights in and/or to the content, including without limitation any publication or use of the content by Micron or others authorized by Micron.
8. Except for the above permission, Micron reserves all rights not expressly granted, including without limitation any and all patent and trade secret rights. Except as expressly provided herein, nothing herein will be deemed to grant, by implication, estoppel, or otherwise, a license under any of Micron's other existing or future intellectual property rights.

How to cite sources from the Micron Educator Hub

- Micron is committed to collaborate with educators to make semiconductor memory education resources available through the Micron Educator Hub
- The content in the Micron Educator Hub has been identified by Micron as current and relevant to our company
- Please refer to the table on the right for proper citation

Use case	How to cite sources
Whole slide deck or whole document Description: User uses the whole slide deck or whole document AS IS, without any modification	No additional citation required
Full slide or full page Description: User incorporates a full slide or a full page into their own slide deck or document	"© 2009-2025 Micron Technology, Inc. All Rights Reserved. Used with permission."
Portion of a slide or portion of a page Description: User copies a portion of a slide or a portion of a page into a new slide or page	This is not allowed

Table of Contents

Intro to Photolithography – goal and objectives

Goal

- Provide a foundational understanding of Photolithography in the semiconductor memory industry and the role of the Photolithography Engineering team

Objectives

- State the purpose of the Photolithography process and how it fits into the overall semiconductor memory fabrication process flow
- Describe the fundamentals of the Photolithography process
- Describe the types of equipment used by Photolithography
- Define the primary measurements Photolithography uses to control the processes
- State common defectivity associated with Photolithography

Target Audience

- This Intro to Photolithography module covers the basics of semiconductor photolithography process.
- NCGs (New College Grads), and new employees in technical roles need to understand these concepts
- Examples of critical target audience roles at Micron that utilize these concepts:
  - Process Technicians
  - Equipment Technicians
  - Process Engineer
  - Equipment Engineer
  - Process Integration Engineer
  - Product Engineer
  - Characterization Engineer
  - Yield Enhancement Engineer
  - Test Engineer
  - Probe Engineer
  - Reliability Engineer
  - Quality Engineer

Pro tip

Everyone interviewing at Micron can use this presentation to prepare for the interview by learning foundational information about memory. Check out the candidate guides for Engineering, Technician and Business roles.

- Micron engineering candidate guide
- Micron technician candidate guide
- Micron business candidate guide

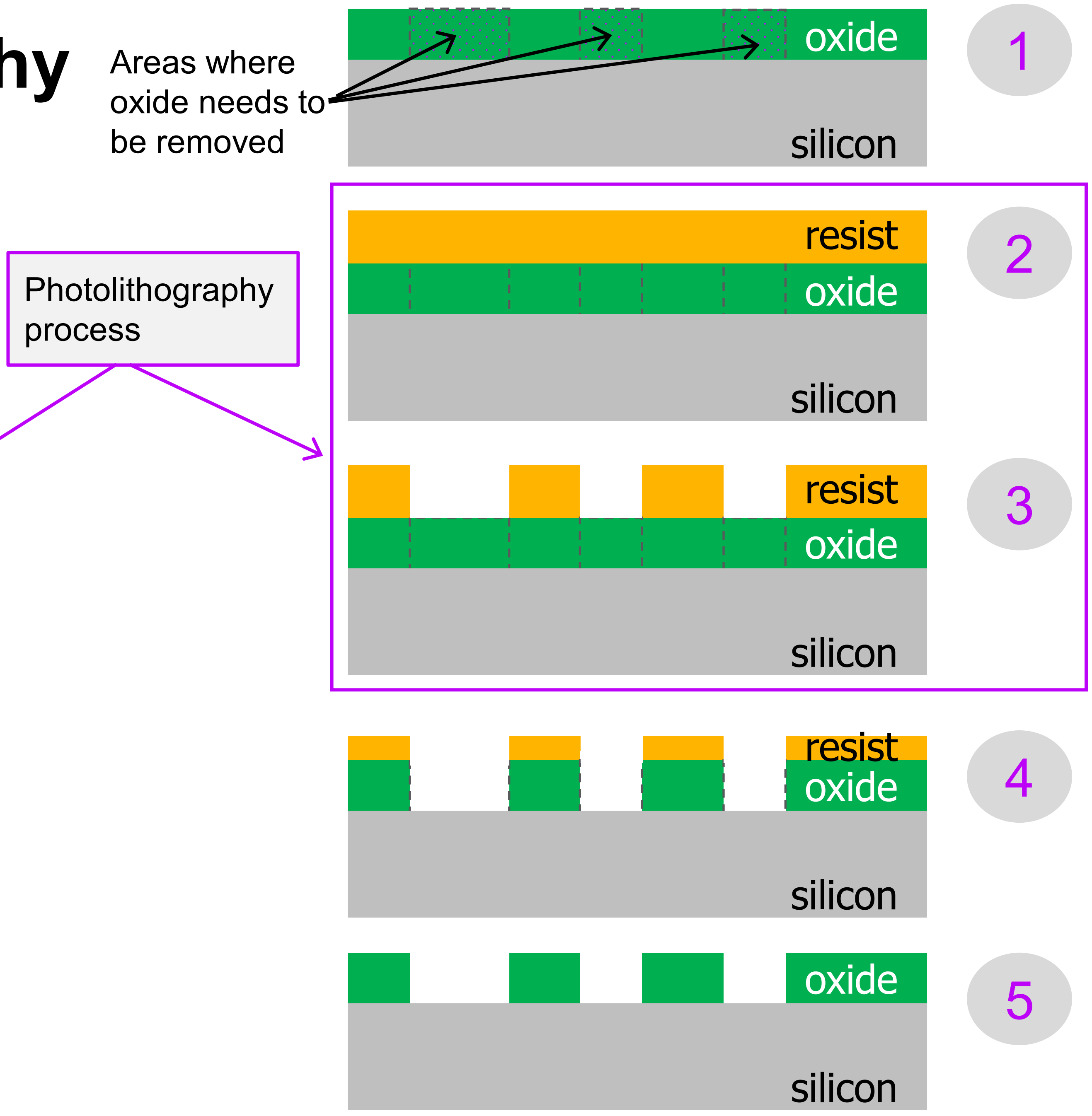
Purpose of Photolithography

micron

Purpose of Photolithography

Example to explain the purpose of the Photolithography process in semiconductor memory fabrication

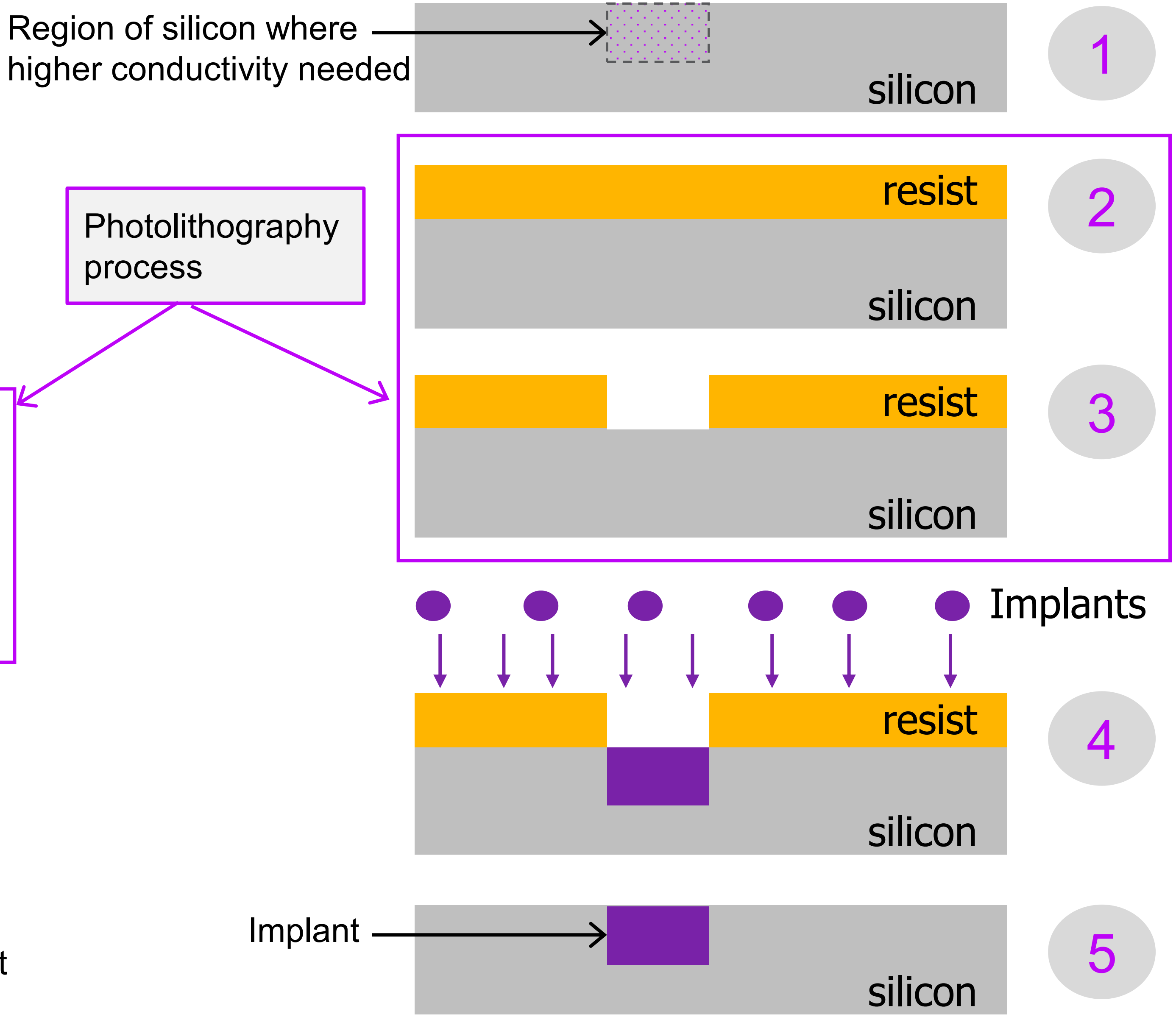
1. A silicon wafer has a layer of silicon dioxide (a.k.a. oxide) and the silicon dioxide needs to be removed in specific areas
2. Photolithography will apply a temporary layer of photoresist (a.k.a. resist)
3. And then remove the resist layer in certain areas (creating a pattern in the photoresist) using the property that the photoresist is sensitive to light
4. The regions not protected by the resist layer can be etched away
   a. Note that Photolithography is usually followed by an etch or an implant. This example shows an etch.
5. Then the remaining photoresist can be removed, leaving the needed etched pattern on the wafer



Purpose of Photolithography (cont')

Another example to explain the purpose of the Photolithography process in semiconductor memory fabrication

1. A region of the silicon wafer needs to have higher conductivity where a contact will land on the silicon. This can be achieved by incorporating an implant in that region of the silicon.
2. Photolithography will apply a temporary layer of photoresist (a.k.a. resist)
3. And then remove the resist layer from the areas where the implant is needed using the property that the photoresist is sensitive to light
4. The regions not protected by the resist layer will receive the implant
   a. Note that Photolithography is usually followed by an etch or an implant. This example shows an implant.
5. Then the resist can be removed, leaving the implant only in the regions where it was needed.



Photolithography basics

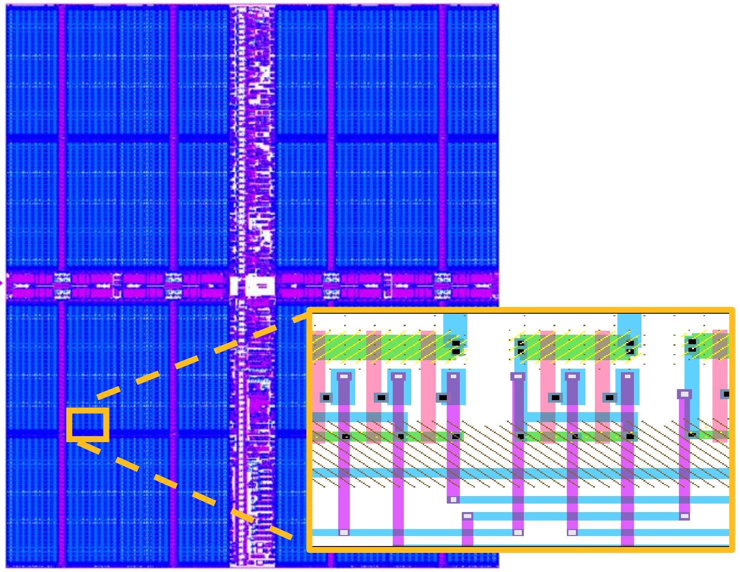
- Photolithography establishes the "floorplan" for the wafers
  - Sets down temporary layers
  - These layers guide other process areas like Etch and Implant in building the structures needed on wafer to create the different components of the circuit such as transistors, capacitors, diodes, contacts and metal connections.

- Photolithography does this through a process similar to traditional photography
  - Uses light through a lens
  - Light is absorbed by a photosensitive material
  - Pattern goes through a development process in order to capture the image

A house floorplan

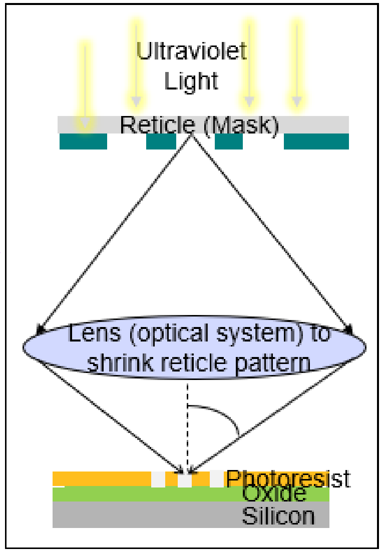
Image created for Micron by Copilot

A DRAM memory die floorplan



Traditional Photography

Image created for Micron by Copilot



Semiconductor Photolithography basic principle

Interesting Facts About Photolithography

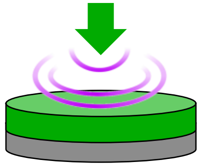
- The word photolithography literally means in Greek:
  - Using light (photo)
  - On stone (litho)
  - To print or write (graphy)
- At Micron, the words “Photolithography” and “Photo” are used interchangeably
- The words “photoresist” and “resist” are also used interchangeably
- The films that Photo applies to the wafer are temporary. Temporary films are usually referred as “sacrificial” films.
- The resist pattern created by Photo is typically used by Etch or Implant.
  - Etch uses the resist pattern to etch films in regions not protected by resist.
  - Implant uses the resist pattern to implant dopants in regions not protected by resist.
- The tools used by Photo are the most expensive tools in the fab

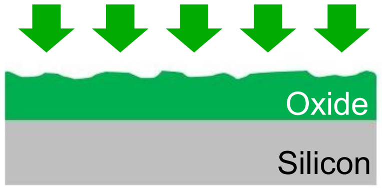
Photolithography in the Overall Process Flow

micron

Wafer Processing Areas – Five Basic Actions

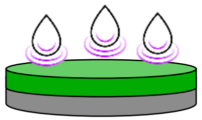
Add Material





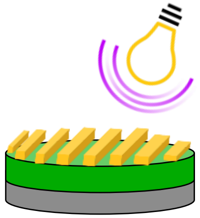
- Diffusion
- CVD (chemical vapor deposition)
- PVD (physical vapor deposition)
- Wet Process (electroplating)

Remove/Etch Material



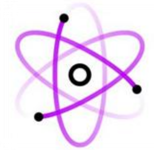
- Dry Etch
- Wet Process
- CMP (chemical mechanical planarization)

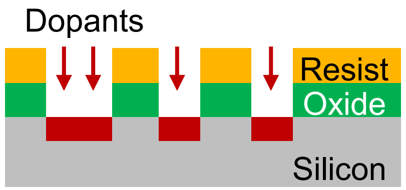
Create Patterns



- Photolithography

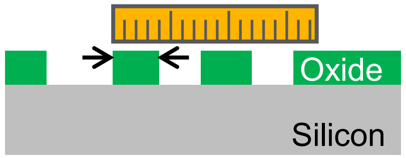
Change Electrical Properties





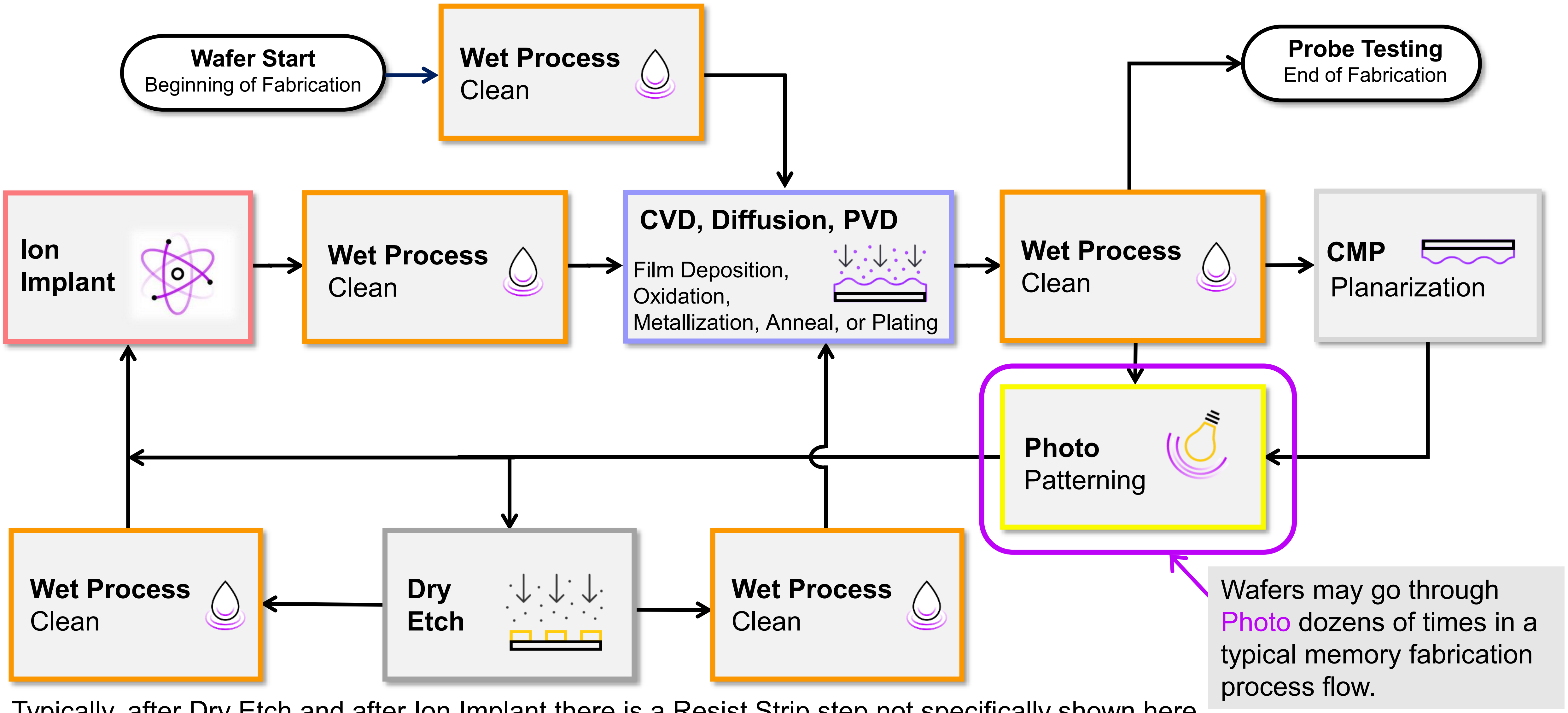
- Implant

Measure/Inspect



- Metrology
- RDA (real-time defect analysis)

Simplified Wafer Processing Flow



Typically, after Dry Etch and after Ion Implant there is a Resist Strip step not specifically shown here.
Metrology and RDA (Real time defect analysis) inspection steps can occur after every process area above.

Wafer Process Traveler and Recipes

This Traveler step takes place in the Photolithography area.

At Micron, the sequential list of every step needed to make a memory chip is called a **Traveler**. Other semiconductor companies may call it “routing sheet”, “lot traveler”, or “routing document”.

Years ago, the Traveler was printed on cleanroom paper and “traveled” along with the box of wafers. Nowadays tracking is performed digitally.

A Traveler may have more than a thousand steps!

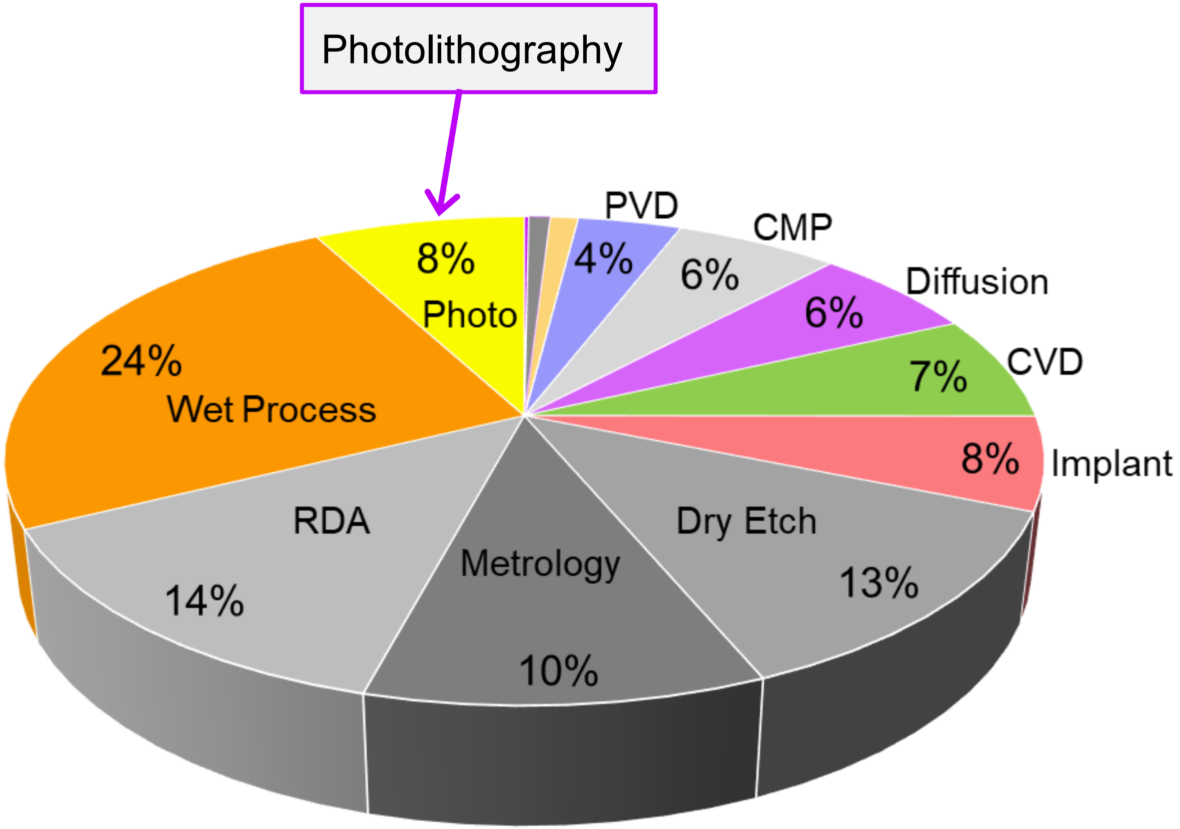
Each Traveler step belongs to one of the 10 Fab areas.

Each Traveler step has a **Recipe** associated with it. The Recipe contains detailed instructions to process the wafer (for example: temperature, pressure, chemicals or gases used, dilution of chemicals, amount of time, etc.)

Step #	Traveler Step	Fab Area
161	TG - GATE HARDMASK DEPOSITION	CVD
162	TG - GATE PHOTO PATTERN	PHOTO
163	TG - GATE PHOTO REGISTRATION	METROLOGY
164	TG - GATE CRITICAL DIMENSION	METROLOGY
165	TG - GATE DRY ETCH	DRY ETCH
166	TG - GATE DRY STRIP	WET PROCESS
167	TG - GATE WET CLEAN	WET PROCESS
168	TG - GATE CRITICAL DIMENSION	METROLOGY
169	TG - GATE STRESS	METROLOGY
170	TG - GATE PROFILE	METROLOGY
171	TG - GATE INSPECTION	RDA
172	TG - GATE SPACER WET CLEAN	WET PROCESS
173	TG - GATE SPACER OXIDE DEPOSITION	CVD
174	TG - GATE SPACER OXIDE DRY ETCH	DRY ETCH
175	TG - GATE SPACER OXIDE WET CLEAN	WET PROCESS
176	TG - GATE SPACER CRITICAL DIMENSION	METROLOGY

Breakout of Traveler Steps by Functional Area

The pie chart on the right shows a typical distribution of the percentage of traveler steps by each fab area in memory manufacturing.

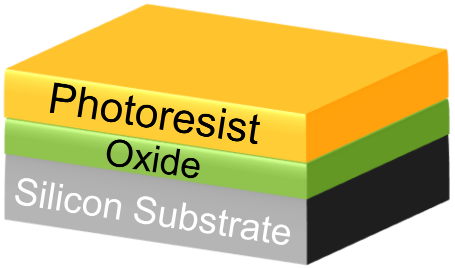


Photolithography Process Basics

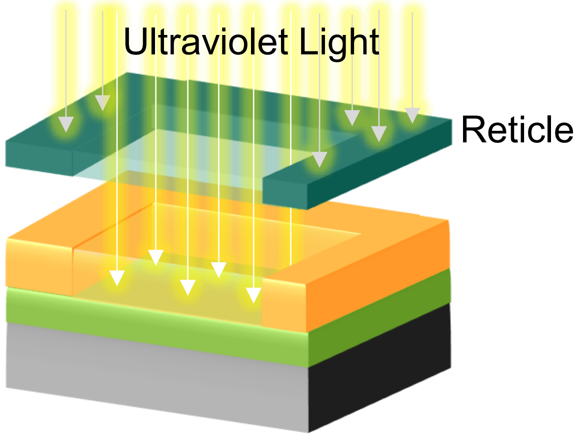
micron

Photolithography

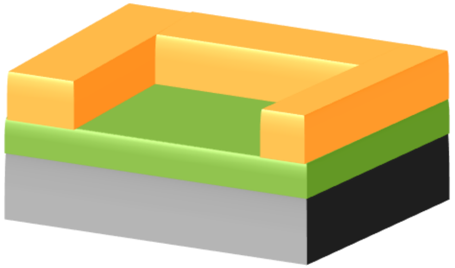
- The Photolithography area defines a temporary pattern that other areas (usually Dry Etch or Implant) use as a mask to create the structures or implants needed on the wafer.
- The temporary pattern is created on a photosensitive film called photoresist (or resist).
- Patterns created on the wafer follow the five steps shown below.
- The first three steps shown are performed in the photolithography area
- Different light wavelengths are used in the semiconductor industry for the Expose step. The smaller the wavelength the smaller the pitches/features that can be printed.
- Photoresist is “sacrificial” as only used to define temporary patterns. Once the resist pattern is used – by the Etch or Implant process – any remaining resist is removed or stripped as shown in step 5.



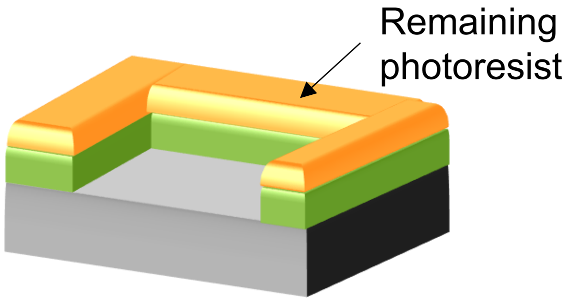
1. Apply Photoresist



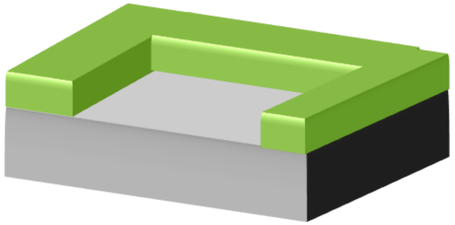
2. Expose Photoresist



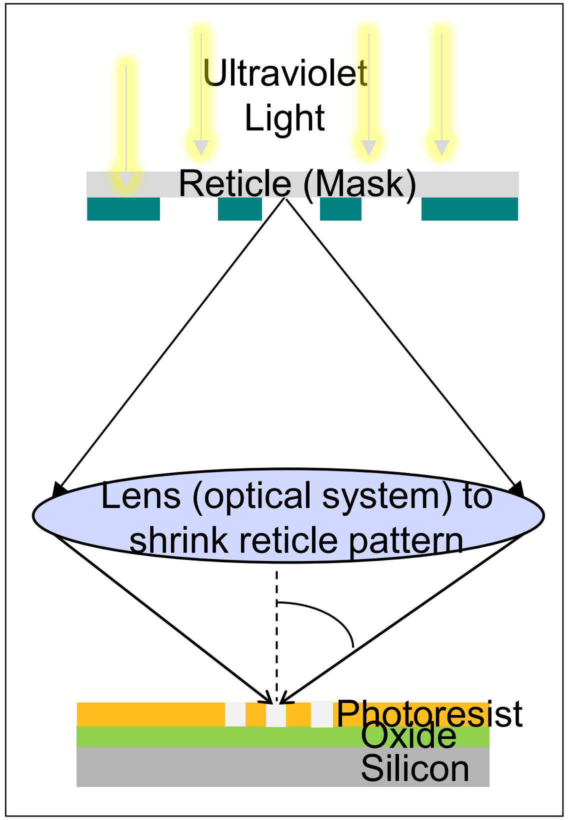
3. Develop (remove unwanted photoresist)



4. Etch (or Implant)

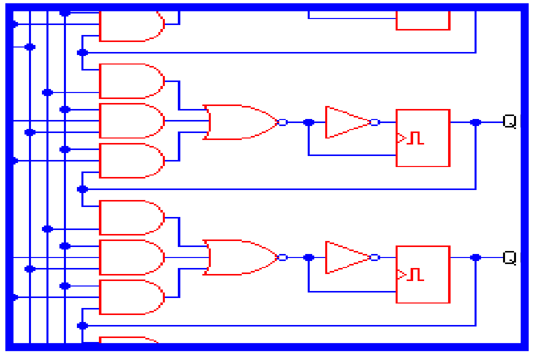


5. Strip Photoresist

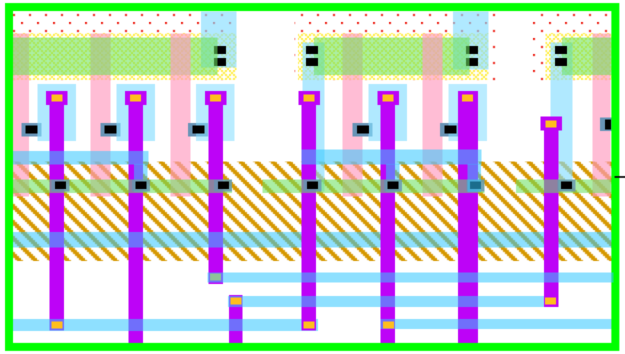


From circuit design to photolithography

1 Circuit designers design the circuits of a new memory

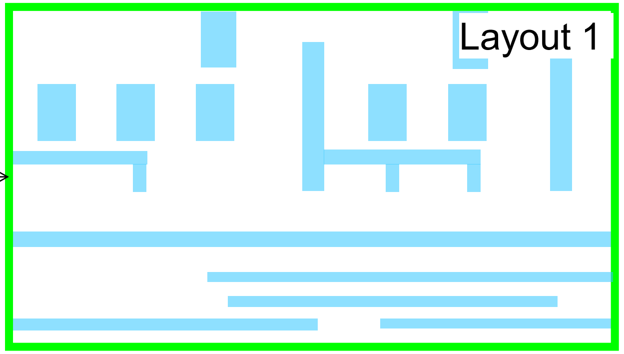


2 Layout designers convert the circuits into shapes to create the different circuit components on the wafer

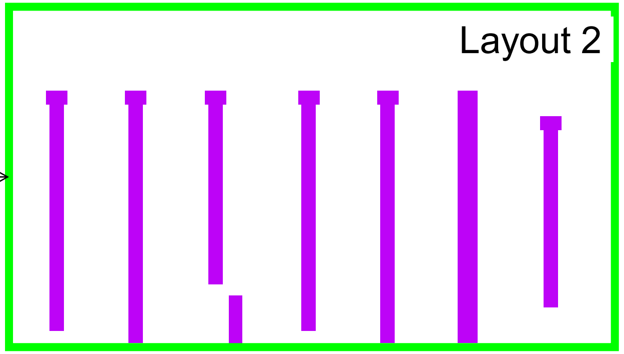


Note: this specific layout does not represent the circuit above. It is for illustration only.

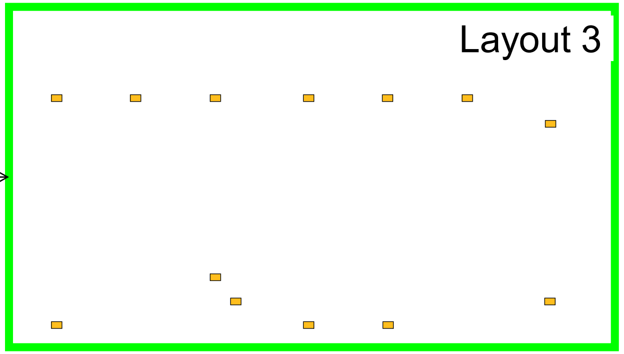
3 Each layer of the layout is written into a reticle. Dozens of reticles are needed to manufacture the memory chip. Here are three layers as illustration.



Reticle 1

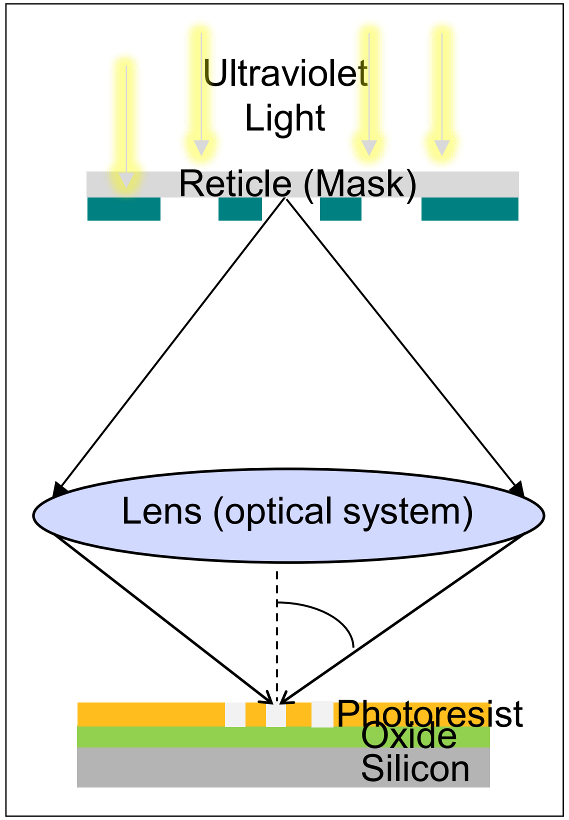


Reticle 2

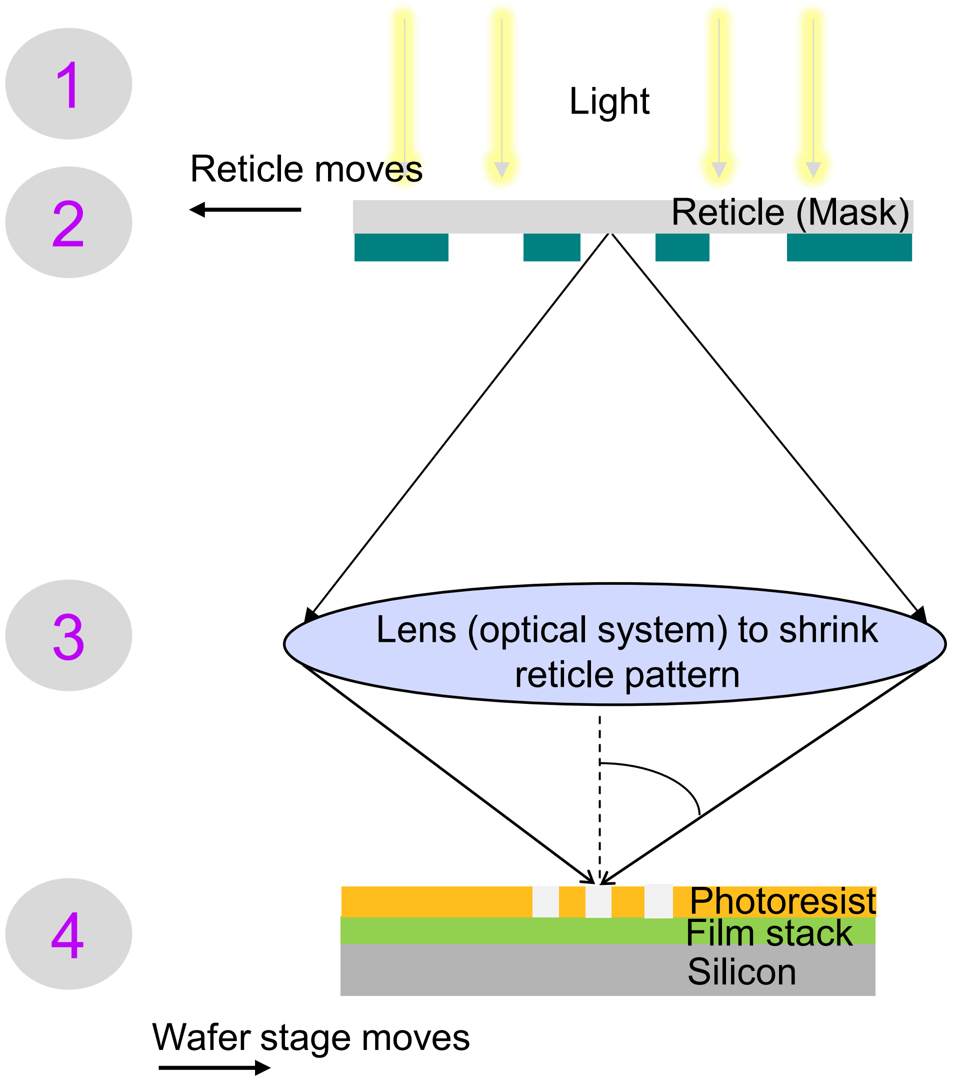


Reticle 3

4 Each reticle creates a unique photoresist pattern at a specific Photolithography step in the manufacturing process



Photolithography Overview



1. Light
   - Light from an ultraviolet (UV) source.

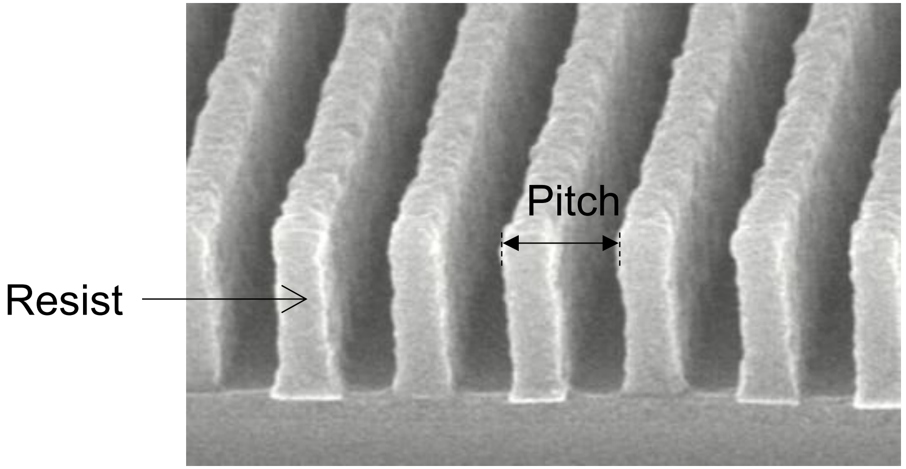
2. Reticle
   - Also known as photomask or mask
   - Contains the pattern to be transferred to photoresist
   - In semiconductor memory manufacturing the reticle pattern is typically 4X larger than the transferred photoresist pattern.

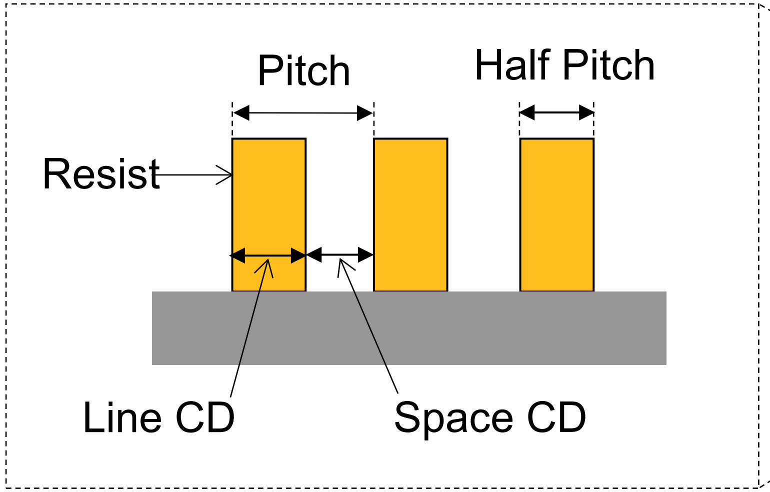
3. Optical system
   - Optical lens system reduces the image
   - Reduced image is transferred to the resist

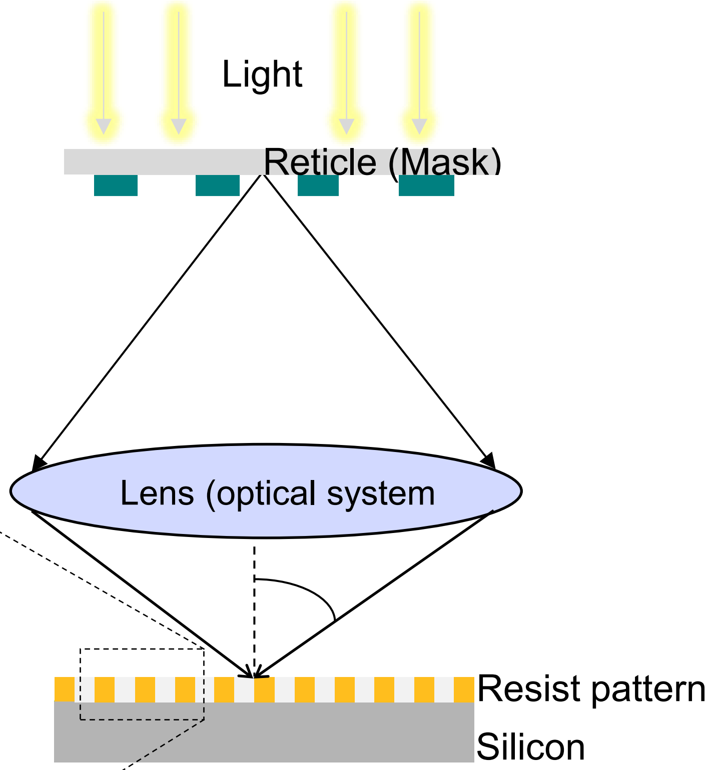
4. Photoresist
   - Also known as resist
   - Resist reacts with light to form the pattern
   - Resist is sensitive to a specific wavelength

Dimensions definitions

- CD = Critical Dimension
- CD examples:
  - Line Width
  - Space Width
  - Diameter (for contacts)
- Pitch = Line CD + Space CD
- If Line = Space
  - Then Half Pitch (hp) = CD
- In the semiconductor memory industry, Feature Size usually refers to “Half Pitch”



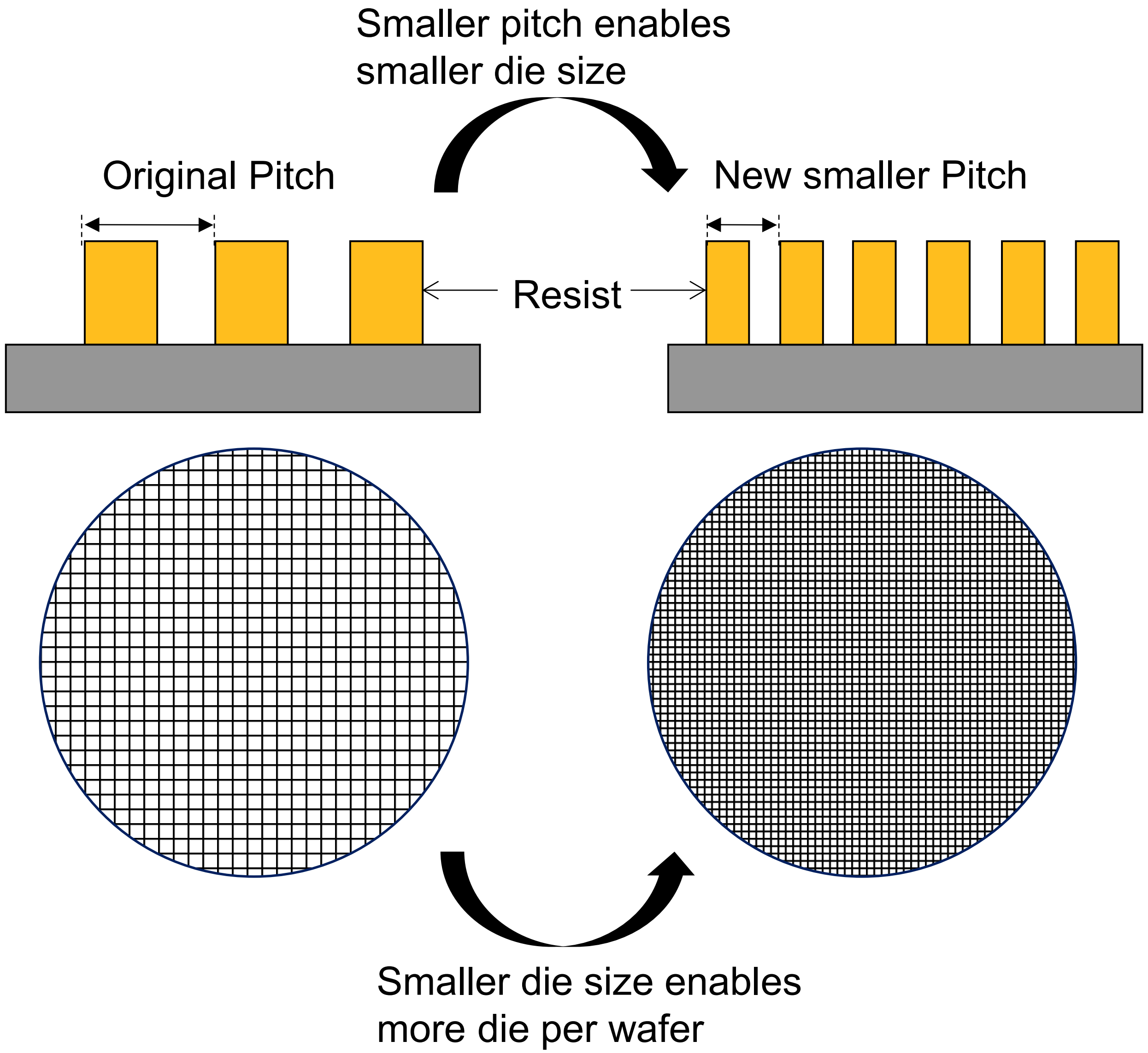




The Quest for Smaller Pitches

- Pitch Size Matters!
- Photolithography is usually tasked with printing the smallest pitch possible
  - But of course, process must be manufacturable (repeatable) with acceptable image quality
- Generally speaking, a smaller pitch leads to:
  - Smaller die size → more die/wafer → more $$$
- Also, given a specific die size, a smaller pitch allows to have more memory density on each die
  - 1 gigabit → 2 gigabits → 4 gigabits → . . .

Example: given a certain memory density (e.g. 1 Gb)…



Resolution

- Resolution = how small can we print?
- The Rayleigh's equation helps answer this question

Rayleigh's Equation

factor that depends on process characteristics

$$R = \frac{k \times \lambda}{NA}$$

Light wavelength (lambda)

Numerical Aperture of the imaging system

Smallest printable size (resolution)

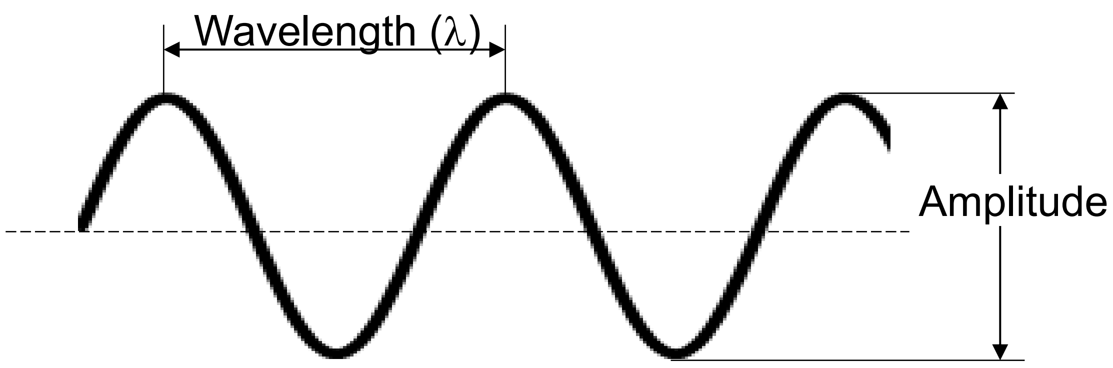
- Rayleigh's equation indicates:

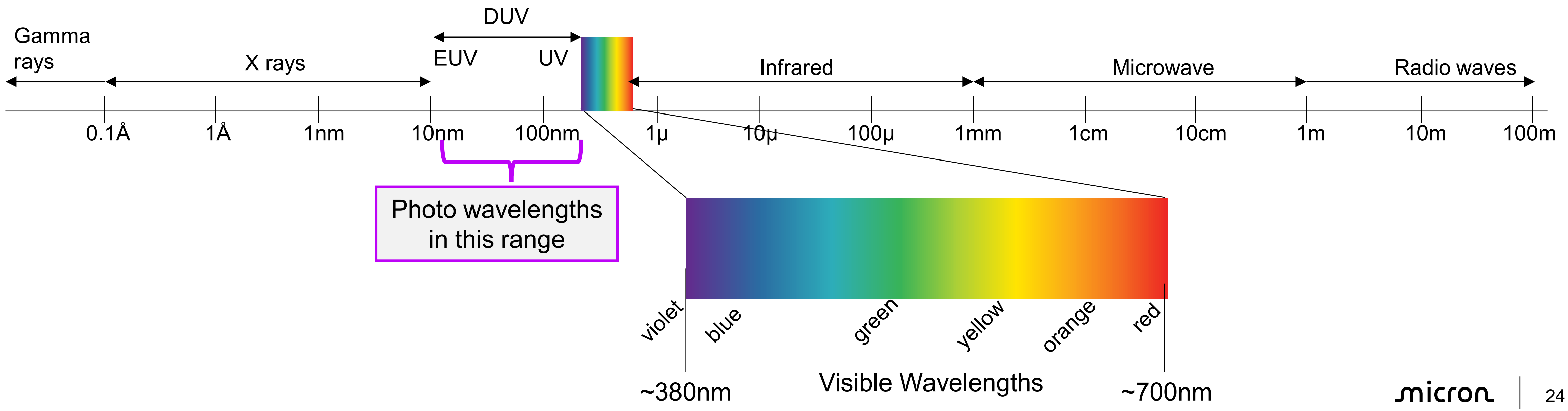
1) As Wavelength (λ) $\downarrow$ Resolution $\downarrow$
2) As Numerical Aperture $\uparrow$ Resolution $\downarrow$

- In the next slides each factor in the Rayleigh's equation is explored in more detail

Electromagnetic Radiation - Wavelength

- Light is an Electromagnetic Wave
- Wavelength (λ) is the distance between the peaks of a wave
- Visible light has wavelengths from about 380 nm (violet) to 700 nm (red). With visible light, wavelength is perceived as color.
- Photolithography uses Ultraviolet (UV) light. UV wavelengths are shorter than visible light wavelengths – UV light is invisible. Newer Photolithography equipment uses EUV wavelength (Extreme Ultra Violete).



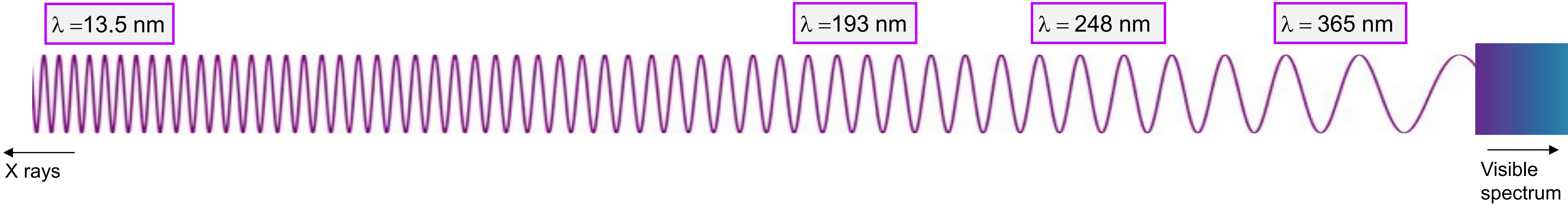


Wavelengths used in the memory semiconductor industry

- Wavelengths used in Photolithography to expose photoresist in Semiconductor Memory manufacturing: 365 nm, 248 nm, 193 nm, 13.5 nm (EUV)

$$R = \frac{k \times \lambda}{NA}$$

Which of the wavelengths used in Photolithography can resolve the smallest pitch?
Hint: look at Rayleigh's equation



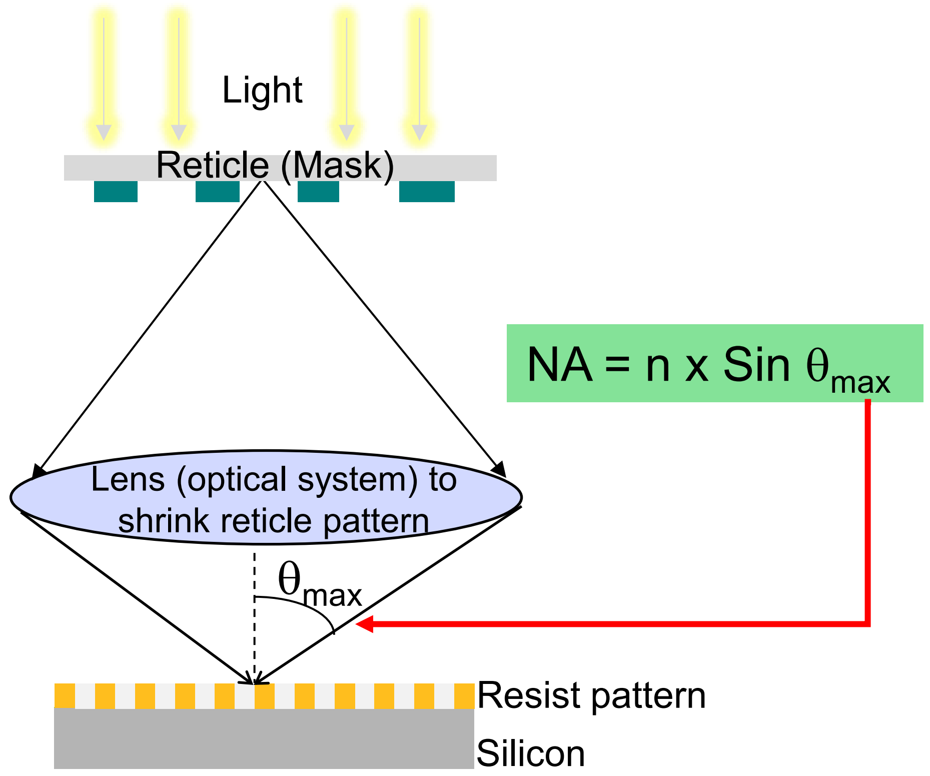
Note: Wavelengths representation not to scale

Numerical Aperture

$$R = \frac{k \times \lambda}{NA}$$

- Numerical Aperture (NA) is a value that characterizes the size of the lens and its ability to capture light from a wide range of angles.
- NA can be described as the *"light gathering ability" of an optical system.*
- Higher NA systems can resolve or print smaller pitches by condensing light from a wider angle (capturing a larger diffraction angle of light)
- NA can be calculated as NA = n x Sin θ_{max}

  − where n is refractive index of medium between resist and lens
- NA is based upon:
  1. The shape and size of the lens
  2. The material/medium between the lens and the wafer



Intro to Immersion Lithography

- The Index of refraction (n_f) is the ratio between the speed of light in a vacuum and the speed of light in another medium or material.
- It is the measure of how much light slows when it travels through a medium or material (with respect to perfect vacuum)

Medium	n_f	Notes
Perfect vacuum (e.g. space)	1	This is the definition of n_f = 1
Air	~1	Slightly higher than 1
Water	1.33	Light slows down with respect to Air
Oils	~1.7	Light slows even more than in Water
Glass-type compounds	1.4-1.6	This is listed in the table to show the n_f of the lens material

Intro to Immersion Lithography

- Historically, the space between the lens and the wafer has been filled with air (Dry Lithography)
- Immersion Lithography was introduced to achieve the effect of increasing the numerical aperture (NA) of the system without requiring a larger lens
  - Effective NA can be calculated as n_f x Sin θ_{max}
- Immersion Lithography fills the space between the lens and the wafer with a medium with a higher index of diffraction than air.
- DI water typically used as medium (de-ionized water), n_f = 1.33

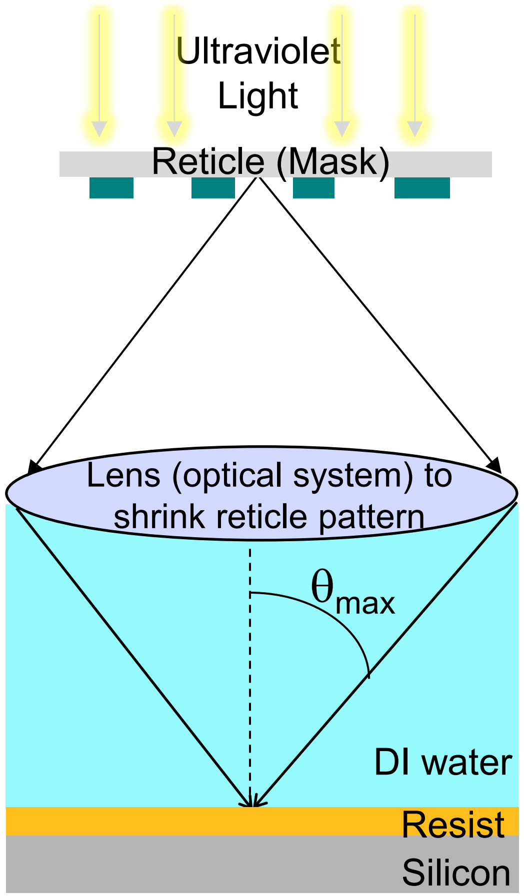
n_f ↑ NA ↑ Resolution ↓

$$R = \frac{k \times \lambda}{NA}$$

Effective NA = n_f x Sin θ_{max}

Medium	n_f @193 nm
Air	~1
Water	1.33
Glass	1.4-1.6

Immersion Lithography



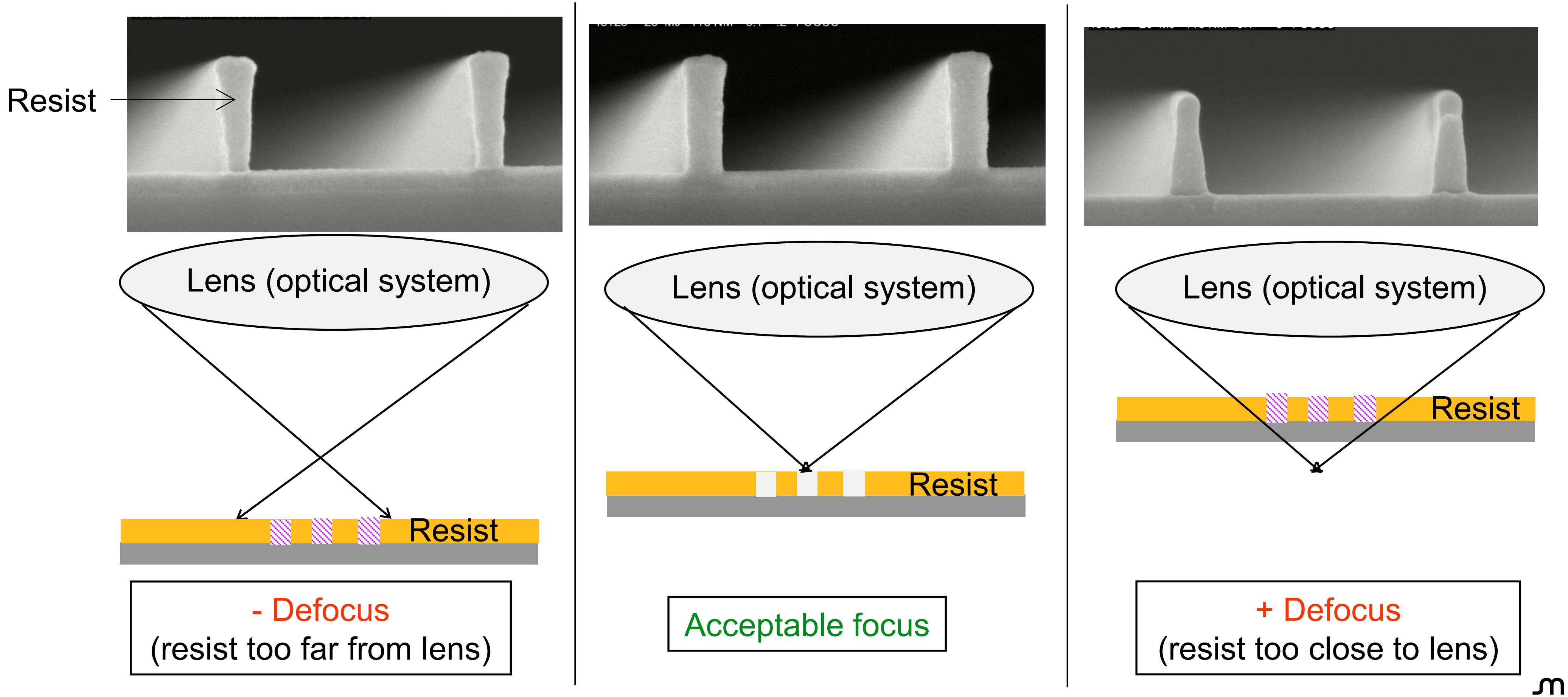
Resolutions by technology

$$R = \frac{k \times \lambda}{NA}$$

	Resolution by Photolithography technology				
Technology	I-Line	DUV	193 nm DUV dry	193 nm DUV Immersion	EUV
Wavelength	365 nm	248 nm	193 nm	193 nm	13.5 nm
Light source	Mercury arc lamp	KrF excimer laser	ArF laser	ArF laser	Sn laser pulsed plasma
Numerical Aperture	NA = 0.45 to 0.65	NA = 0.8	NA = 0.93 / 0.92	NA = 1.35	NA = 0.33
Theoretical min k	0.25	0.25	0.25	0.25	0.25
Minimum Half Pitch	280-350 nm	80-110 nm	57 nm / 65 nm	38 nm	13 nm

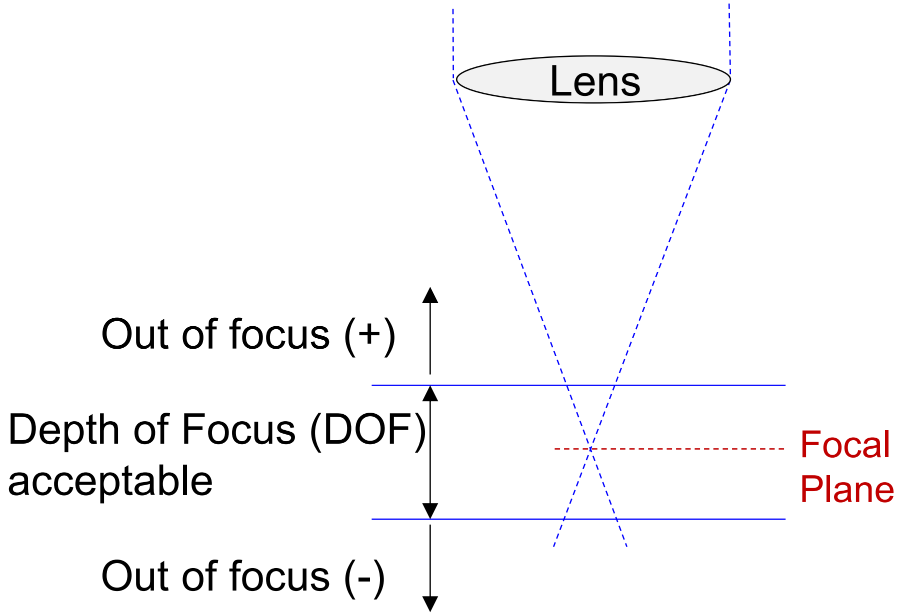
Photolithography Parameters: Focus

- Focal plane refers to the precise vertical position of the wafer where the projected image from the scanner lens is sharply formed. The wafer stage can be adjusted vertically to place the resist in the focal plane.
- The typical unit used to describe focus is nm.
- Focus must be adjusted within a narrow range to achieve the desired image quality and feature sizes (CD's).

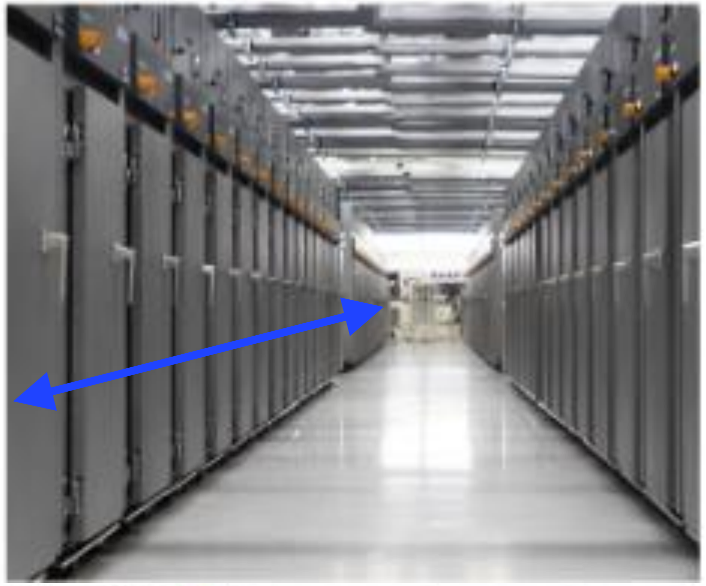


Depth of Focus (DOF)

- Depth of Focus is the range of focus positions that yields an acceptable image, i.e., the range in which the image is in focus and clearly resolved.
- Large DOF is desirable because the wafer is not perfectly flat and the tool stage leveling system is not perfect
- Higher NA lenses have lower DOF
  - Depth of focus proportional to $1/NA^2$



- Large DOF
- The items at the front of the image and the ones in the back have similar "sharpness" (in focus)



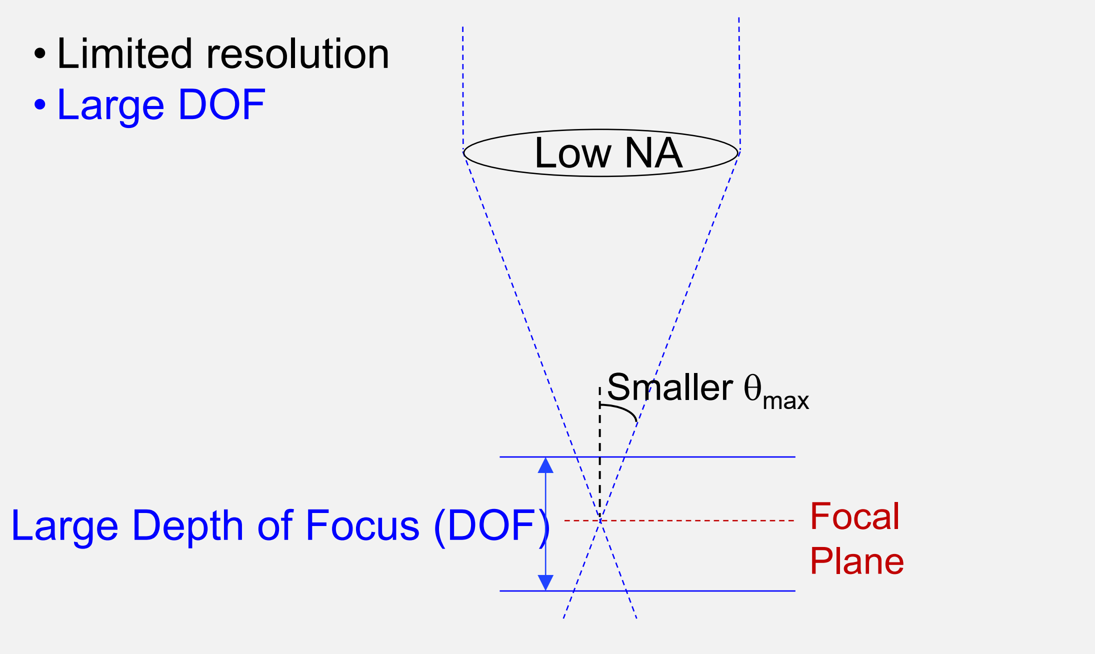
- Small DOF
- The items at the front of the image are sharp and in focus, while background is blurred (out of focus)

Numerical Aperture and Depth of Focus

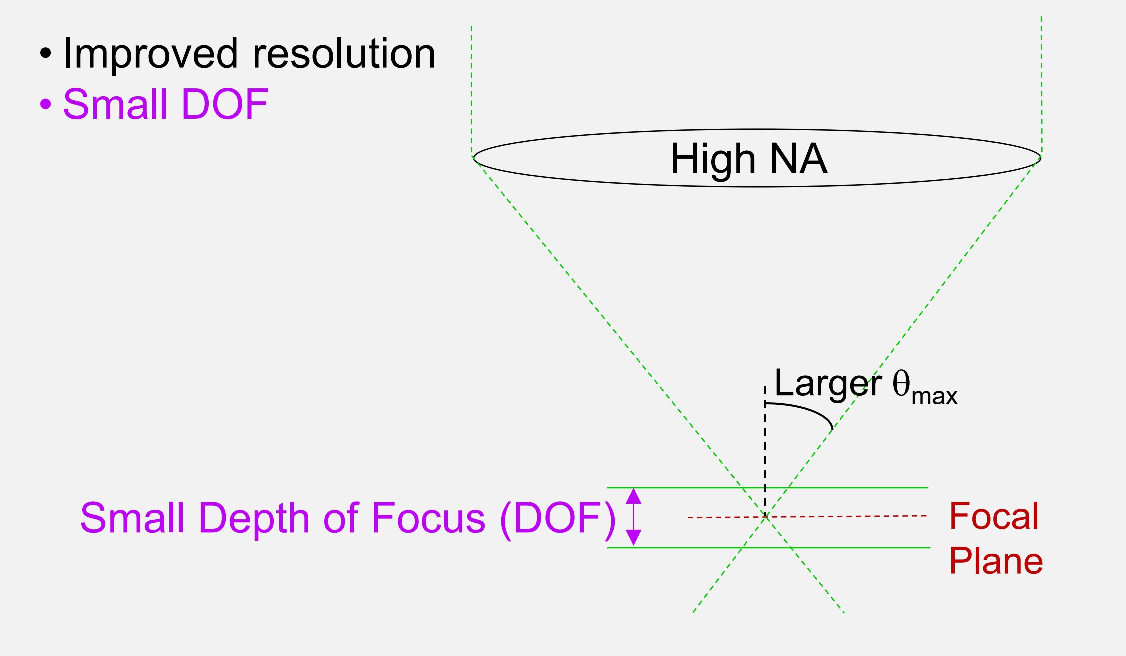
- A higher NA lens system captures a larger diffraction angle of light
  - ☺ Higher NA is capable of resolving smaller pitches (higher resolution), BUT . . .
  - ☹ Higher NA reduces Depth of Focus (DOF) proportional to $1/NA^2$
- DOF is the range in which the image is in focus and clearly resolved

$$R = \frac{k \times \lambda}{NA}$$

Low NA

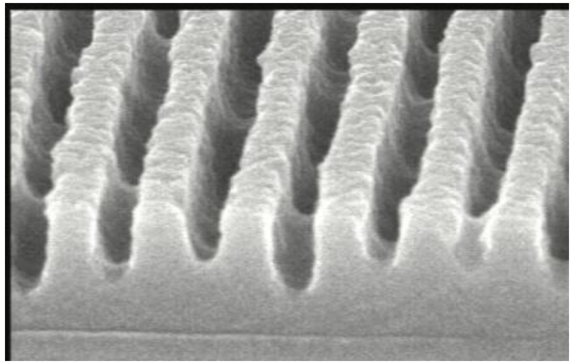


High NA

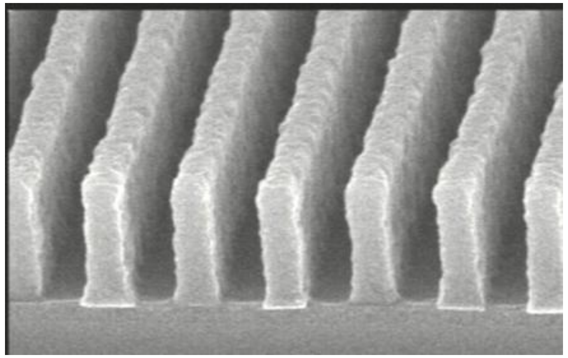


Photolithography Parameters: Dose

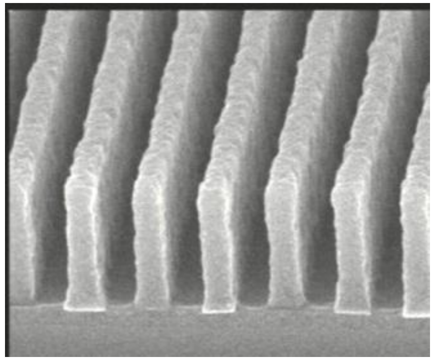
- **Dose**: is the amount of light energy that reaches the photoresist.
- Dose has units of energy per unit area
  - The typical unit used to describe dose is mJ/cm2 (milli Joules per square centimeters).
- Dose must be adjusted within a narrow range to achieve the desired image quality and feature sizes (CD's).



underexposed
(too low dose)



Acceptable dose



overexposed
(too high dose)

k_1 – Rayleigh's Process Coefficient

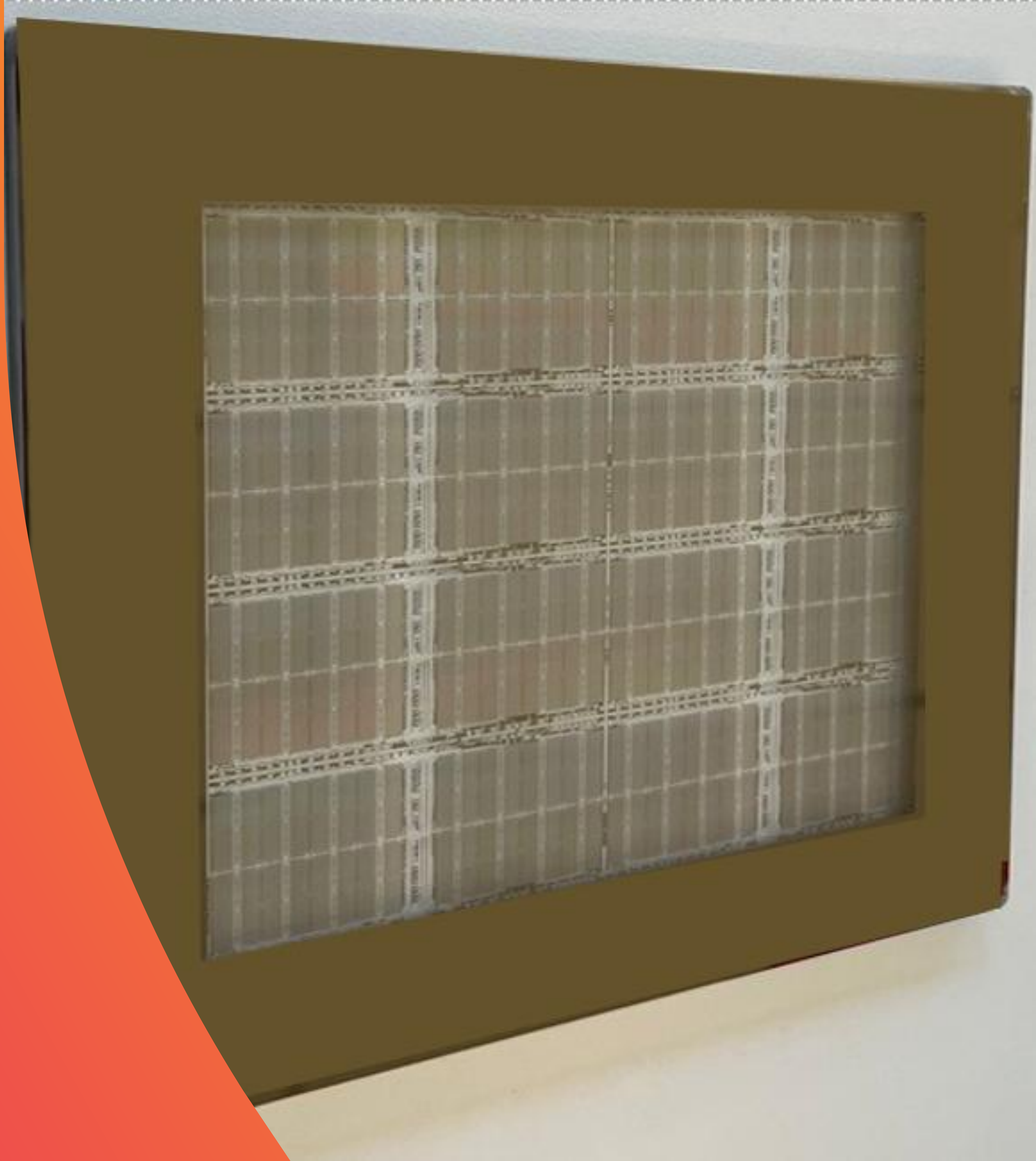
- k_1 is a process coefficient in the Rayleigh equation
- k_1 is a complex factor based on several lithography variables such as:
  - Quality/type of photoresist
  - Resolution enhancement techniques utilized
    - PSM - Phase Shift Masks
    - OAI - Off-Axis Illuminations
    - OPC - Optical Proximity Correction
    - Light polarization

  Will be covered in future modules
- Theoretical minimum limit for k_1 is 0.25
- Current lowest production k_1 is less than 0.3

$$R = \frac{k_1 \times \lambda}{NA}$$

Intro to Reticles

micron

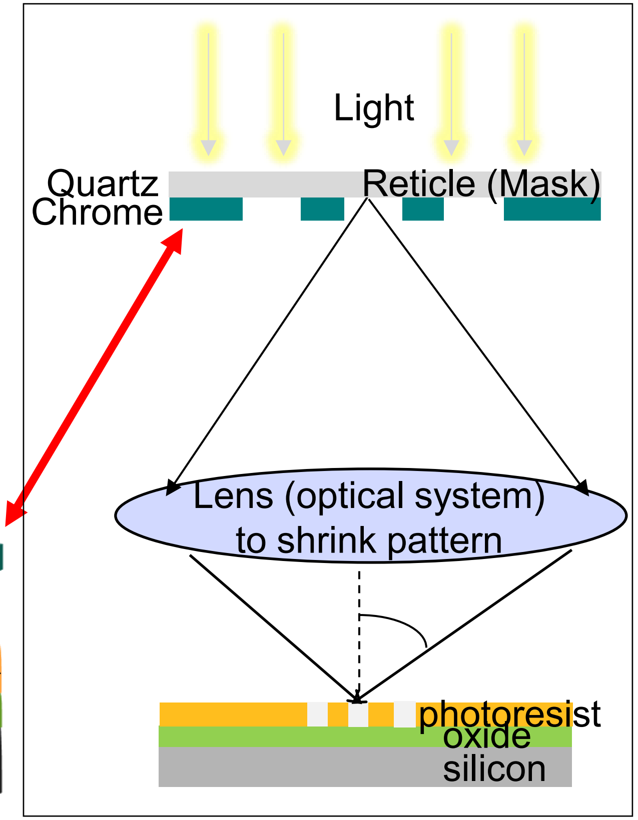


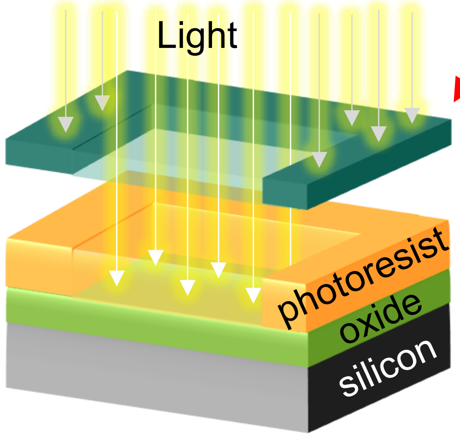
Reticles

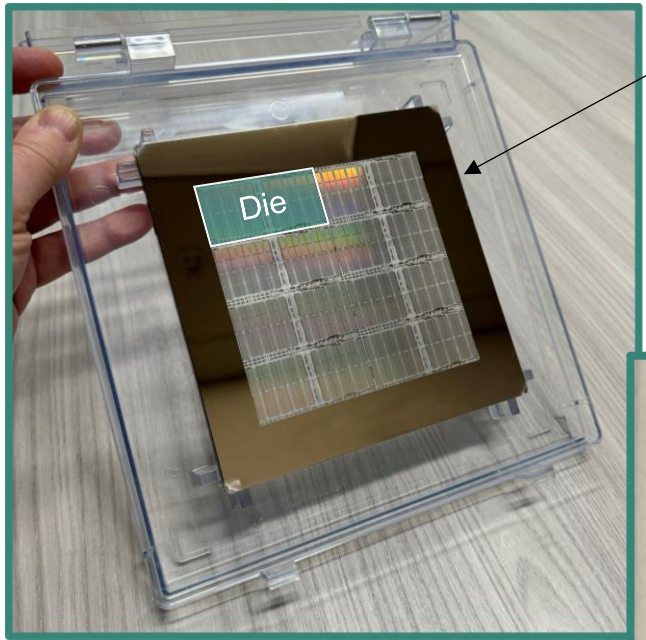
- Reticles, also called Masks or Photomasks, are used in Photolithography to expose a temporary pattern on the photoresist
- Micron uses different types of reticles. The reticle type described here is the Binary reticle (quartz + chrome). Other types of reticles will be covered in future modules.
- A binary reticle is a very flat piece of quartz or glass substrate with a layer of chrome on one side. Patterns are etched into the chrome during reticle fabrication.
- Micron has a state-of-the-art Mask Shop where reticles for the Micron fabs are manufactured
- Reticles typically have die patterned in an x by y array
- The reticle shown here has a 2 die x 4 die layout

Die	Die
Die	Die
Die	Die
Die	Die

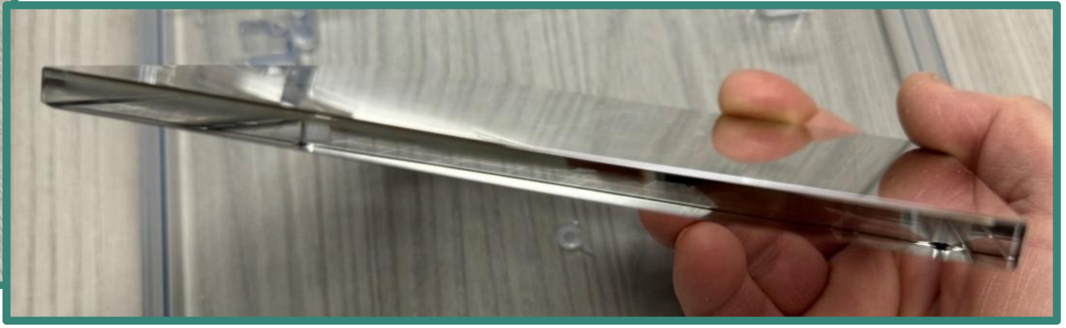
- The spaces in between die are used for inline process monitoring structures as well as electrical devices that can be tested inline or at the end of wafer processing







Picture of a reticle in a protective box
(frame markings have been blurred)

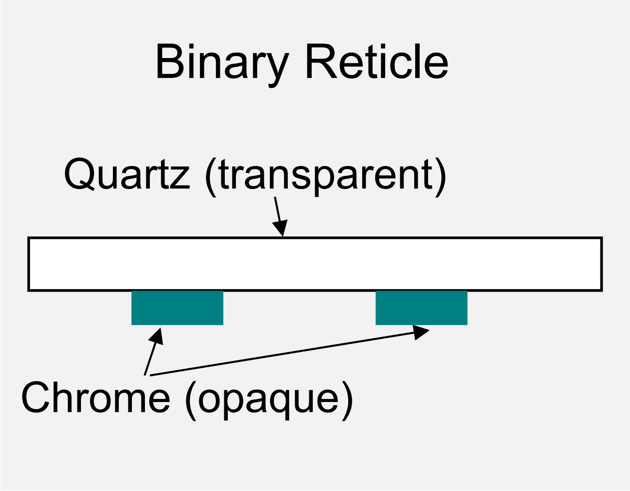


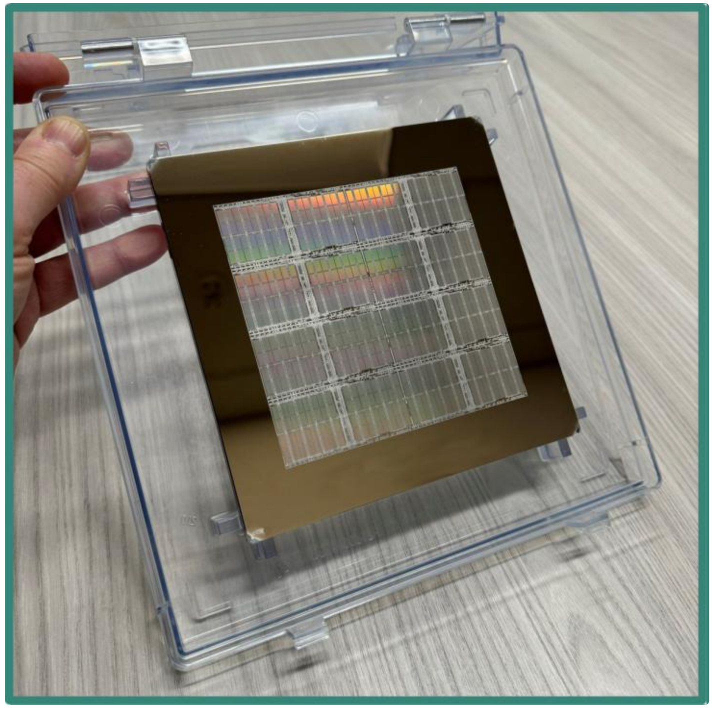
Picture of a reticle – different perspective

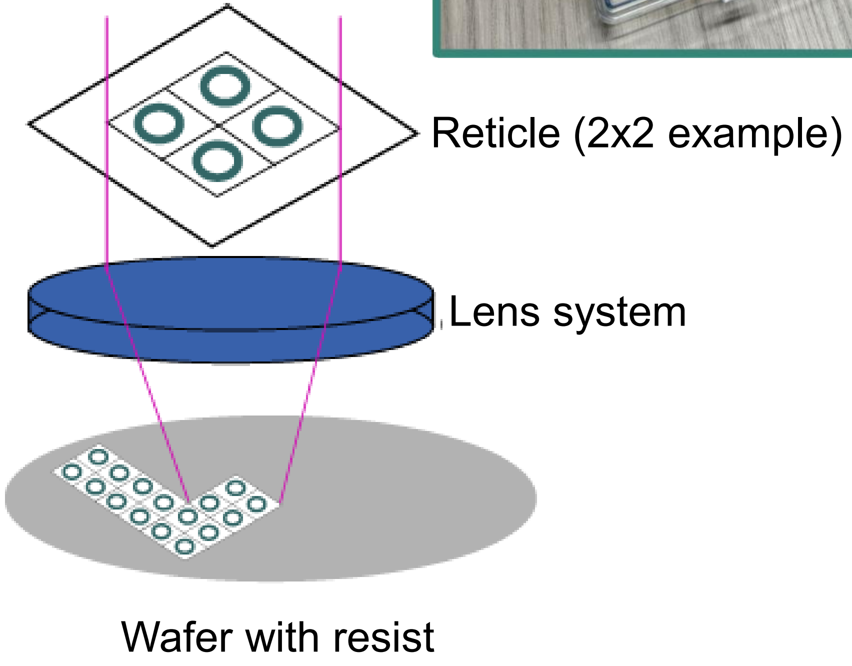
Reticles

- The reticles are delivered to the wafer fab where they are used in the Photolithography tools
- In the Photolithography tool light passes through the quartz, but not through the chrome
- Photolithography involves projecting the reticle image onto the wafer
- Features in the reticle are typically 4X larger than what is printed in the resist
- Projecting the reticle field several times side-by-side onto the wafer is known as stepping
  - A reticle has a small number of die. To fill the whole wafer with die pattern the reticle field needs to be exposed multiple times. Each exposure is called a shot.

Photolithography Engineers collaborate with different teams to define reticle specs and coordinate with the mask shop to ensure specs align with wafer printability and process integration goals.



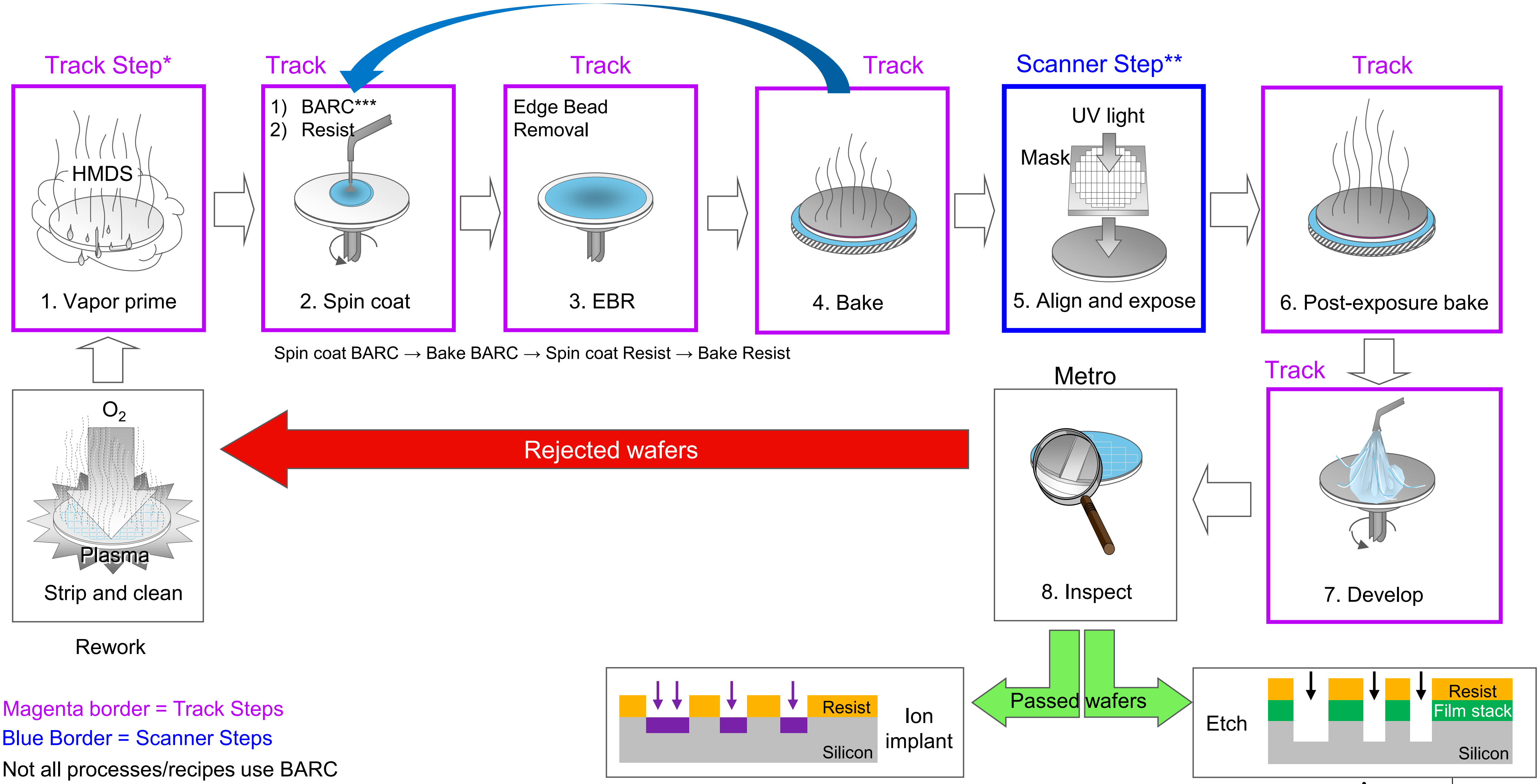




Types of Processes in Photolithography

micron

Photolithography Steps – Simplified flow

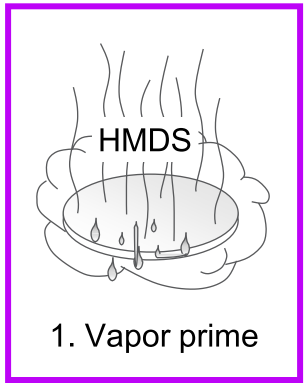


* Magenta border = Track Steps

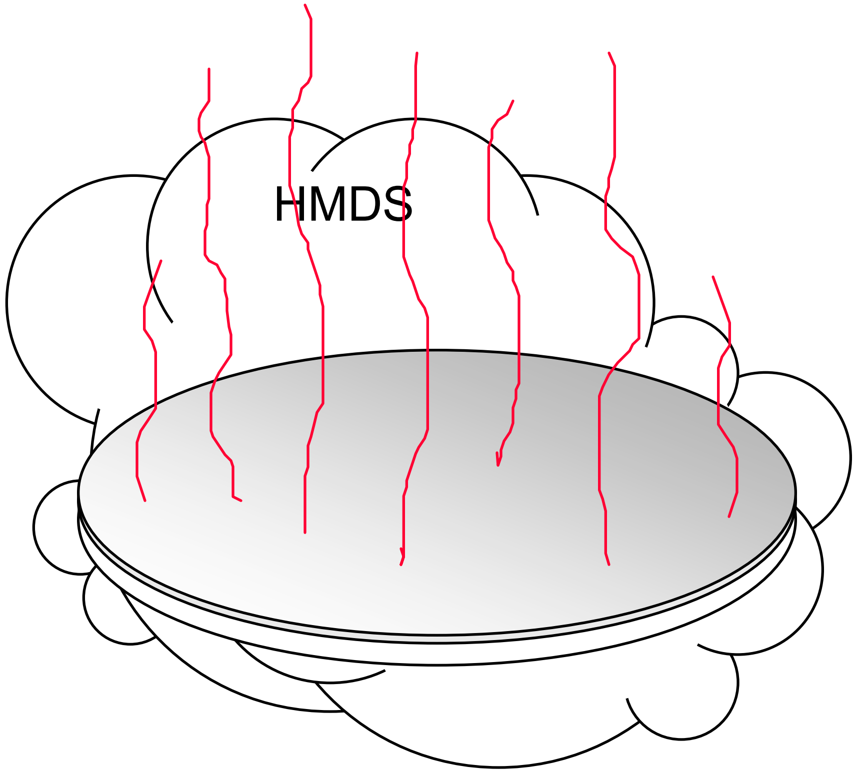
** Blue Border = Scanner Steps

*** Not all processes/recipes use BARC

Surface Preparation (HMDS Vapor Prime)

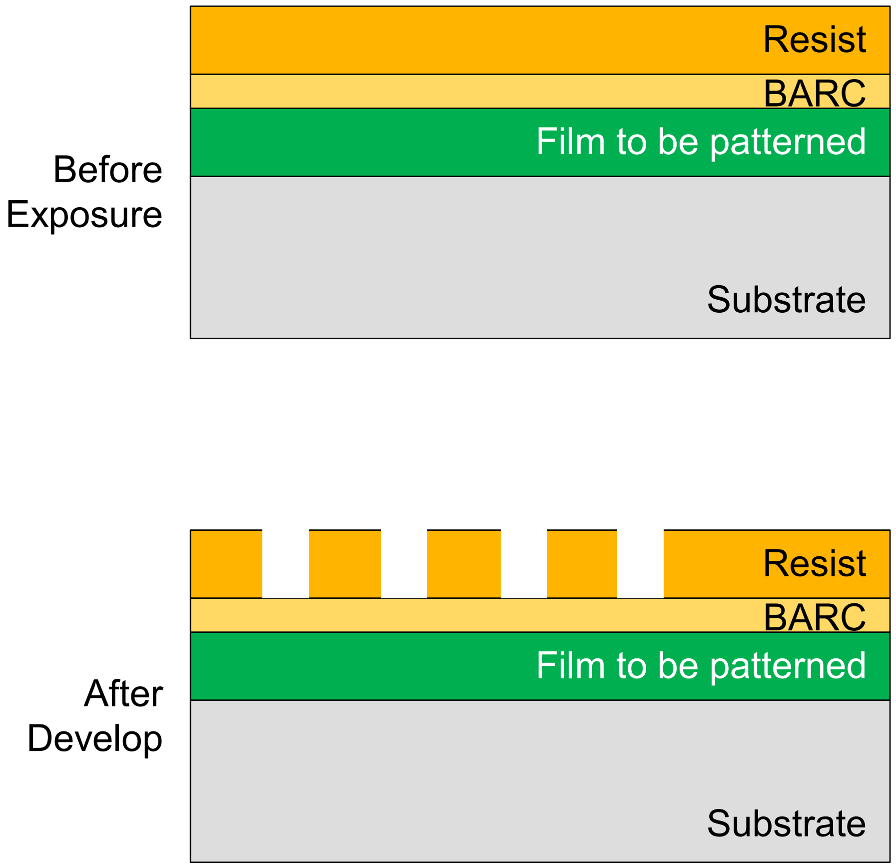


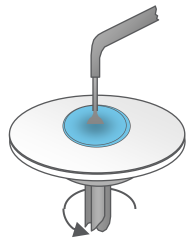
- Purpose: eliminate water molecules from the wafer surface to improve contact angle between the resist and the wafer which improves resist adhesion
- Dehydration bake in enclosed chamber with exhaust
- Clean and dry wafer surface (hydrophobic)
- Flow Hexamethyldisilazane (HMDS) across wafer surface which reacts to the wafer to improve contact angle
- Time and temperature depends on process



Spin Coat Film - Bottom Anti-reflective Coating

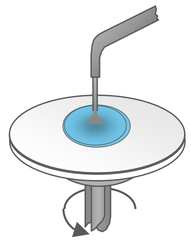
- BARC is a film that is spun onto the wafer immediately prior to application of Photoresist for some processes
- Not every process requires BARC. Example: several DUV layers require BARC under the resist, but I-Line (365 nm) does not typically require BARC
- Purposes of BARC:
  1. Planarizes the surface prior to resist application
  2. Reduces reflectance of the DUV light from the substrate
  3. Improves the profile of the patterned resist (reduced footing)
- Next slides cover these topics in more detail



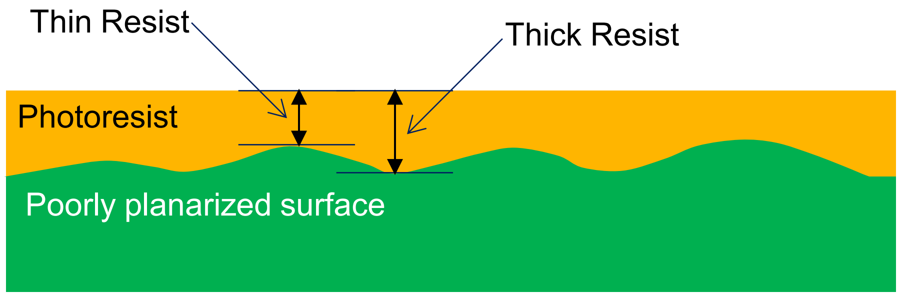


2. Spin coat BARC

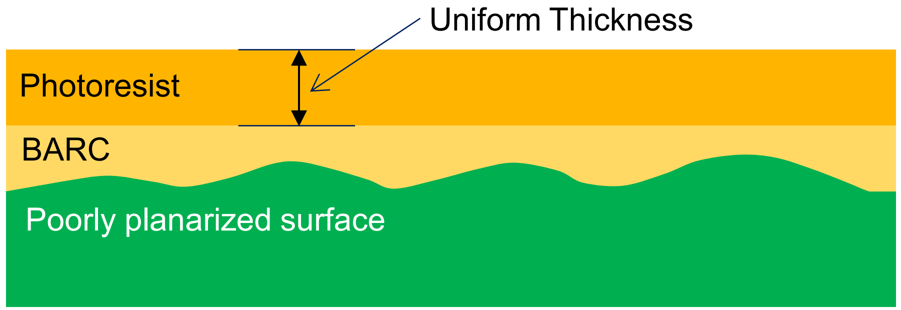
BARC - Planarity



- Planarity:
  - Many of the wafer fabrication processes leave an uneven wafer surface with some topography.
  - This uneven wafer surface causes the DUV light exposure to be absorbed by the thin films at different rates, depending on the resist thickness.
  - The result is excessive line-width variations.
  - BARC is used to maintain an even resist thickness.



Without BARC

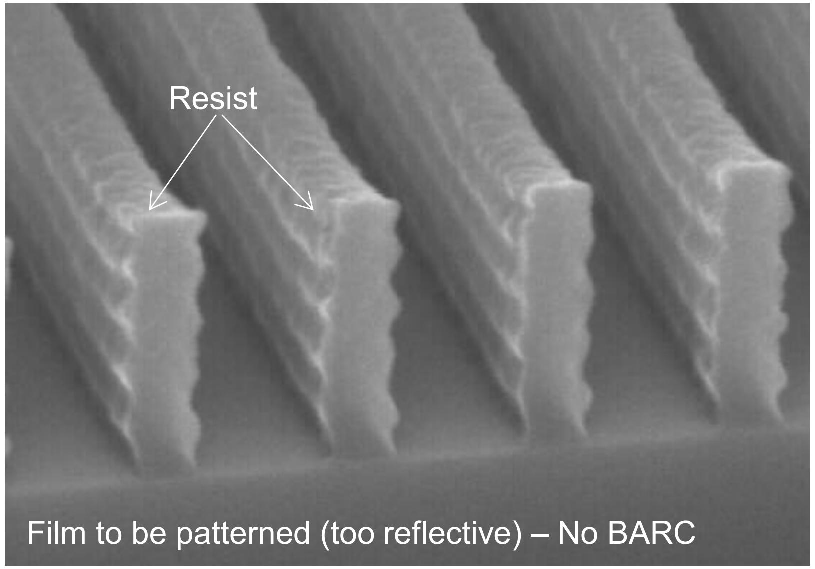


With BARC

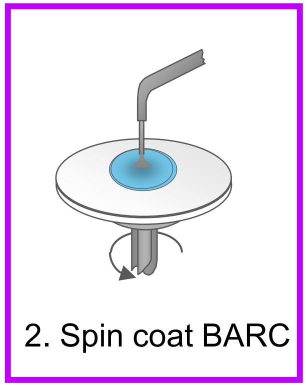
BARC – Reflectivity Control

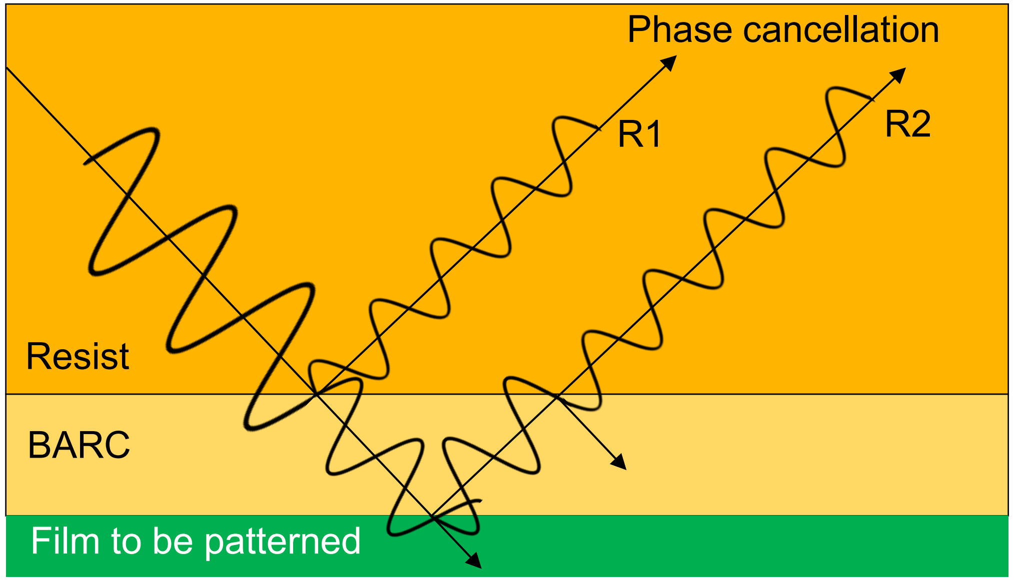
- Light reflected from a flat surface underneath the resist creates an interference pattern when combined with the incident light.
- The result is a wavy resist sidewall (see picture) that can lead to poorly defined features in dry etch. Standing waves also limit the amount of light energy that is absorbed by the resist.
- BARC is one of many anti-reflective coatings (ARCs) used in semiconductor manufacturing. BARC films are typically carbon-based polymers.
- Principle
  - Light reflects at film interfaces and causes constructive/destructive interference.
  - The amount of interference between the initially reflected ray and subsequently reflected and refracted rays depends on:
    - Index of refraction (n) of resist and underlying layer
    - Thickness of underlying layer.

Photolithography Engineers need to identify the best BARC film (n and k values) and BARC thickness for their processes.



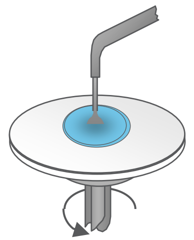
SEM showing “standing waves” in the resist





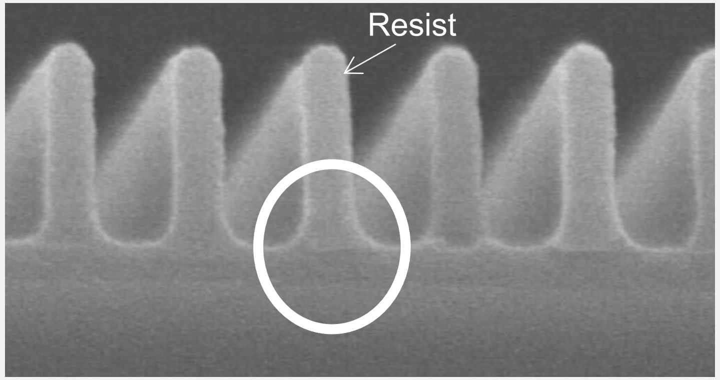
BARC – Footing reduction

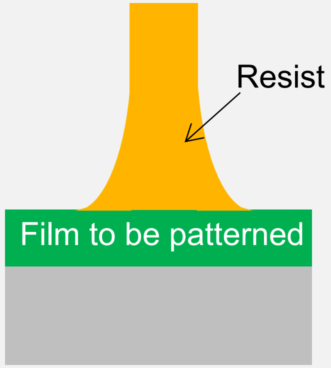
- Photoresist patterned directly on top of some films yields a “footed” profile (see pictures on the left)
- BARC helps prevent footing and achieve a more vertical profile

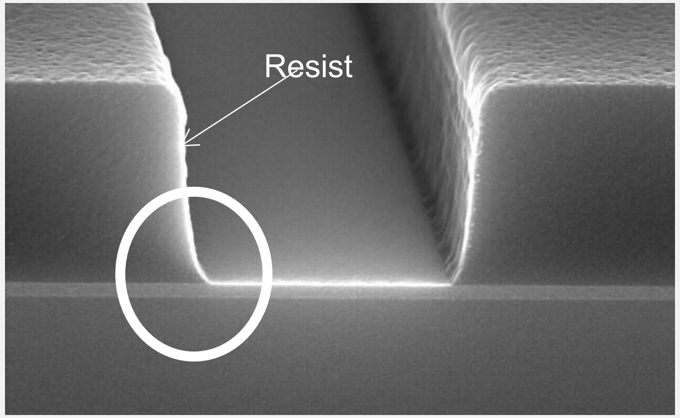


2. Spin coat BARC

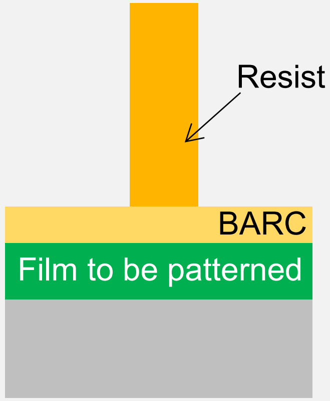
Footed Profiles - no BARC

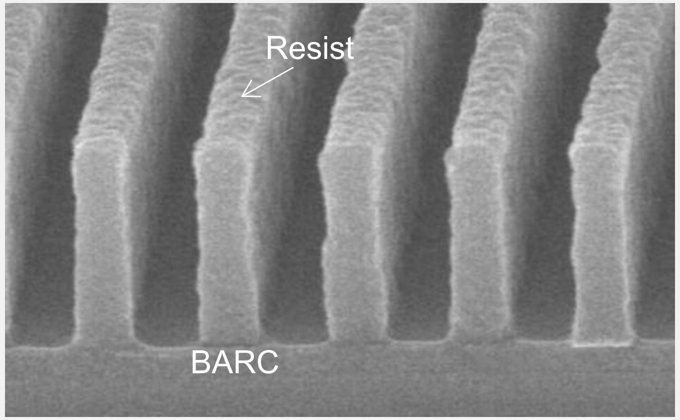




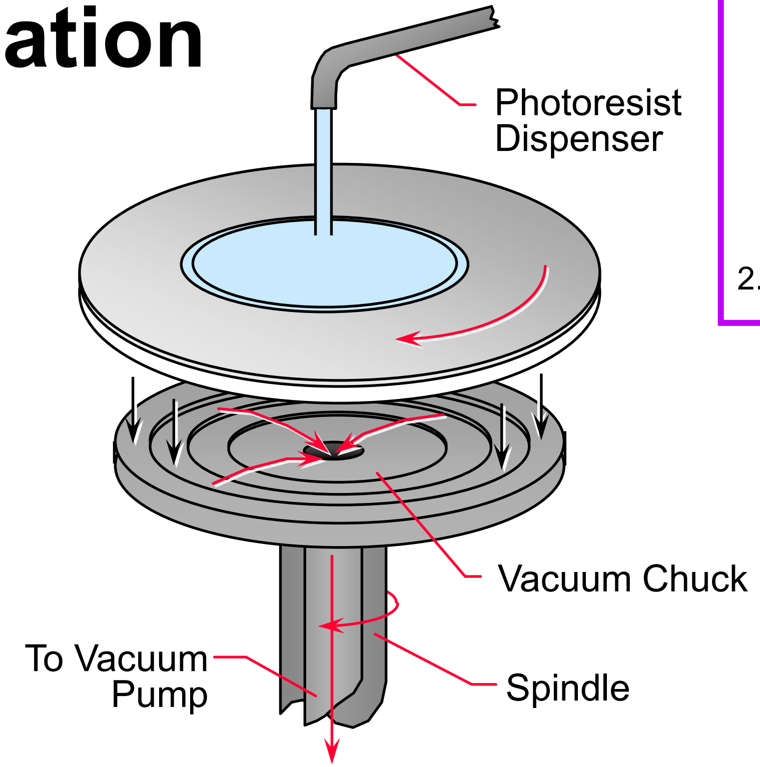


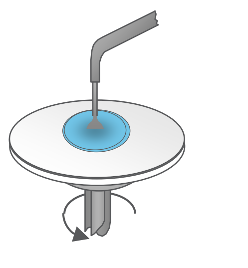
Better Profile - with BARC



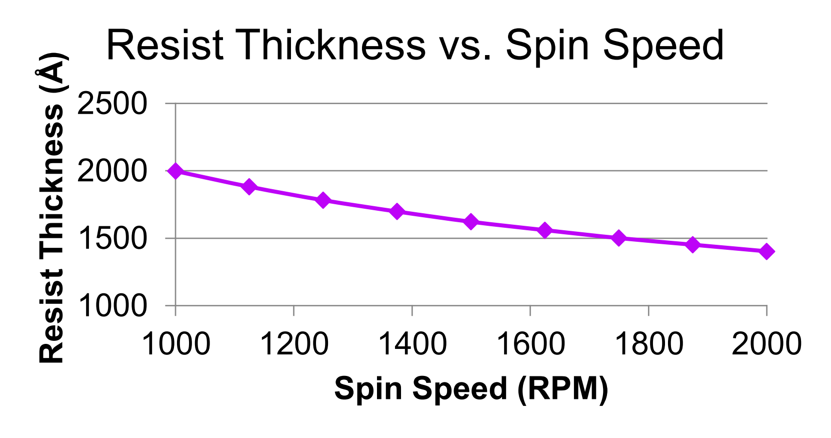


Spin Coat Film - Photoresist Application




2. Spin coat Resist

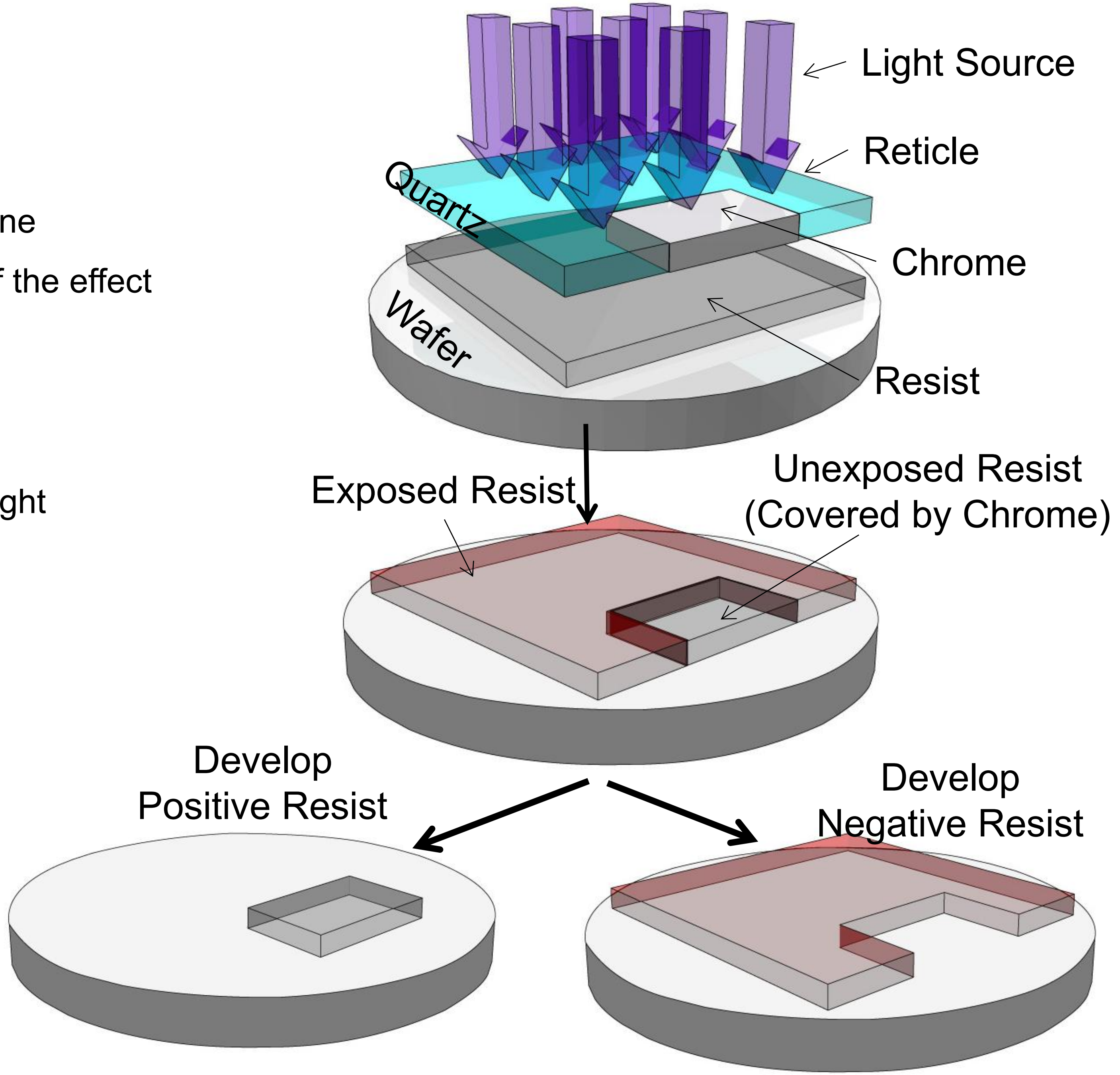
- Photoresist (or resist) – photosensitive polymer used to create a temporary pattern
- Wafer held onto vacuum chuck
- Recipe example:
  - Dispense several ml of photoresist
  - Ramp up spin speed (thousands of rpms) to desired thickness
- Spin speed determines resist thickness (see chart on the right)



Photolithography engineers must identify the optimal photoresist for their specific process - including exposure wavelength, patterning stack, thickness, and resolution requirements. This can also include characterizing new photoresists collaborating closely with photoresist vendors to qualify emerging formulations and recommend enhancements tailored to advanced lithographic techniques.

Photoresist Tone

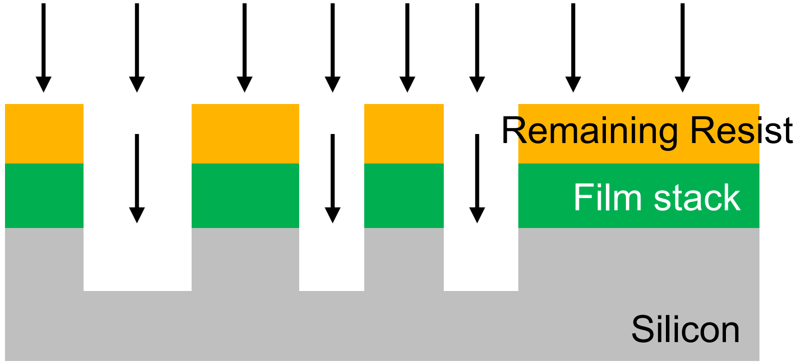
- Resists can be categorized as **positive** or **negative** tone
- For a positive develop process, here is a description of the effect of resist tone:
  - **Positive** tone resist photo process
    - Removes regions of resist exposed to light
    - Leaves on wafer regions of resist not exposed to light
  - **Negative** tone resist photo process
    - Removes unexposed regions of resist
    - Leaves on wafer regions of resist exposed to light



Photoresist thickness for Etch process

- Resist patterns are typically used by an Etch process or by an Ion Implant process
- Resist is consumed during the Etch process.
- As the schematic on the right shows, at the end of the Etch process typically there should still be some remaining resist protecting the stack.

Before Etch process



After Etch process

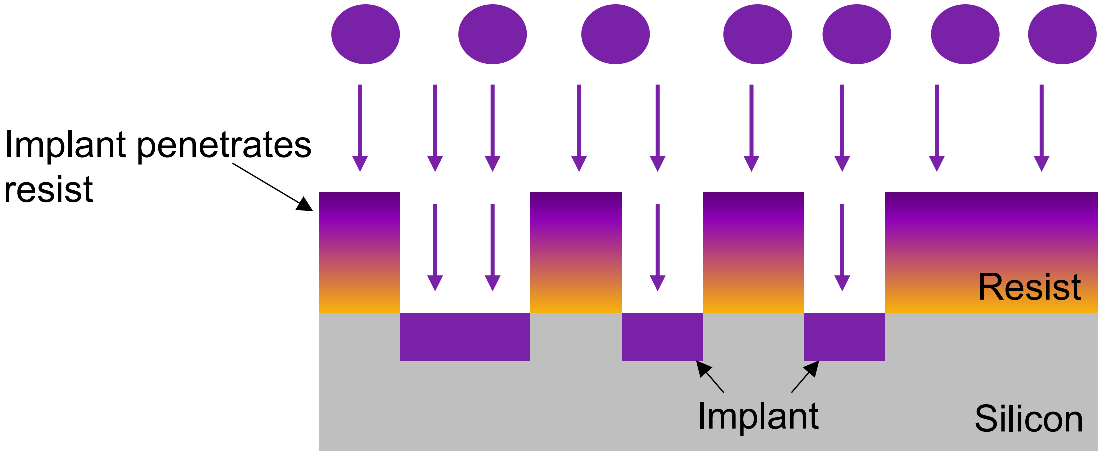
Photolithography Engineers work with **Etch Engineers** to characterize the relative etch rates between the resist and the various materials in the film stack and calculate the resist thickness required to ensure enough resist remains after the Etch process.

Photoresist thickness for Ion Implant process

- Resist patterns are typically used by an Etch process or by an Ion Implant process.
- Resist is used during the Ion Implant process to protect certain regions of the wafer from receiving implants.
- As the schematic on the right shows, implants penetrate the resist, so the resist needs to be thick enough to prevent implanting the film below.

Before Ion Implant process

Photolithography Engineers work with **Implant Engineers** to understand the Ion Implant recipe parameters (species, energy, dose) and calculate the required resist thickness.



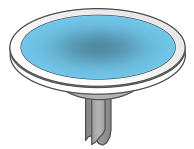
After Ion Implant process

Edge Bead Removal (EBR)

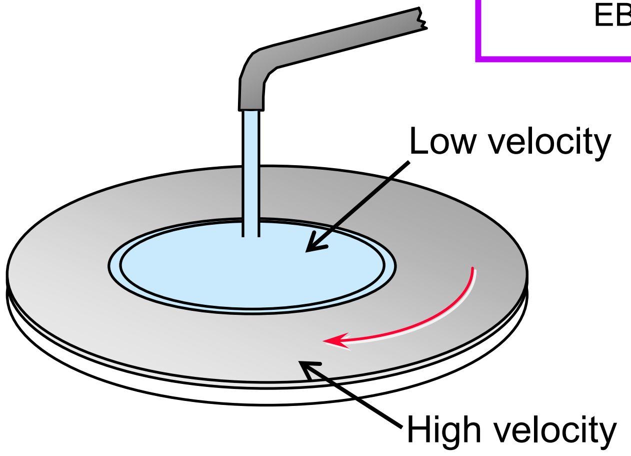
- Photoresist solvent evaporates more quickly at the edge of the wafer than any other place on the wafer because the wafer's radial velocity is greatest there.
- This is a result of both axial and radial airflow dynamics influencing the rate at which solvent is evaporated.
- The rapid loss of solvent forces viscosity to increase, establishing a higher concentration of solids in the moving liquid piling up at the edge of the wafer.
- Consequently, resist thickness is increased.
- This thick region or "bead" of photoresist is called edge bead.
- For some processes, this bead is undesirable, so it needs to be removed. But for other processes this bead is actually desirable, and it is kept on the wafer.
- Following the Coat process, while the wafer is still in the coat module, the edge bead is addressed using chemical (solvent) or optical means.

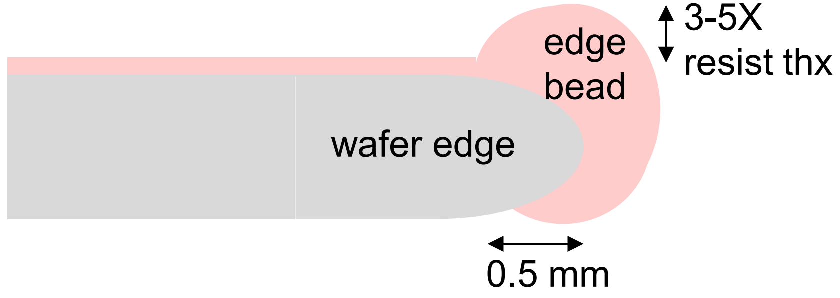
Photolithography Engineers need to determine the specific methodology to address EBR for their processes.

Edge Bead Removal

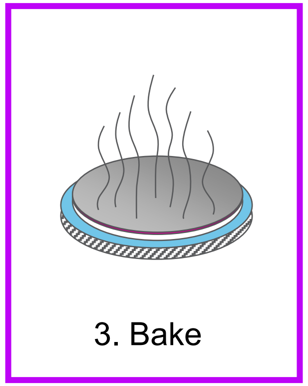


EBR

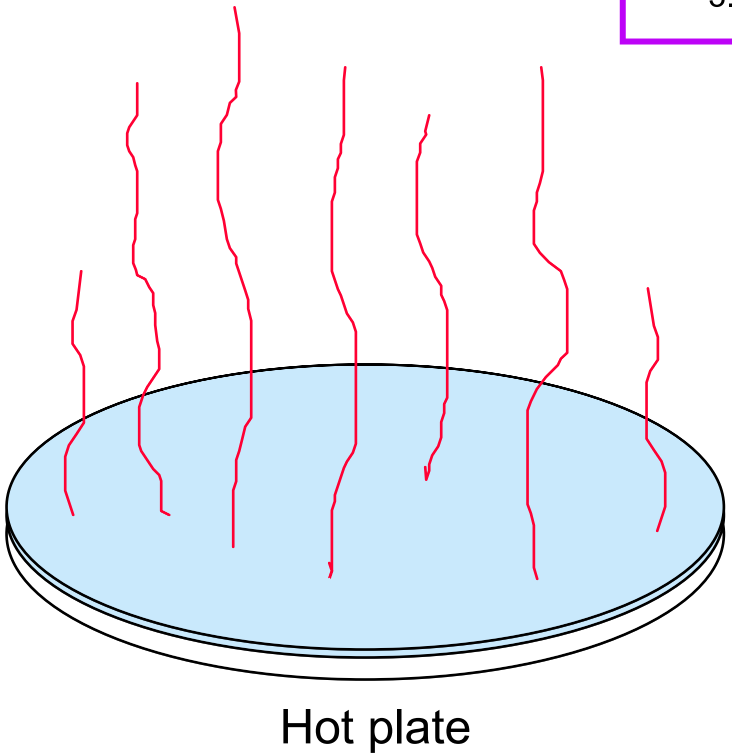




Soft Bake



- Soft bake evaporates excess solvents from the resist and solidifies/hardens the spun-on film.
- Sets the resist in preparation for exposure
- Soft bake improves resist adhesion and reduces out-gassing during exposure
- The soft bake key recipe parameters are time (a few minutes) and temperature (~100 to ~200°C)



Photolithography Engineers need to identify the appropriate soft bake recipe parameters for their specific film and application.

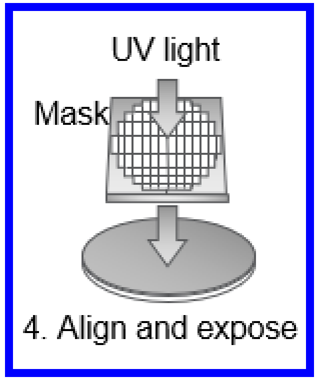
Alignment and Exposure

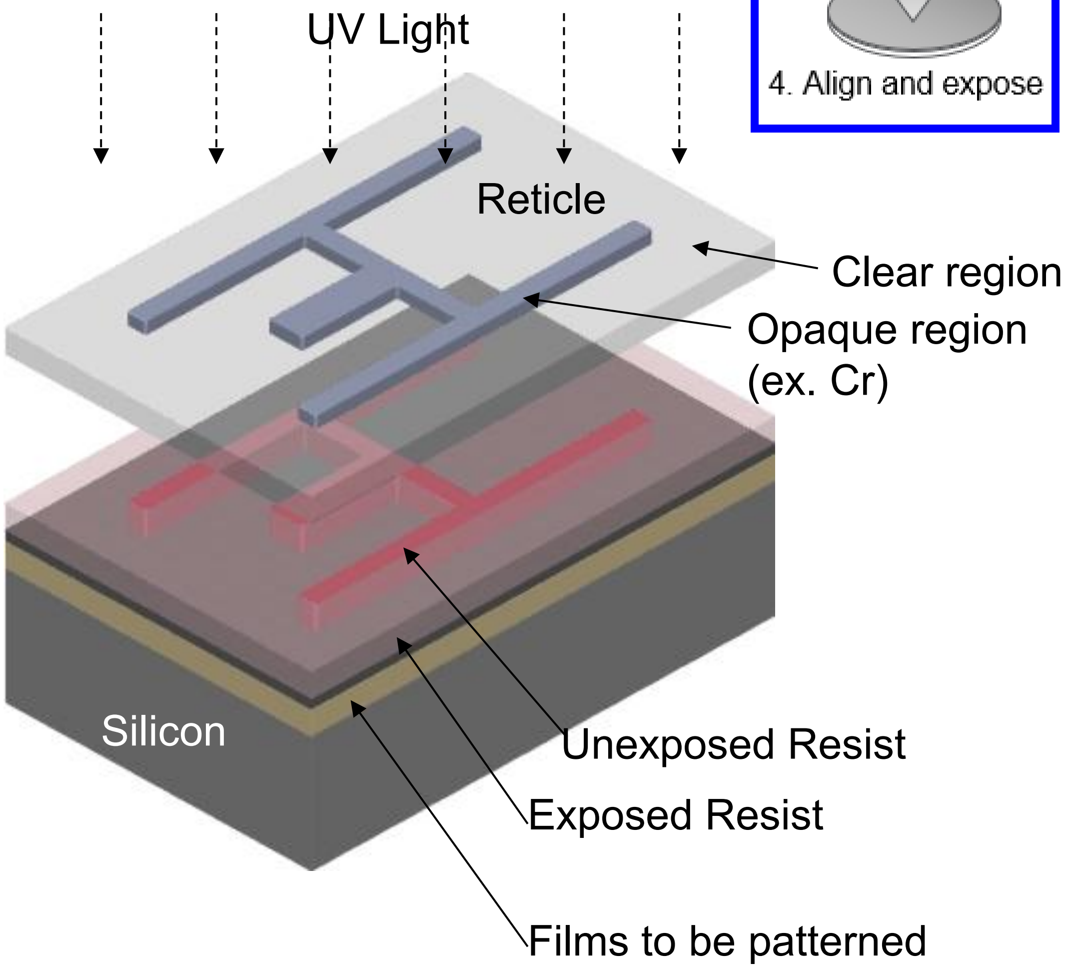
Alignment:

- Aligns current pattern to previously existing pattern
- Special structures are created on wafer which are used to align the wafer

Exposure

- Exposes resist film with UV light passed through a patterned reticle
- Exposure activates photo-sensitive components of photoresist
- Key parameters of the exposure process are dose (energy) and focus (distance between the wafer and the lens)



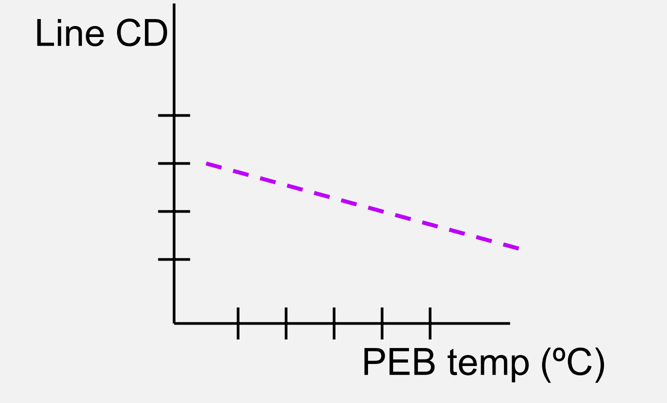


Photolithography Engineers dedicate significant effort - spend most of their time - optimizing this step. Need to ensure precise alignment/overlay/CD control, and validate the process is repeatable, fast and uniform.

Post-Exposure Bake (PEB)

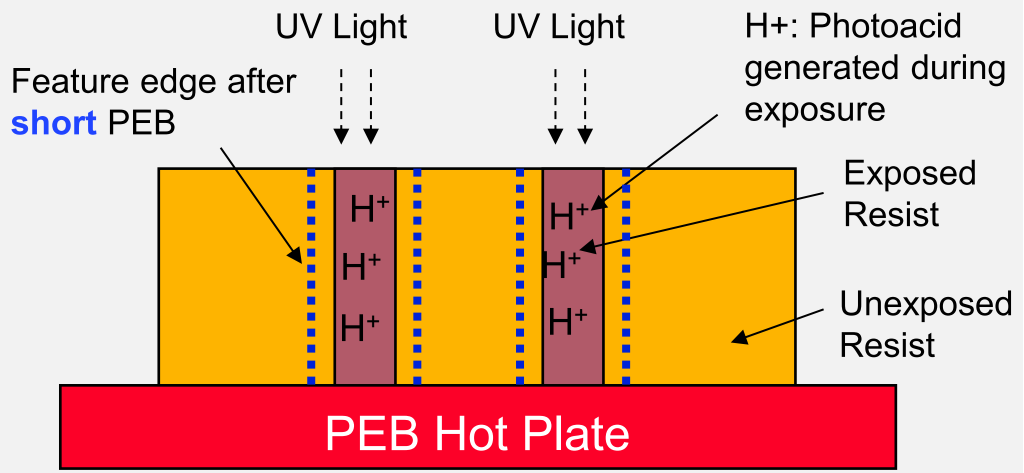
- Completes chemical reactions that are initiated during exposure
- Positive tone resist line (CD) shrinks with PEB driven acid diffusion
- CD is highly sensitive to PEB temperature, duration, and thermal uniformity. Variations in these parameters can lead to CD drift, line-edge roughness, and pattern fidelity issues.
- Quenchers (base additives) are used to limit acid diffusion
- The wait time between exposure and PEB and the thermal ramp rate during PEB also affect CD uniformity.

Photolithography Engineers must identify the optimal PEB parameters, and ensure repeatability (wafer to wafer/run to run) and uniformity across the wafer

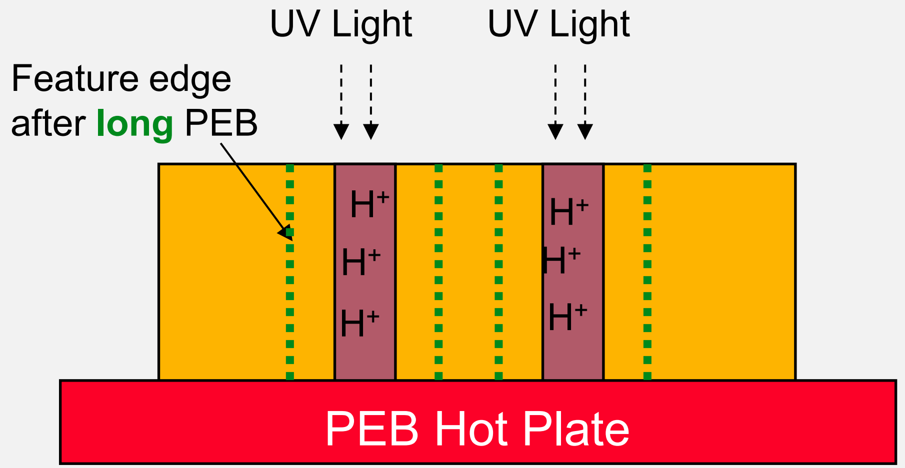


Example trend for positive resist

Post-exposure bake (PEB) – Positive resist example



Shorter Post-exposure bake (PEB) Line CD

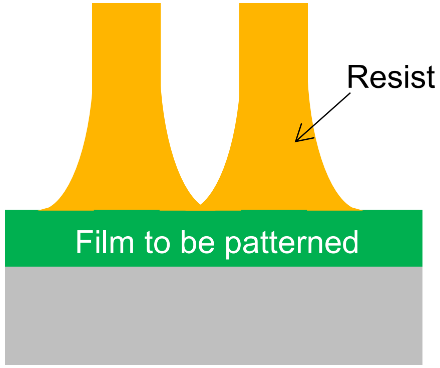


Longer Post-exposure bake (PEB) Line CD

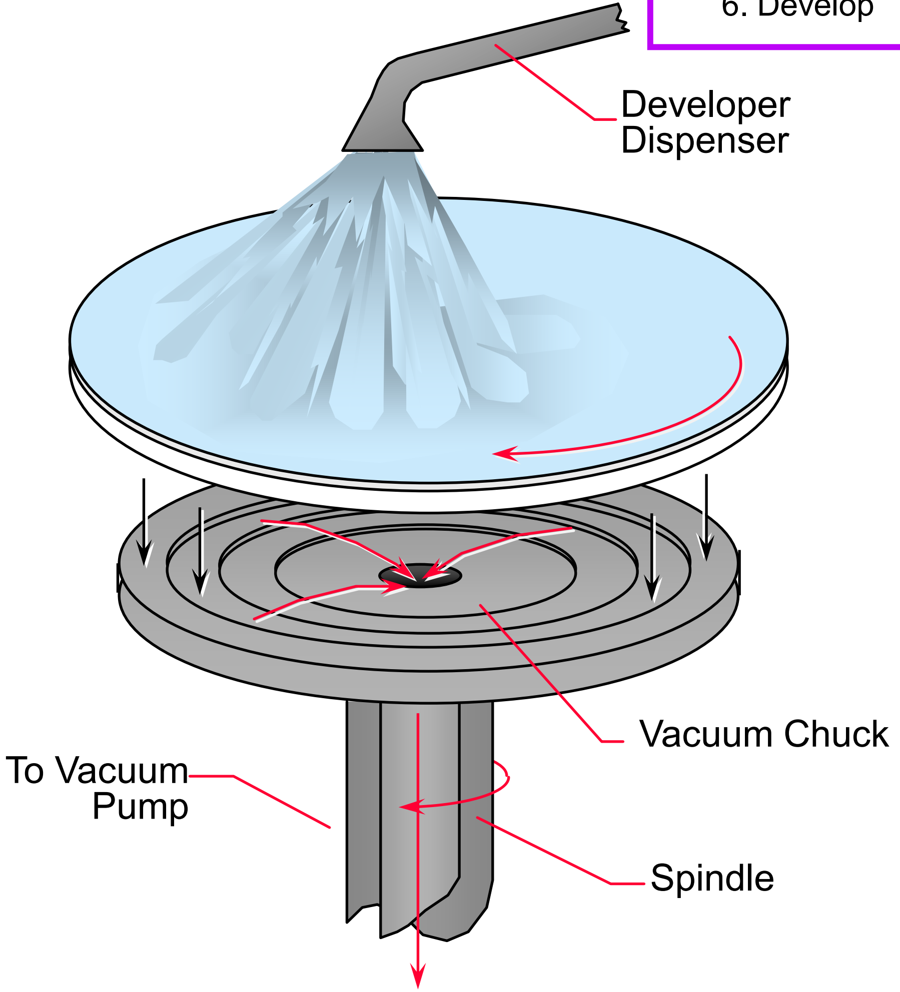
Develop

- Soluble areas of photoresist are dissolved by developer solution
  - TMAH: tetra methyl ammonium hydroxide in water
    - Used for positive and negative tone resist (case 1-2 in next slide)
  - nBA: n-butyl acetate
    - Negative tone developer for positive resist (case 3 in next slide)
- Surfactants may be added to minimize capillary forces that may cause resist line toppling/collapsing
- Developer process needs to be tuned for individual resists
- Key parameters: Hardware (nozzle type, bowl shape, etc.), flow rate, duration, location of developer dispenser, spin parameters (speed, etc.), filtration, rinse, etc.

Photolithography Engineers must identify the optimal Developer process to improve CD uniformity and minimize defectivity like toppling, underdeveloped resist, unwanted (redeposited) resist, etc.



Example of underdeveloped resist

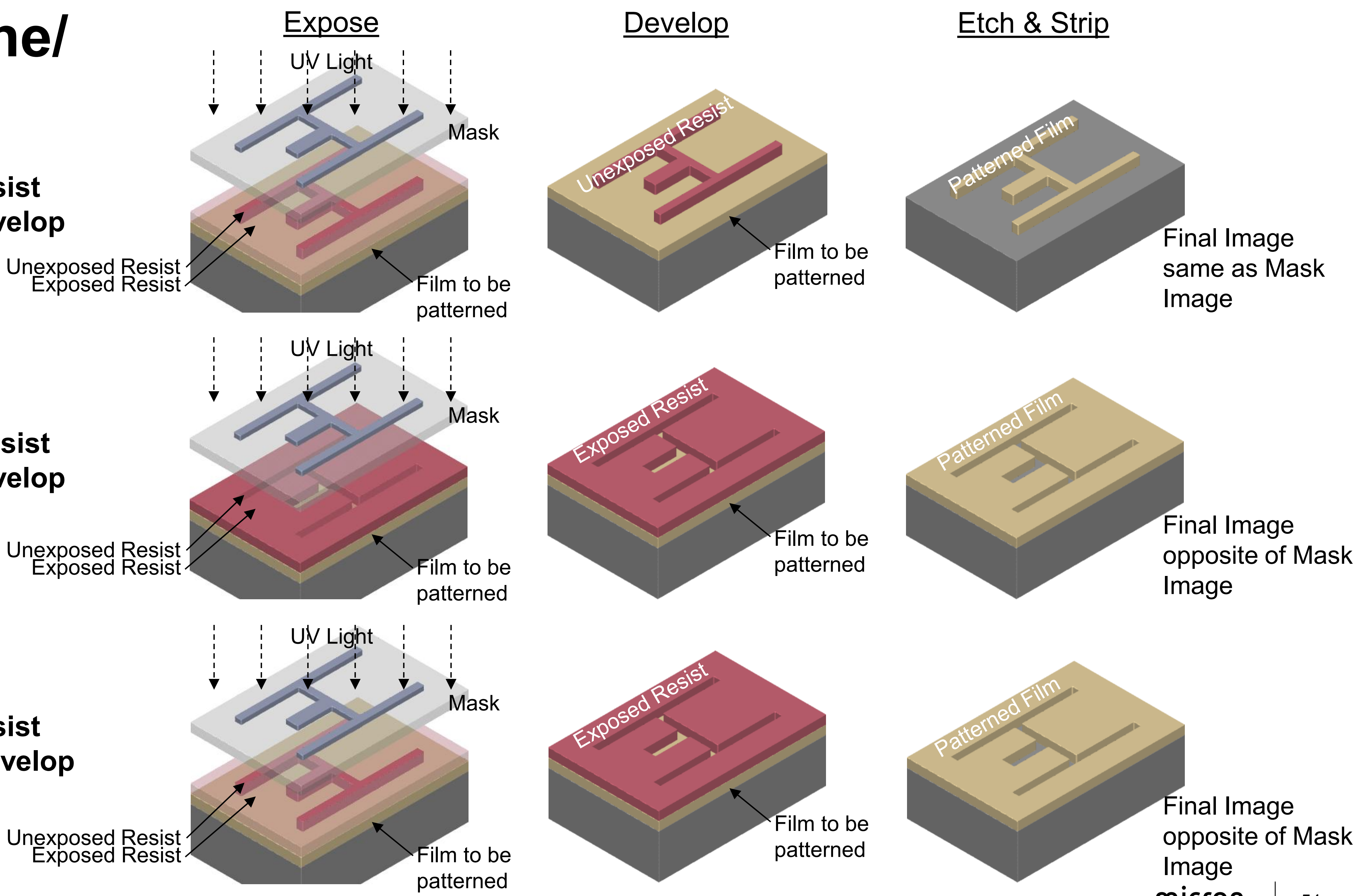


Resist Tone/ Develop

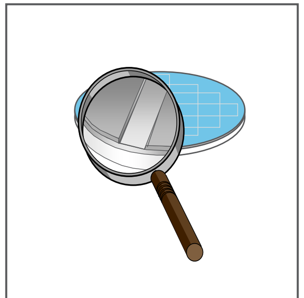
Case 1 **Positive Resist Positive Develop**

Case 2 **<u>Negative</u> Resist Positive Develop**

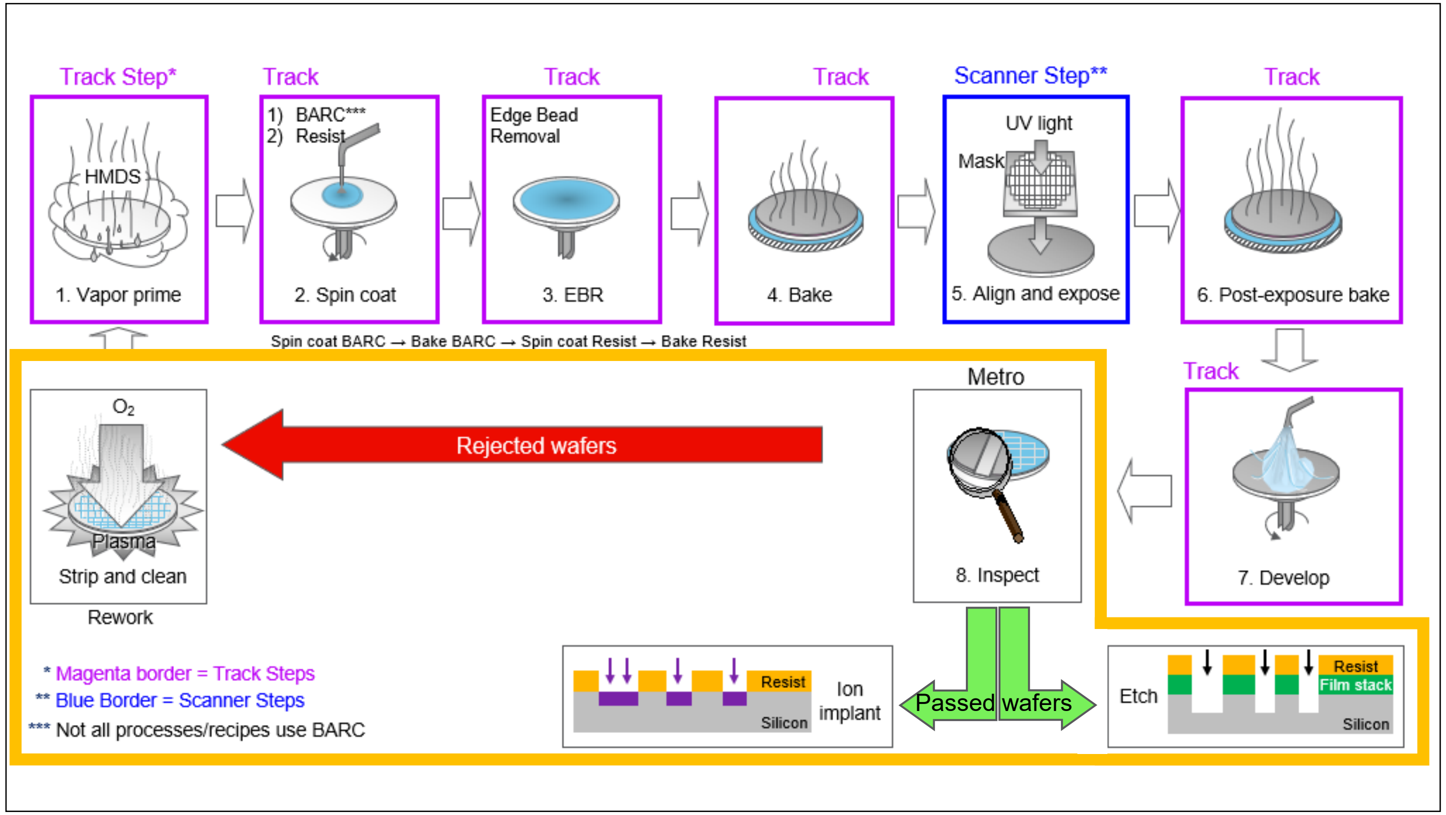
Case 3 **Positive Resist <u>Negative</u> Develop**



Inspect

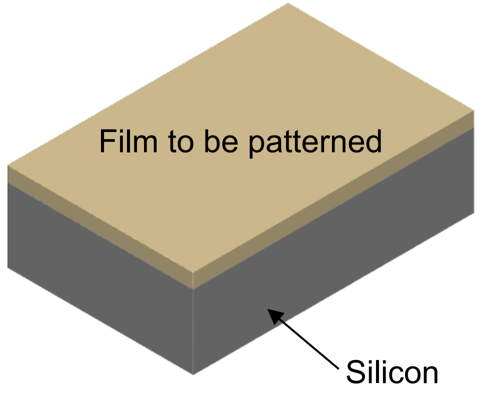


- Inspect
  - Inspect the wafer for pattern integrity and defects
  - Measure critical dimensions (CDs)
  - Check overlay accuracy
- Pass inspection: Wafer continues to next area for further processing (Etch, Ion Implant, etc.)
- Fail inspection: Wafer is reworked
  - Wafer goes to Resist Strip (to remove the resist)
  - Photo process starts over

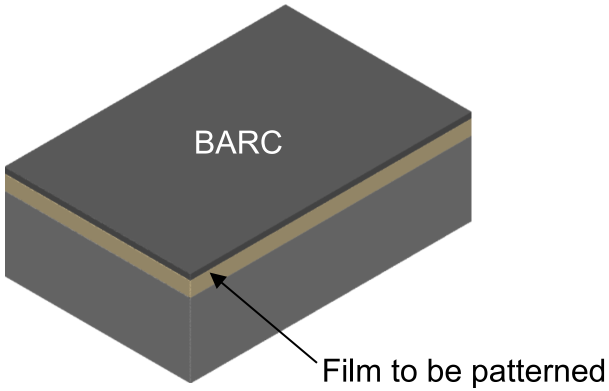


Note: inspections after Develop have the advantage that rejected wafers can be reworked. But after the wafer went through Etch or Implant wafer cannot typically be reworked and needs to the scrapped.

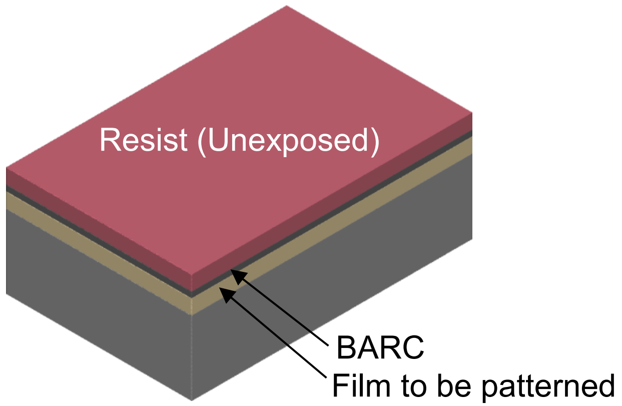
Patterning Process Flow – High Level Overview



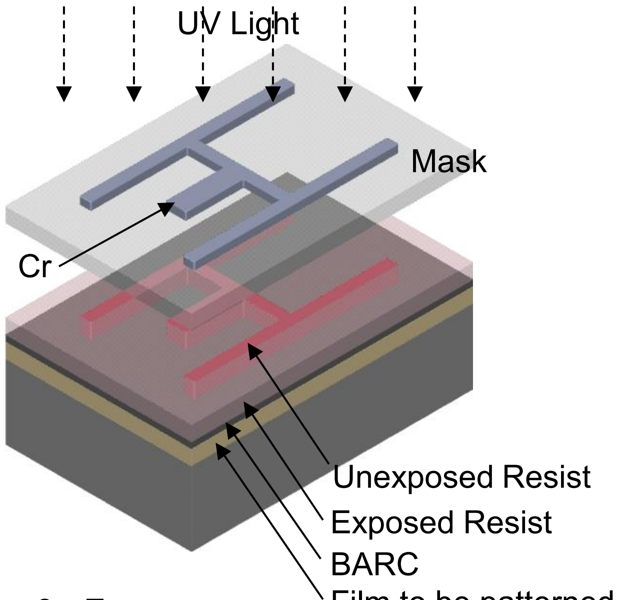
Silicon Wafer with Film to be Patterned
(one film or a film stack)



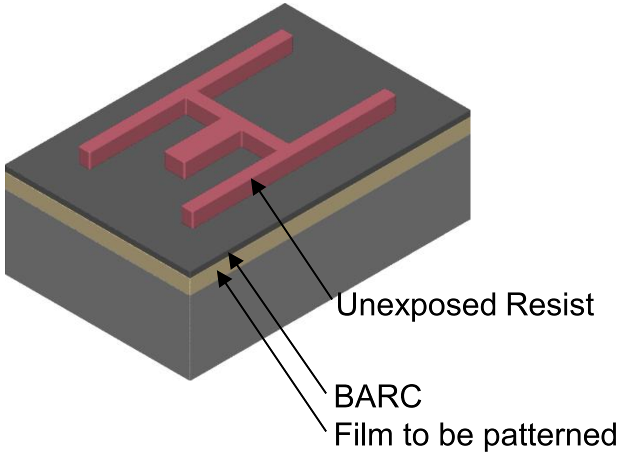
1: BARC Coat
(used is some processes)



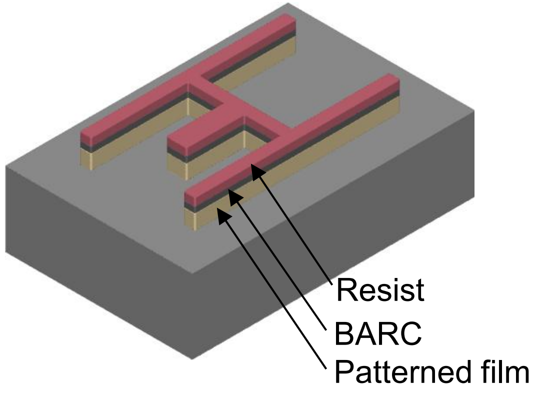
2: Resist Coat



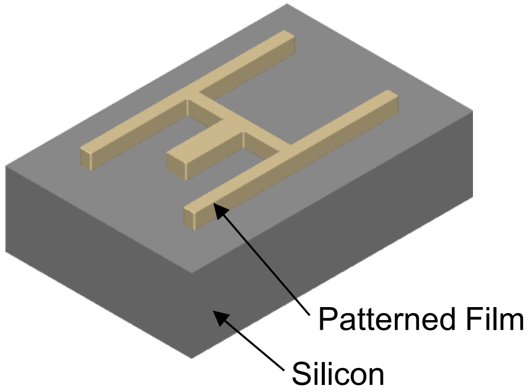
3: Expose



4: Develop
(Positive Resist/Positive Develop depicted)



5: Etch



6: Resist and BARC Strip

Photo Processes – Summary

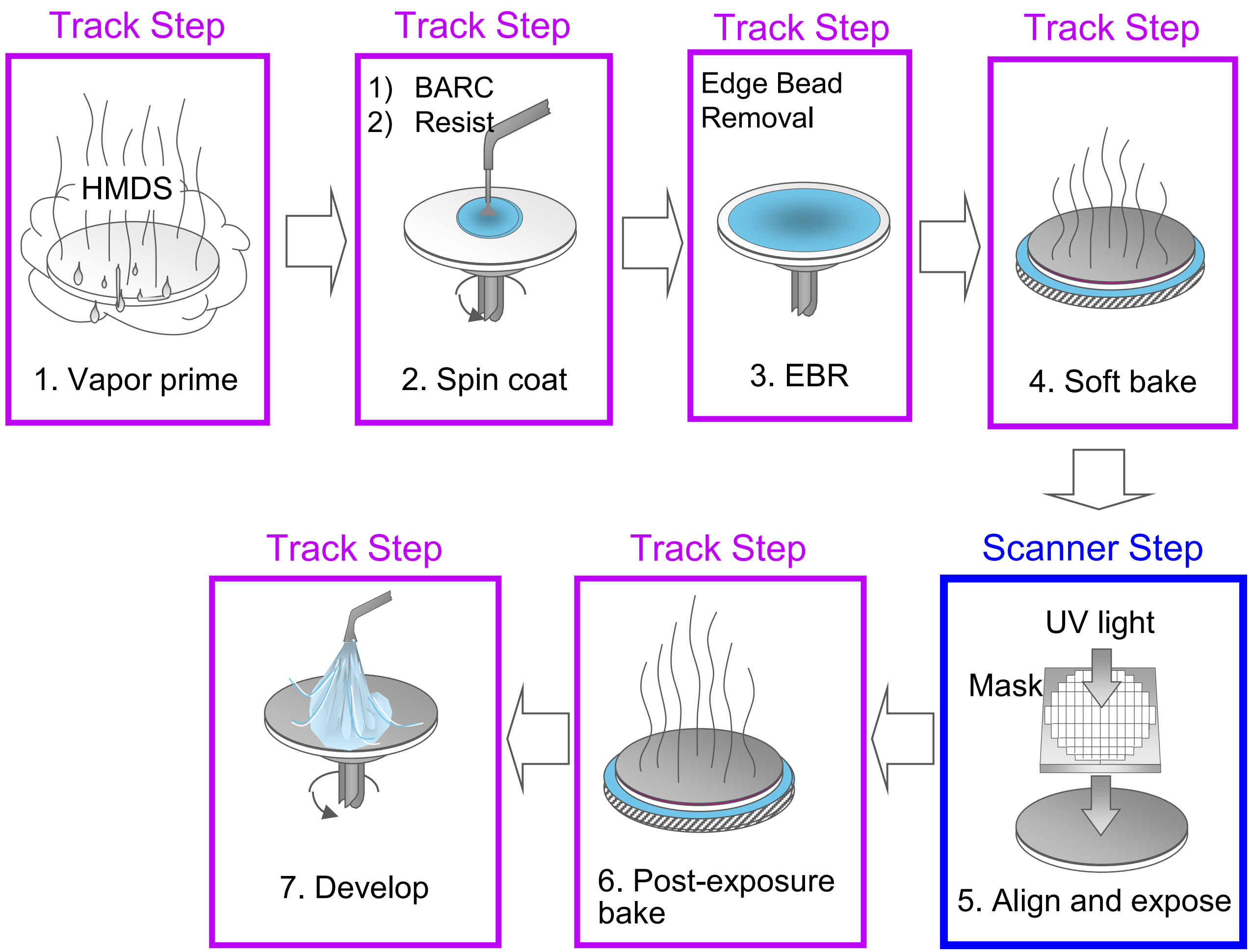
Process	Chemical(s) Used	Tool	Purpose
Vapor Prime	HMDS	Track	Remove moisture from the wafer surface to promote adhesion of resist.
BARC coat	BARC	Track	Deposit a layer of antireflective coating at a target thickness before depositing resist (for some processes). Helps with reflectivity and uniformity. BARC films are typically carbon-based polymers.
Resist Coat	Photoresist	Track	Deposit a very uniform layer of resist at a target thickness.
EBR	Solvent	Track	Edge bead removal. Remove the thicker resist at the very edge of the wafer.
Softbake	n/a	Track	Remove solvents from the resist in preparation for exposure.
Alignment	n/a	Scanner	Ensure the pattern to be printed is correctly positioned with respect to the pattern already on the wafer.
Exposure	n/a	Scanner	Transfer the pattern on the reticle into the resist layer.
Post Exposure Bake	n/a	Track	Minimize standing waves in the resist, complete the exposure process for DUV.
Develop	TMAH (positive and negative tone resist) nBA (negative tone develop) Surfactants (sometimes)	Track	Soluble areas of the photoresist are dissolved by developer solution after Exposure.

Equipment used in Photolithography

micron

Track Modules and Scanner

- Track and scanner typically linked (see picture) to meet critical timing between steps and to minimize contamination
  - This is known as a linked system or cluster
- Tracks and scanners manufactured by different vendors



Track

- Tracks perform the following operations:
  - Application of chemicals to the wafer (resist, developer, etc.)
  - Heating and cooling of the wafer
- Track typically linked to scanner, but in some cases it can be stand-alone for certain coat-only processes or develop processes
- Some modules of the track have windows which allows us to observe the process (see picture)

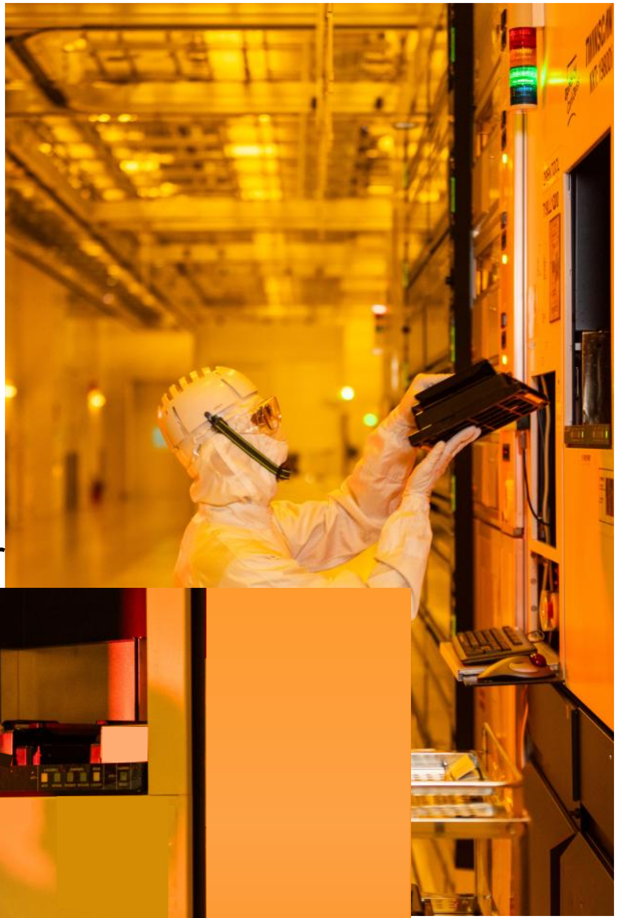
Photolithography Equipment Engineers work with Fab layout and facility team to ensure on-time installation and operation of equipment. They are responsible for the maintenance of toolsets (hardware, software and system interfaces). They develop and optimize existing equipment to meet productivity requirements, and identify, diagnose and resolve equipment related problems.

Track FOUP Load

- Picture shows the side of the Track where FOUP boxes are loaded into the tool. FOUP: Front Opening Unified Pod.
- A FOUP is a rigid, sealed plastic pod designed to:
  - Protect wafers from contamination during transport and storage.
  - Enable automated handling by interfacing with robotic systems and load ports.
  - Maintain a controlled environment, often with purge gas capabilities
  - Transport up to 25 300-mm diameter wafers
- The FOUPs are transported by the AMHS system. AMHS: Automated Material Handling System
- Tracks can have over 100 wafers inside at a time in internal racks and modules.

Scanners

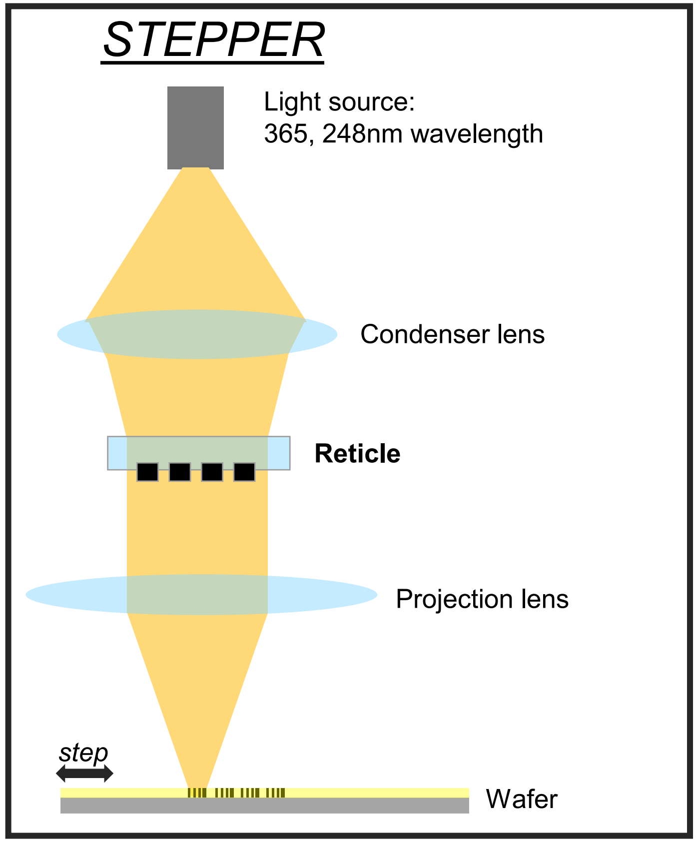
- The Reticles are loaded into the scanner
- Scanners perform the align step, map the wafer surface and adjusts the wafer stage vertically to keep image in focus, and perform the exposure step
- Reticle and wafer stage move to expose every die on the wafer
- Scanners by wavelength:
  - 365 nm (I-line)
  - 248 nm (DUV)
  - 193 nm (dry)
  - 193 nm (immersion)
  - 13.5 nm (EUV)

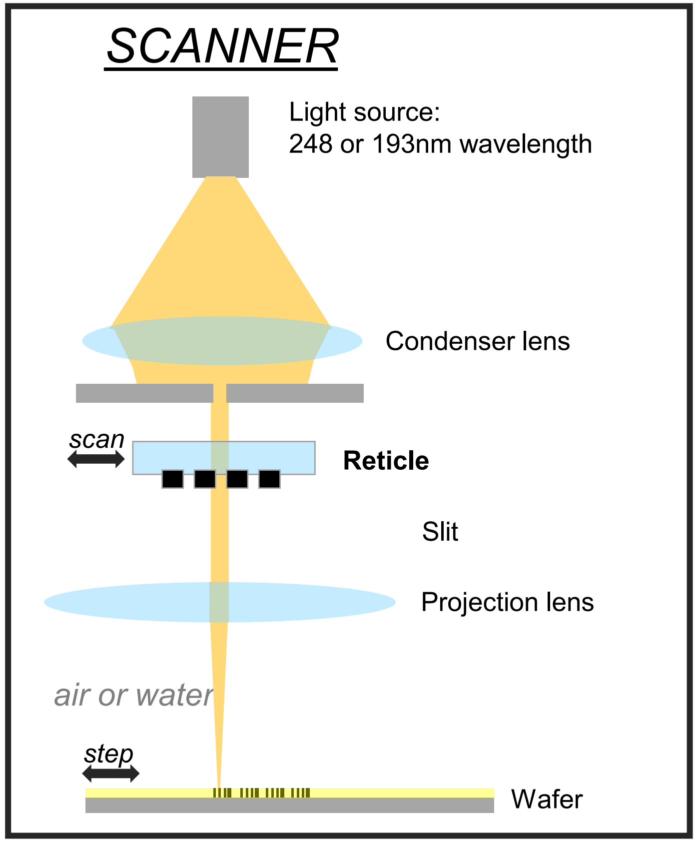


Engineer loading reticles in scanner

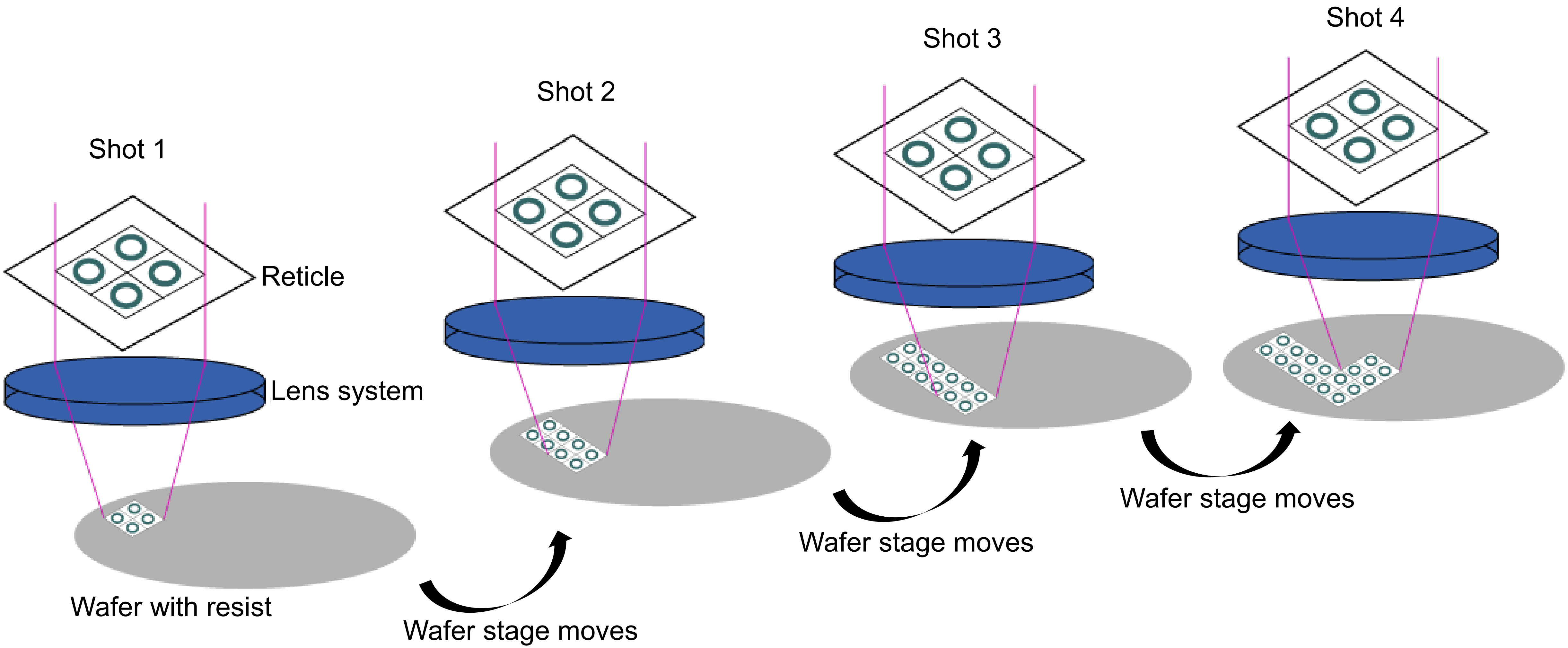
Stepper versus Scanner

- Stepper Technology
  - Stepper projects the whole reticle field at once
  - A light source (such as a mercury i-line lamp or a KrF laser) projects light through a condenser lens and a reticle onto a wafer. The reticle contains the pattern to be printed, and the projection lens reduces the image size typically by a factor of four.
  - This technology is typically used for wavelengths of 365nm and 248nm.
- Scanner Technology
  - Operates similarly to stepper technology but uses a scanning motion to project the pattern onto the wafer through a slit. This allows for higher precision.
  - Scanner technology is used for wavelengths of 365nm, 248nm, 193nm and EUV.



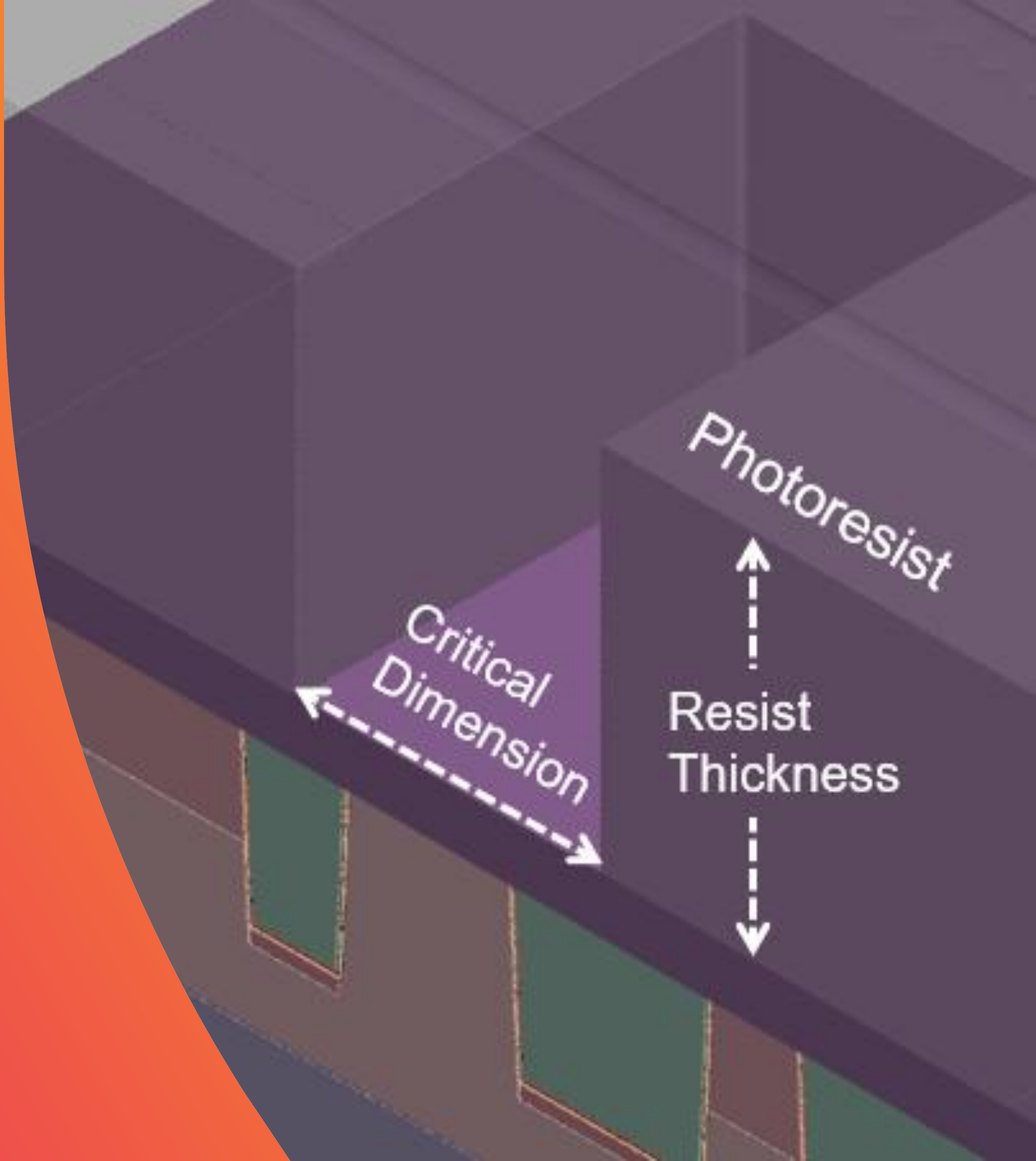


Stepper illustration



100+ shots may be needed to cover the whole wafer
Efficiency opportunity: fit in a reticle as many die as possible to minimize number of shots

Primary Measurements in Photolithography



Photolithography Measurements

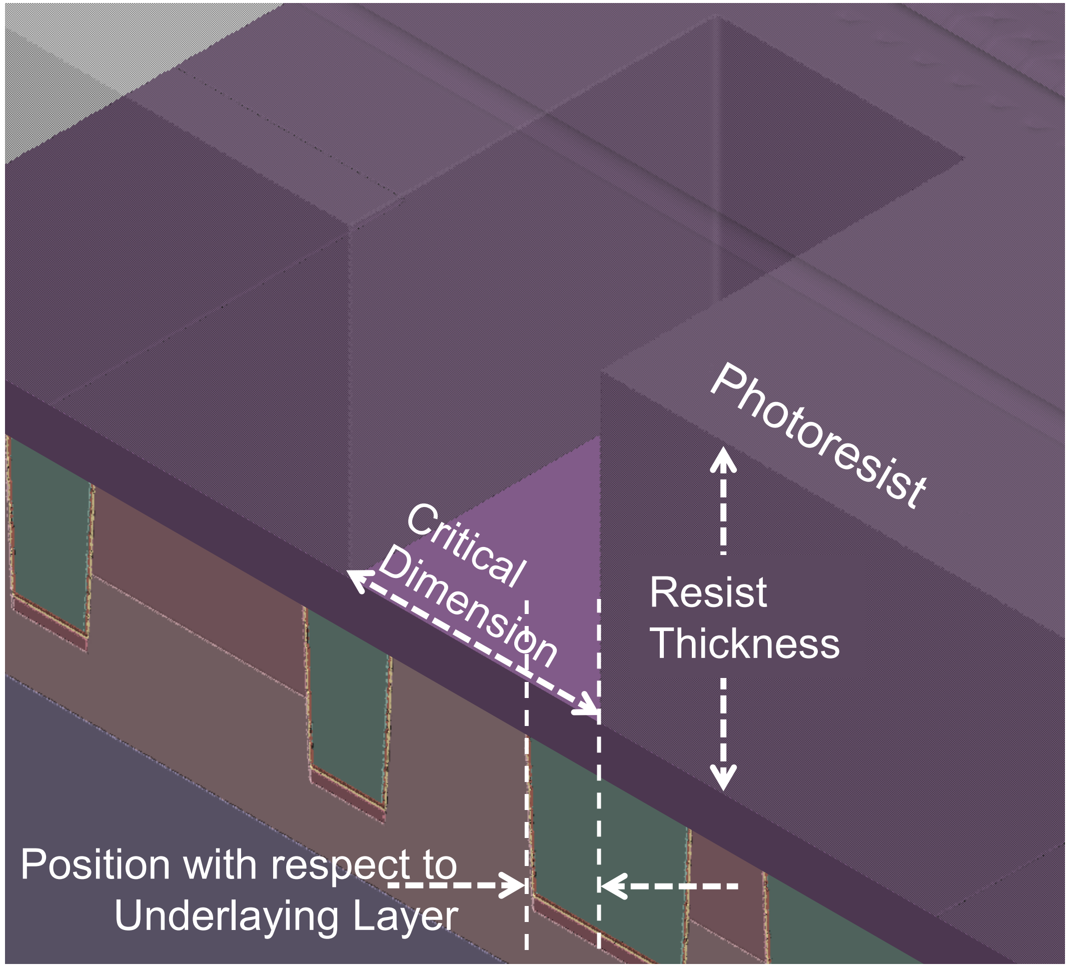
Metrology is key to ensure the resist pattern is on target

<u>Resist Thickness</u>: After resist is spun on the wafer, its thickness is measured to ensure the pattern will form correctly.

<u>Particle Monitor</u>: measure defectivity on resist coat on wafer to ensure resist meets quality requirements.

<u>Critical Dimensions (CD's)</u>: After the resist pattern is developed, the printed features are checked to ensure they are the correct size required by the circuit design.

<u>Registration</u>: The resist pattern is also checked to ensure it is closely positioned with respect to the previous patterns to ensure that the devices and structures will be correctly formed and will operate properly. This measurement is also known as "Overlay".

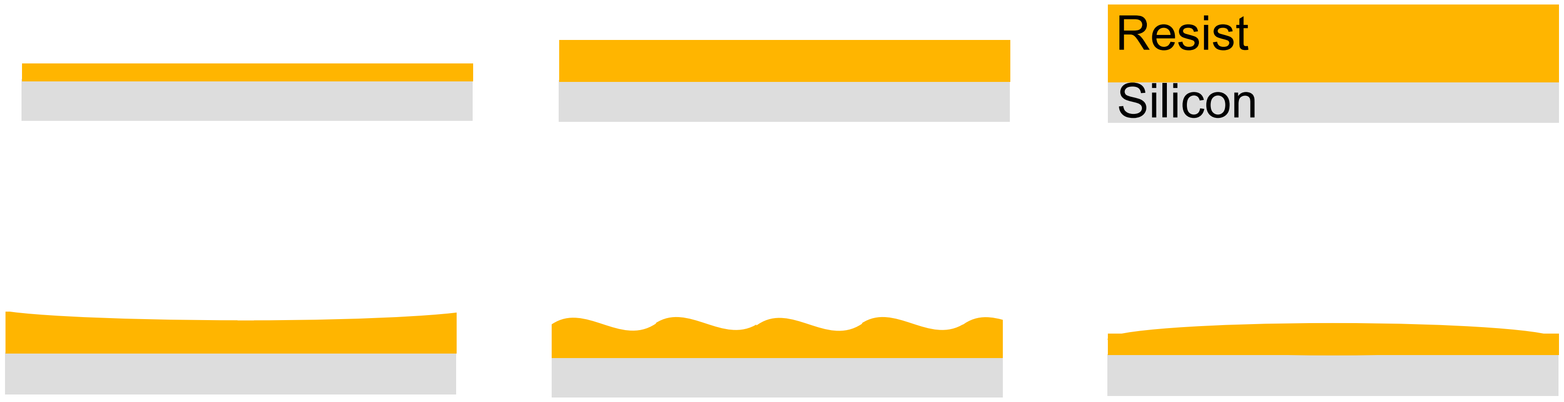


Resist Thickness

- **Resist Thickness** can be measured periodically
  - Resist is spun on bare silicon wafer and cured (soft baked)
  - Several measurements are taken per wafer using a spectroscopic ellipsometer
- **Mean Resist Thickness** is an average of the measurements
- **Range** is calculated by subtracting the lowest measurement from the highest measurement

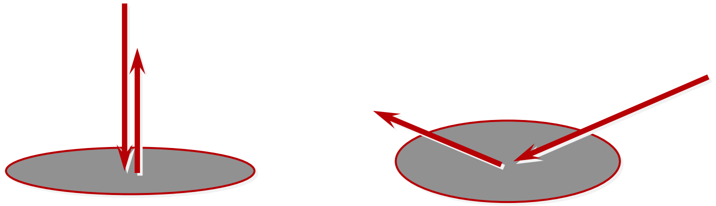
What is ellipsometry?

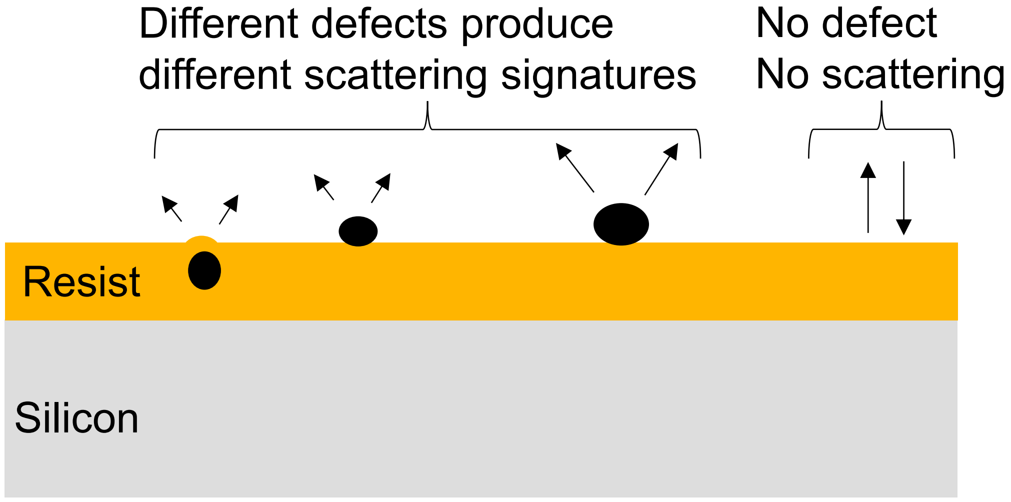
This technique measures the intensity of reflected light at different wavelengths to determine film thickness. This principle is widely used in semiconductor manufacturing because it is non-destructive and highly accurate for thin films.



Particle Monitor Measurement

- Goal: measure particles/defectivity on resist coat on wafer to ensure resist meets quality requirements.
- This measurement provides information about particles and surface defects. For example:
  - Number of defects
  - Location of defects
  - Size of defects
- Theory of operation
  - Illuminates spinning wafer with a stationary laser
  - Uses either normal or oblique incident laser beam
  - Collects scattered light from particles
    - The scattering power of the defect is proportional to the diameter of the defect. The scattering power drops significantly with a reduction in sphere size.
  - Sizes and counts particles



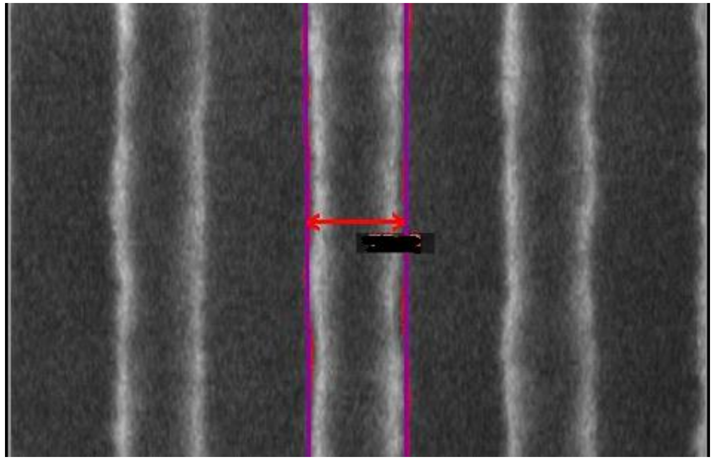


Scattering schematic

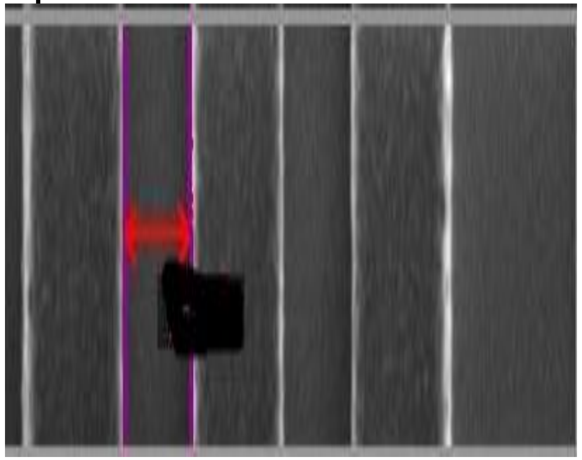
CD Measurements

- Critical Dimensions (CDs) are measured on resist features to verify the scanners are printing the desired dimensions and the process is in control
- If the CDs are out of spec the wafer can be reworked (resist is stripped/removed and Photo process can be done again)
- Typical CD measurements include line width, space width and contact CD
- CD measurements can be taken at the bottom, at the top, or mid-way of the resist
- CDs are generally measured using a CD SEM (Scanning Electron Microscope) technique (see next slide)
- The CD SEM tool can be trained to recognize and locate specific patterns using recipe-driven automation and pattern recognition algorithms

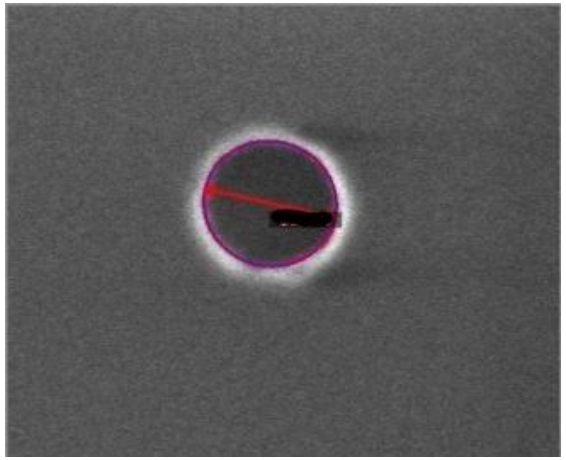
Line

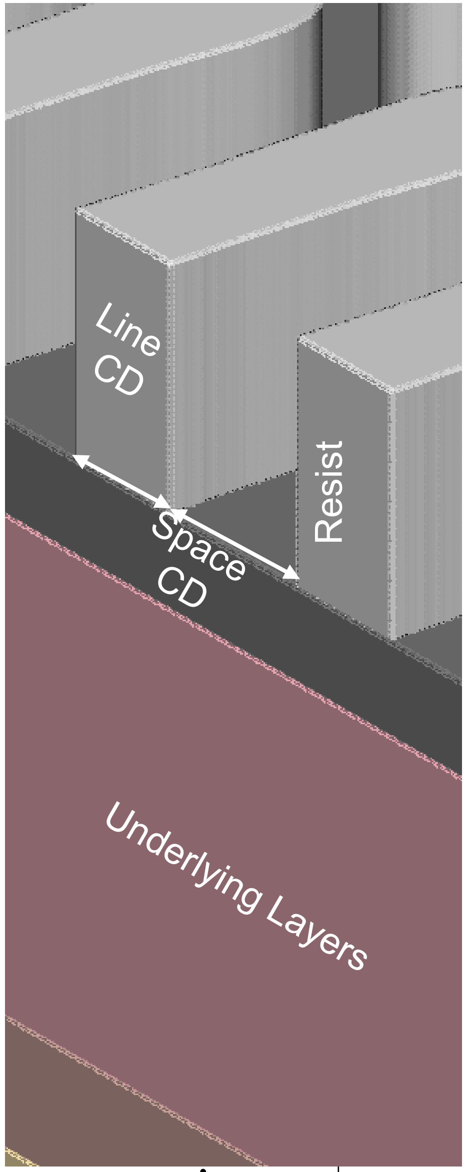


Space



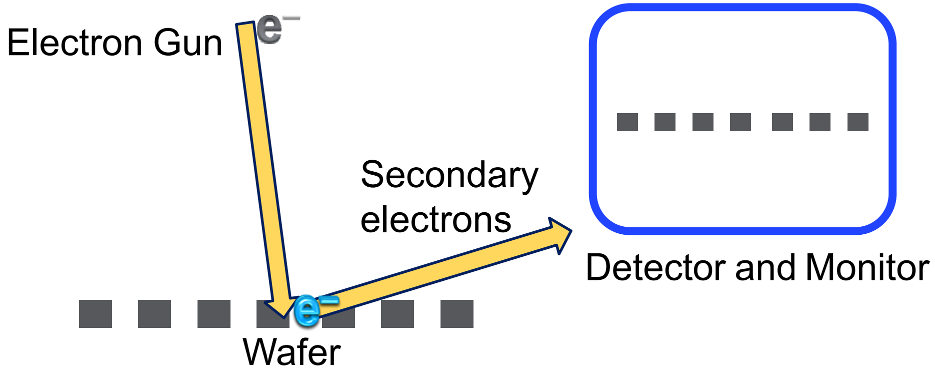
Contact

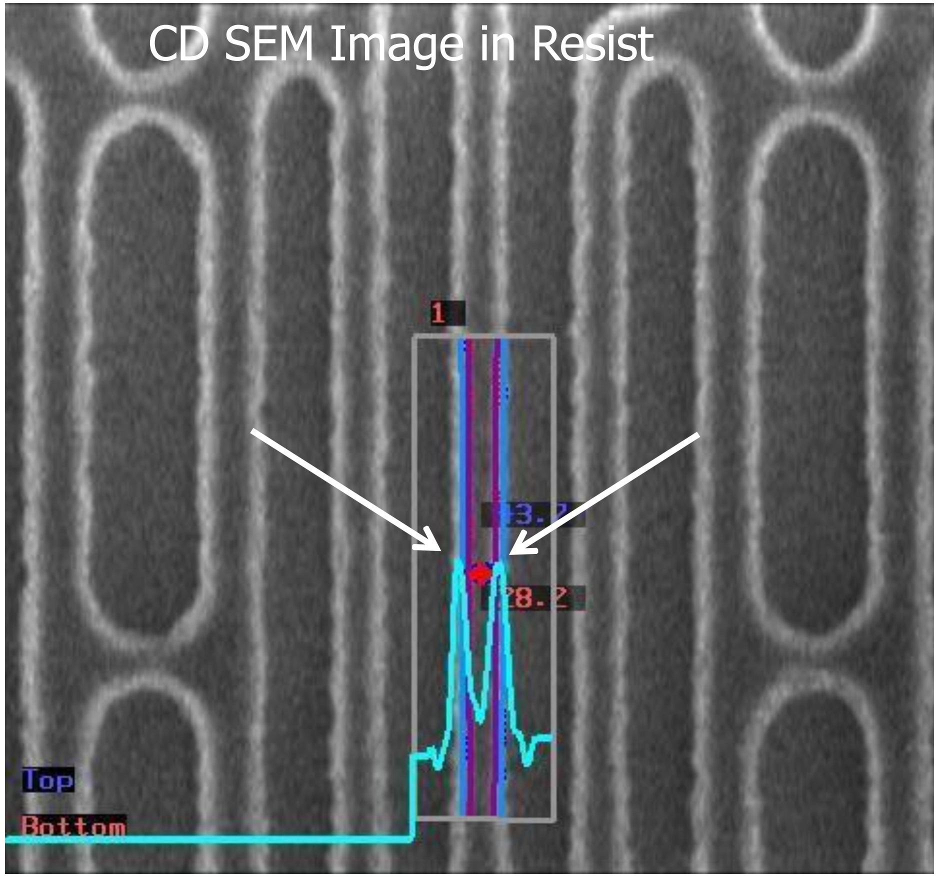




CD SEM Theory

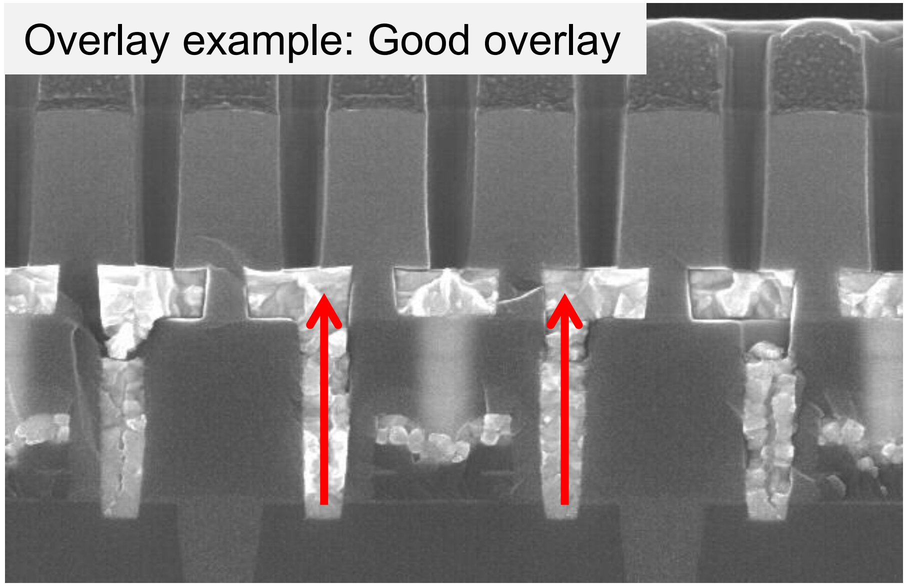
- Wafer is loaded in a CD SEM tool and wafer is transferred to a high vacuum chamber
- The Pattern Recognition software is programmed to find a VERY specific site on a specific die location on the wafer
- A very tightly focused beam of electrons is directed at a small spot on the wafer.
- When the electron beam strikes the sample, “secondary” electrons are released from the atoms of the sample
- The electron beam then scans across the measurement site in a linear fashion. An “intensity profile” of the scan is produced.
- This intensity profile is used to form the image of the sample on a display monitor
- The image is used to generate measurement based on the specific algorithm for the type of feature of interest (line, space, contact, etc.)
- Gray scale changes in the image are used to detect the edges of the feature to be measurement
- In some cases, the waveform can resolve “Bottom CD” vs. “Top CD”
- The process repeats for the next measurement site on the wafer

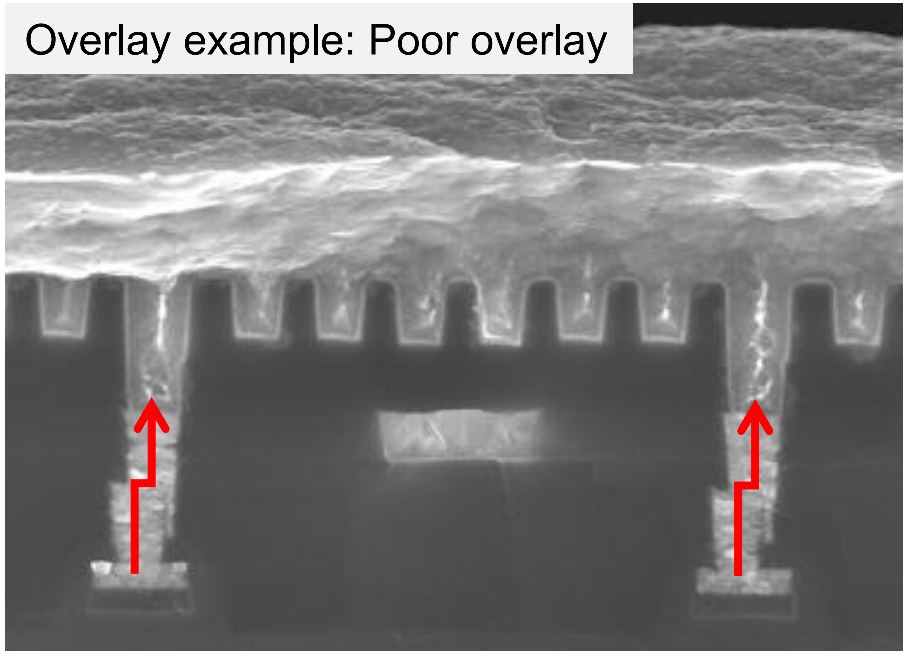




Overlay

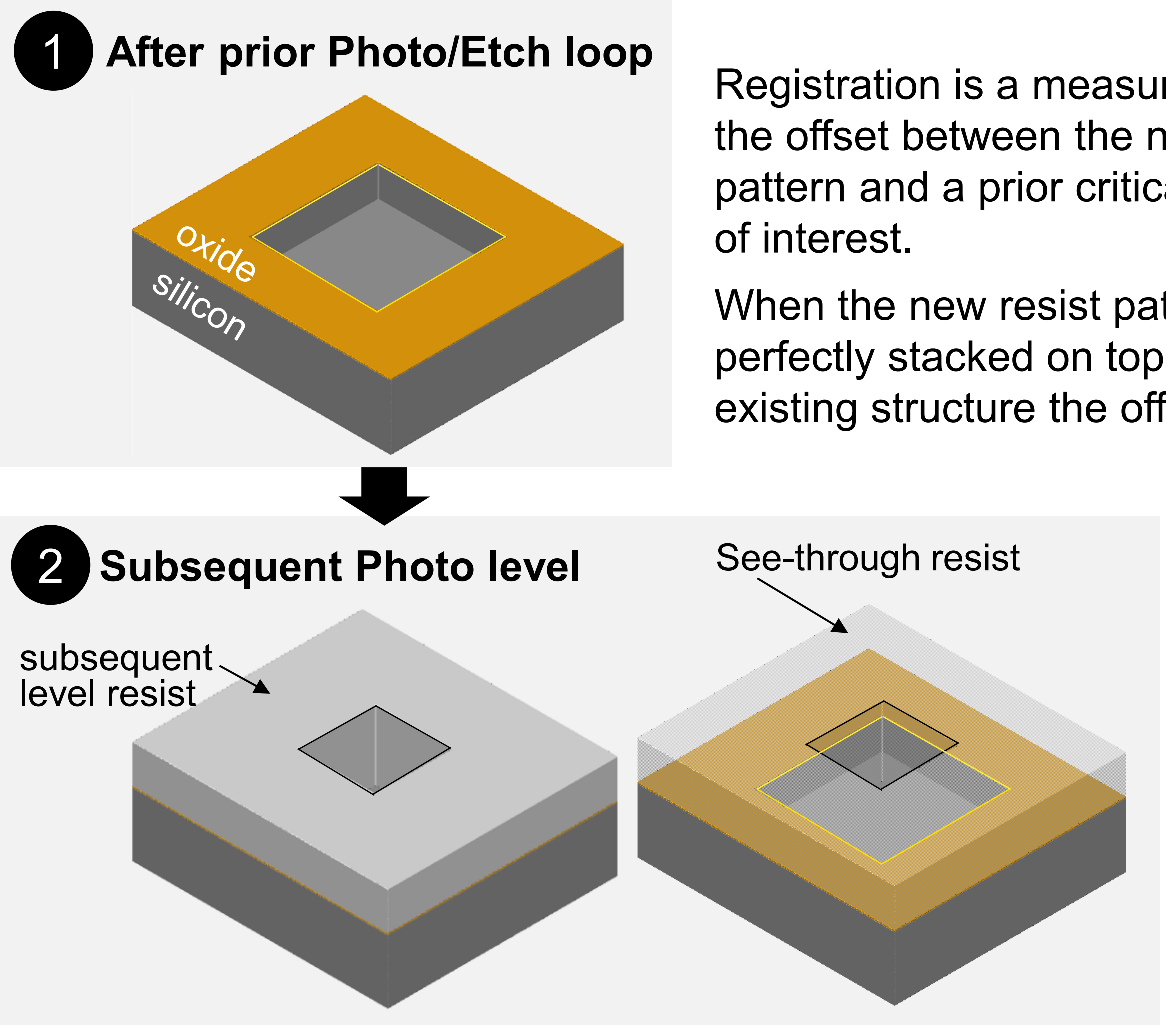
- Photolithography layers: Structures like active areas, transistor gates, contacts and interconnects are built layer by layer, with each layer patterned using photolithography
- In semiconductor manufacturing, precise stacking of structures is critical. The placement of one layer relative to another is known as overlay.
  - Example: Making sure that a contact hole lands precisely on top of a transistor gate
- Overlay metrology systems are utilized to measure layer to layer overlay
- Overlay error: If the pattern from one layer is misaligned with the previous layer, it results in an overlay error. This can cause electrical defects, yield loss, or performance degradation.
- Observe the cross-sections in this slide to compare examples of good overlay versus poor overlay





Registration

Registration is the measurement of how well structures are placed relative to each other. Different types of registration marks and measurement techniques are used. Here is the description of the box-in-box marks.

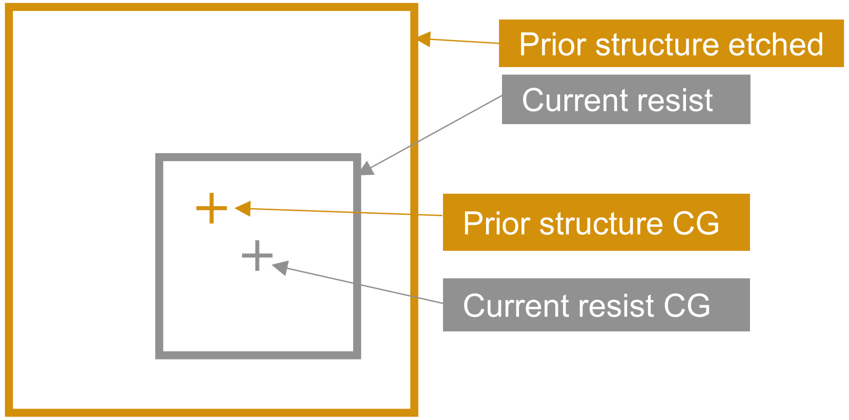


Registration is a measurement of the offset between the new resist pattern and a prior critical structure of interest.

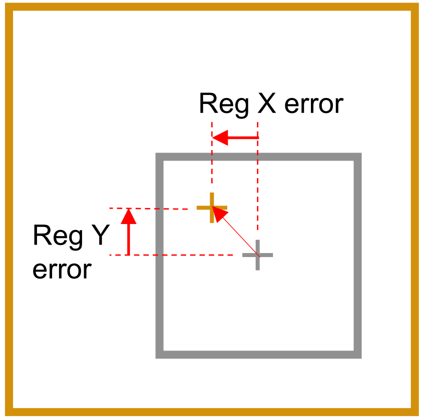
When the new resist pattern is perfectly stacked on top of the existing structure the offset is zero.

Registration Measurement:

Compare positions of center of gravity (CG) of the boxes



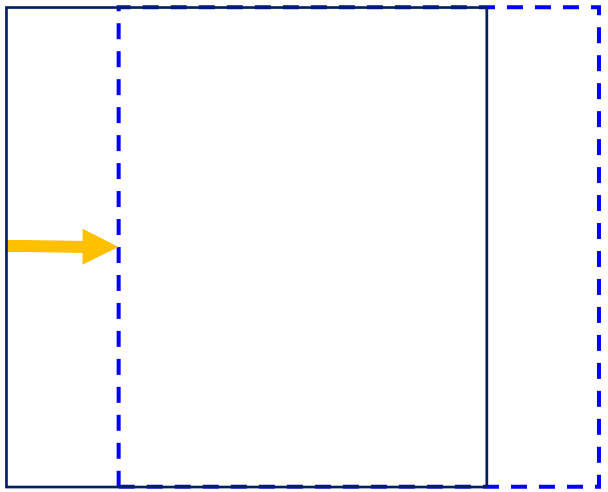
Measure CG displacement
Obtain a X and Y error for each point measured

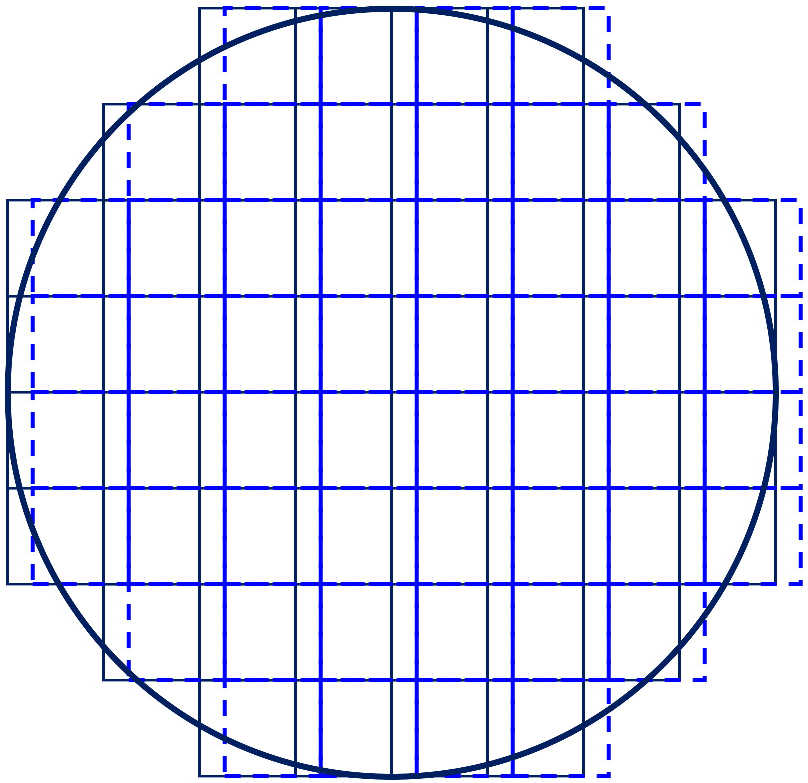


Registration Errors

- X-shift translation

Black: prior etched layer
Blue dashed: new resist pattern

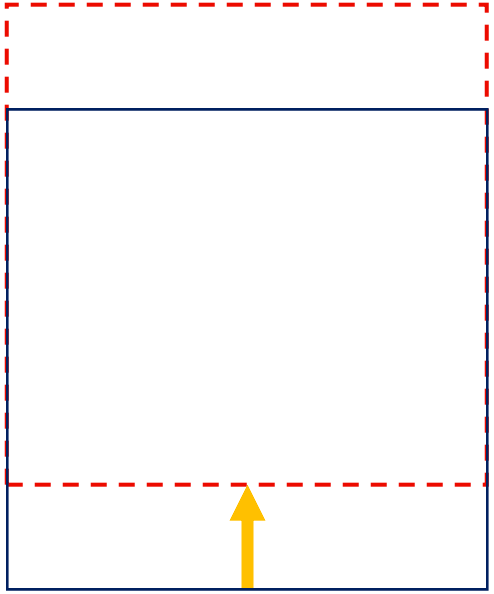


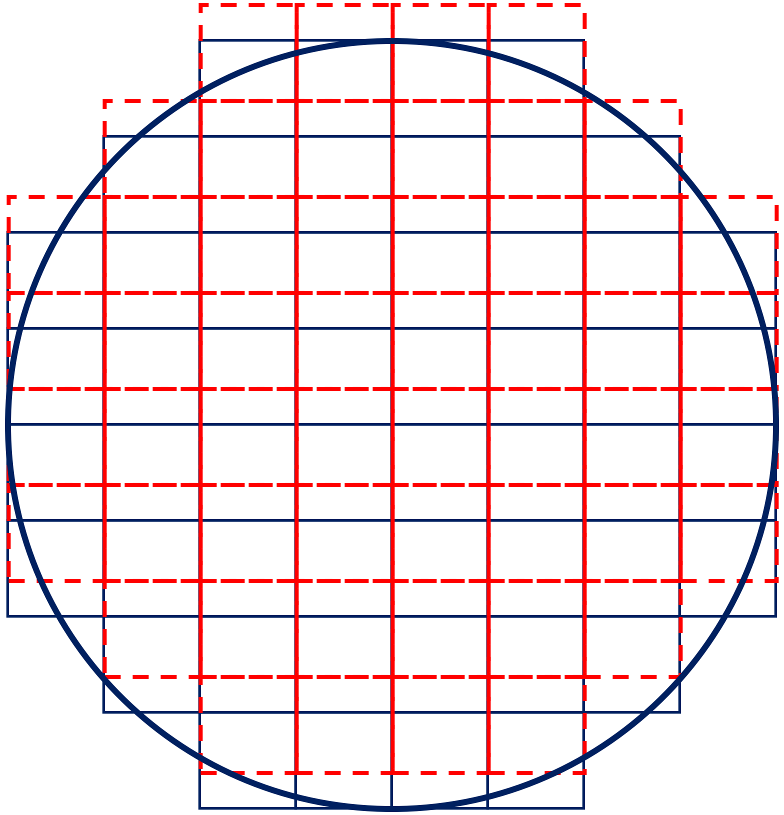


Registration Errors

- Y-shift translation

Black: prior etched layer
Red dashed: new resist pattern

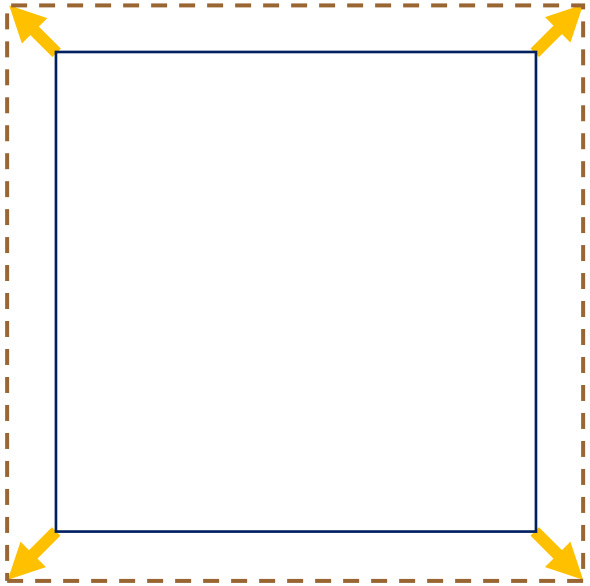


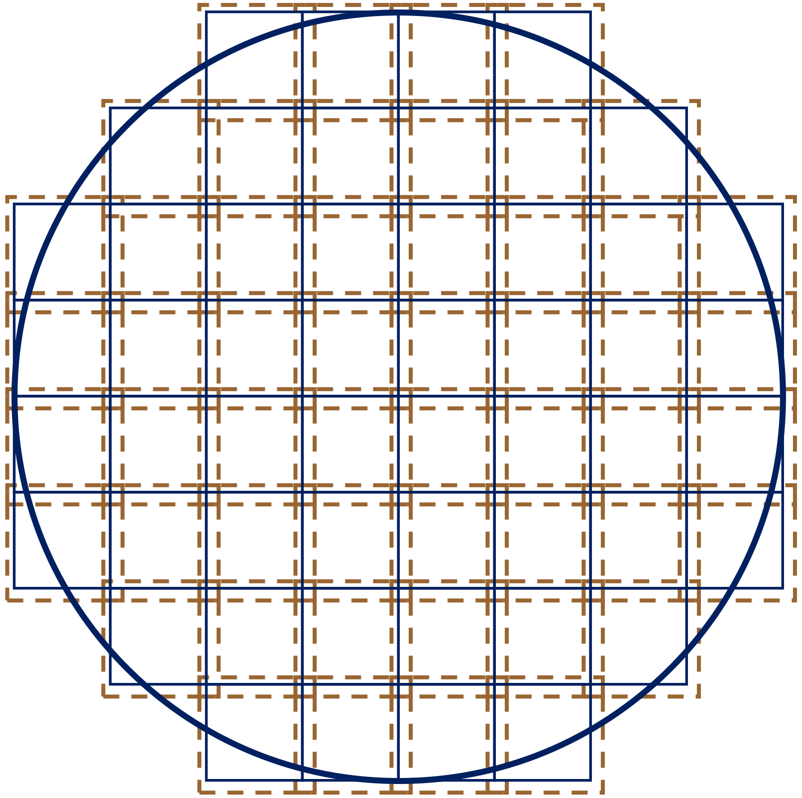


Registration Errors

- Field Magnification
  (Shot expansion)

Black: prior etched layer
Brown dashed: new resist pattern

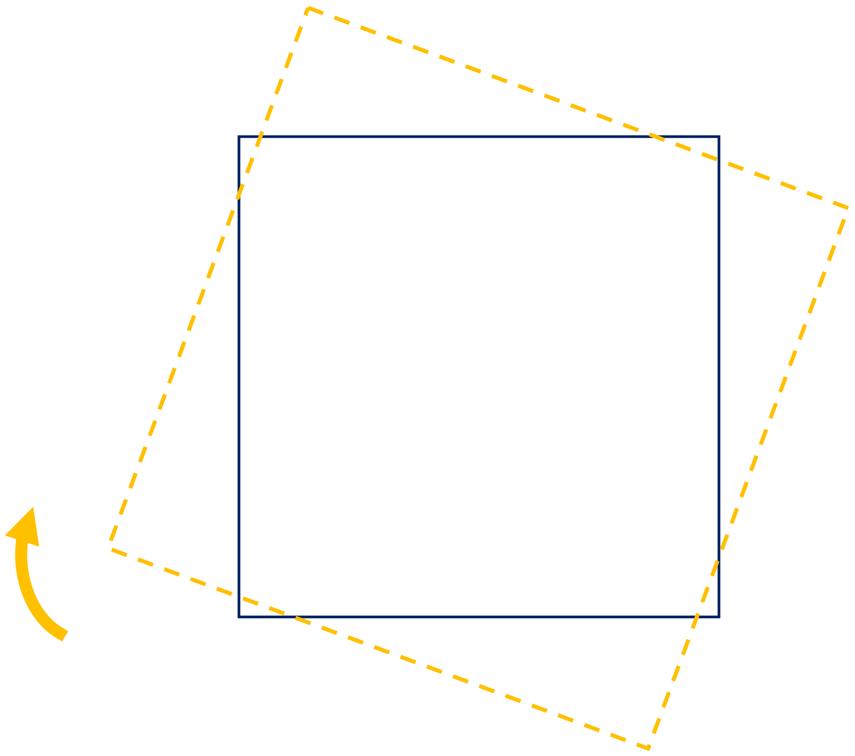


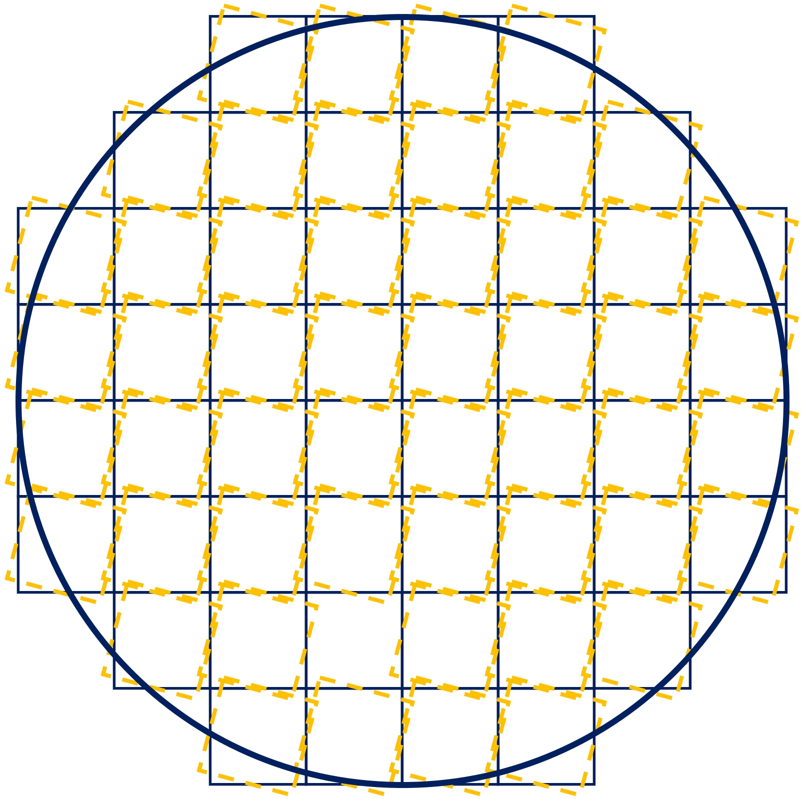


Registration Errors

- Field Rotation

Black: prior etched layer
Yellow dashed: new resist pattern

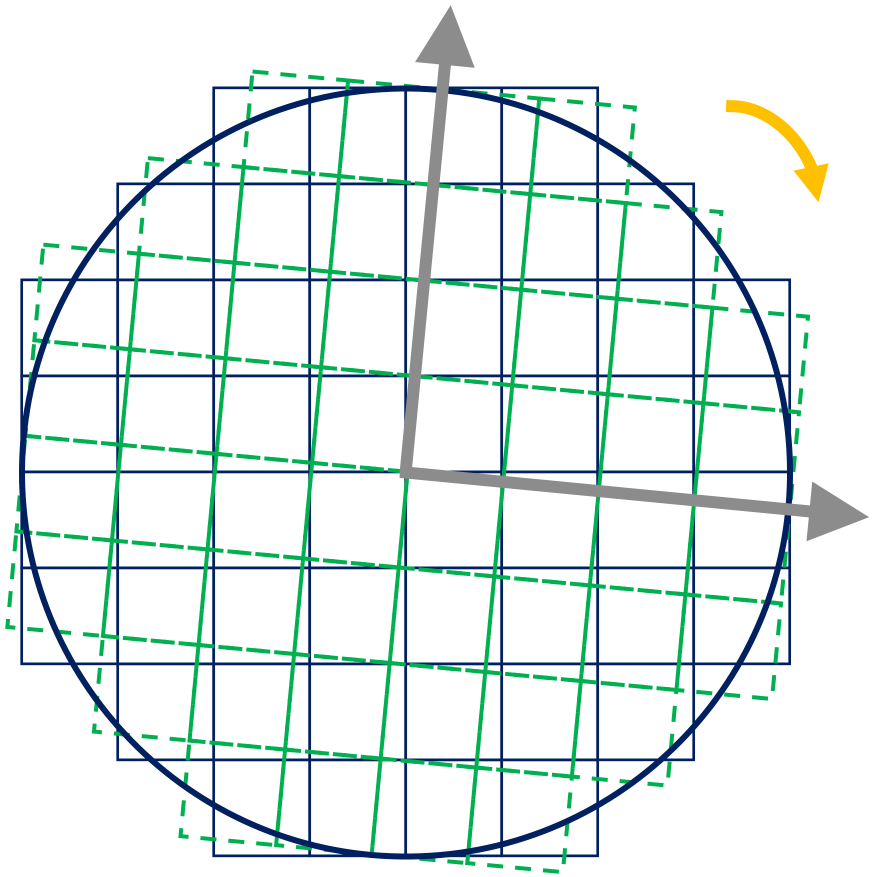




Registration Errors

- Wafer Rotation

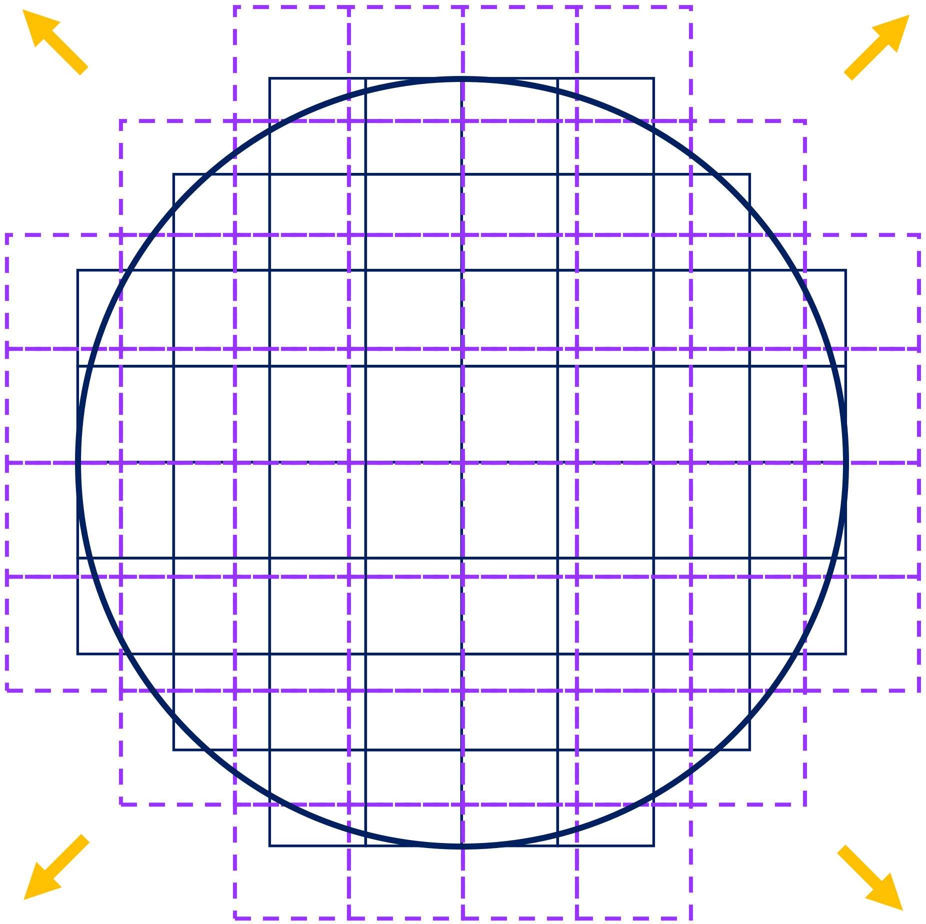
Black: prior etched layer
Green dashed: new resist pattern



Registration Errors

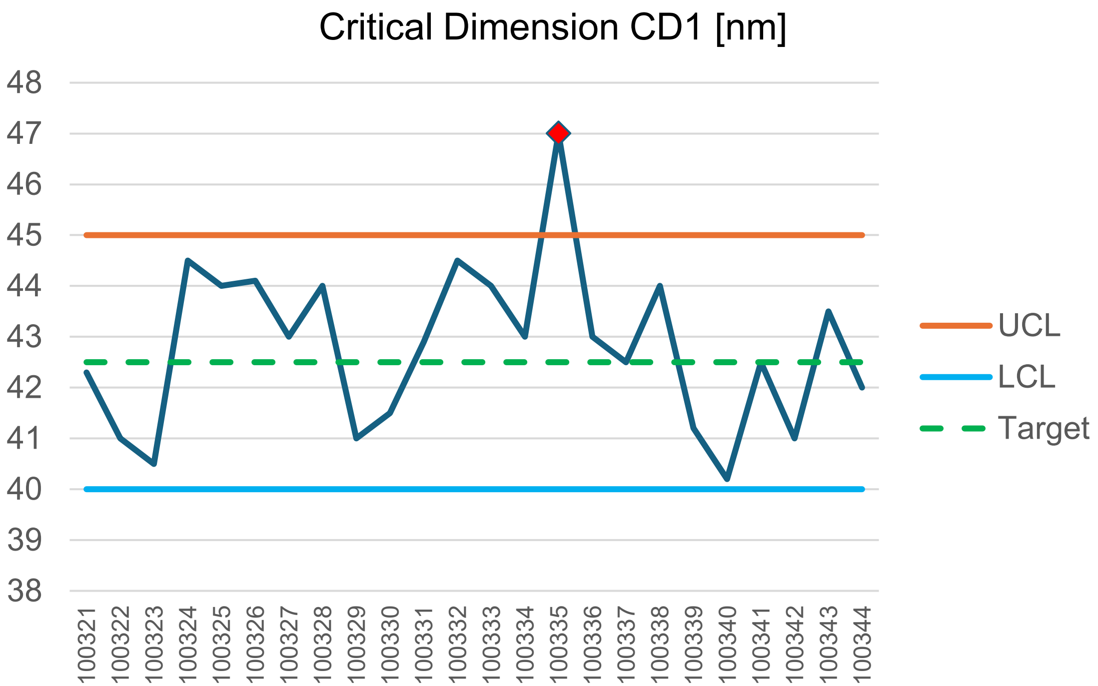
- Wafer Magnification

Black: prior etched layer
Purple dashed: new resist pattern



Statistical Process Control (SPC)

- Metrology measurements (e.g., resist thickness, CD measurements, etc.) are sent to an SPC chart
- SPC charts may be set up to collect raw data (individual measurements) or aggregate data (e.g., mean average chart, standard deviation chart, range chart)
- SPC uses statistical methods to monitor and control manufacturing processes with the goal to produce products within specifications and consistent quality
- SPC is used for proactive defect prevention. It detects trends and anomalies early and flags them to allow intervention before defects occur
- For a flagged OOC (out of control) condition need to react to a defined reaction mechanism
- Reviewing SPC charts is typically one of the first steps of a defect analysis investigation
- SPC is widely adopted across industries to improve product quality and operational efficiency.

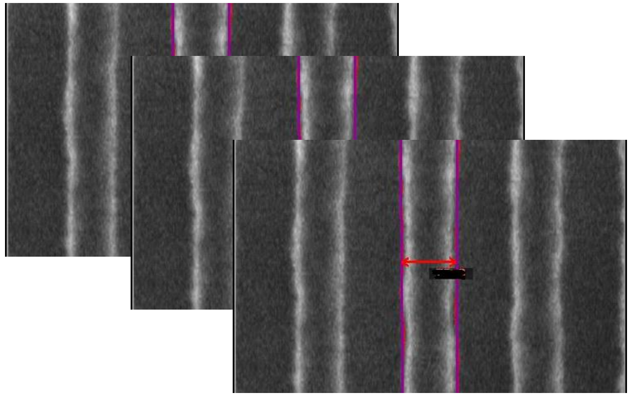


Photolithography Engineers set up SPC charts for their processes and create OOC reaction mechanisms, which may include getting notified when their processes are out of control.

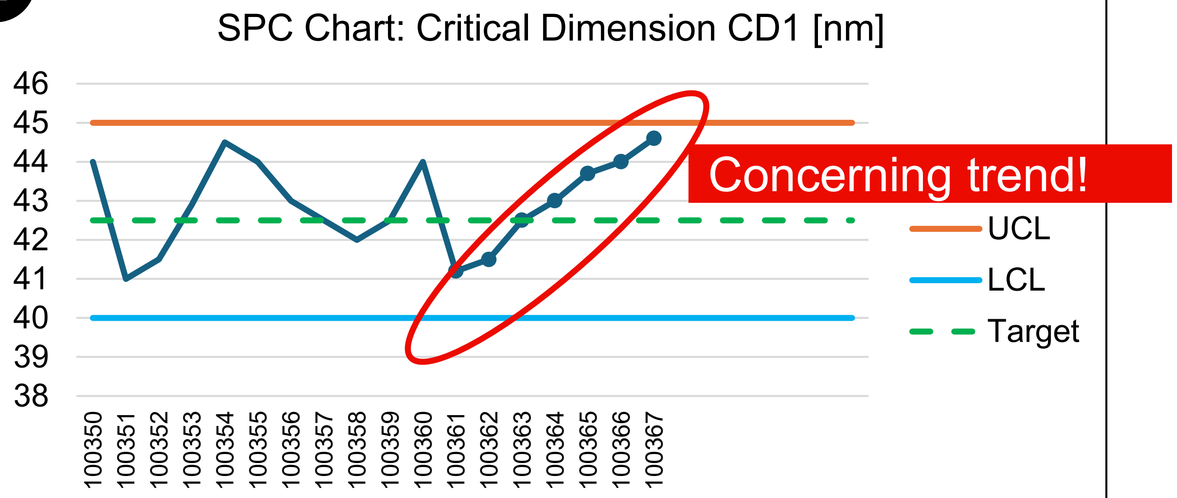
Photo process control loop example

1

CD SEM Measurements
CD1 – Line CD

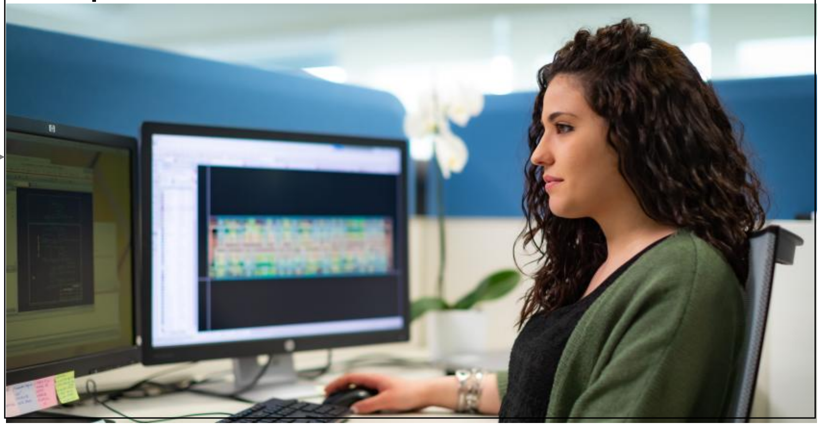


2

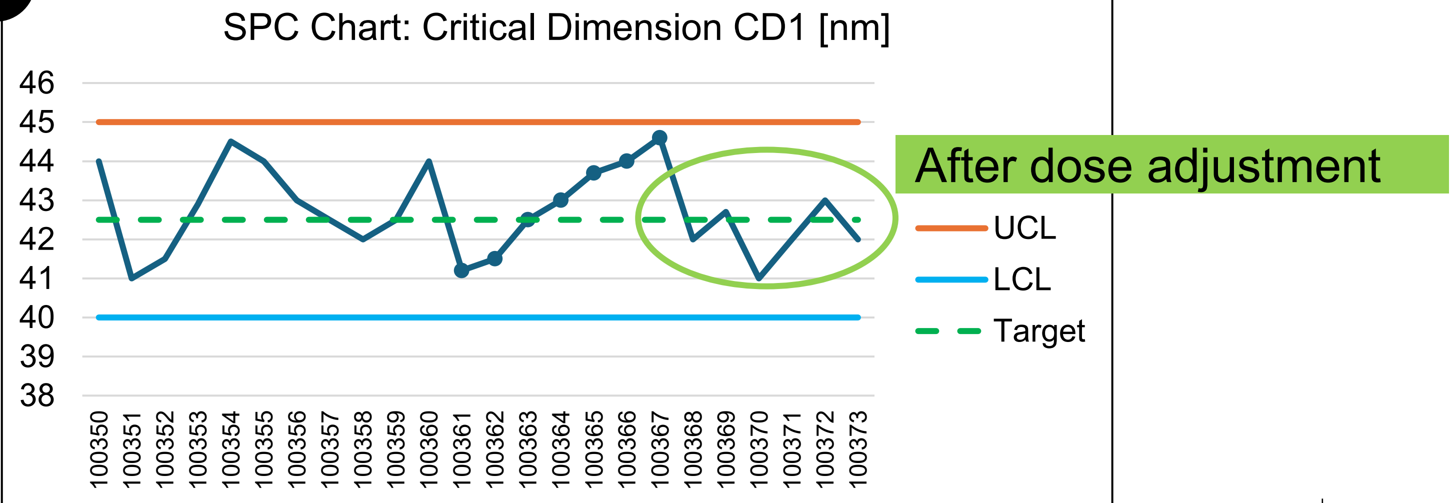


3

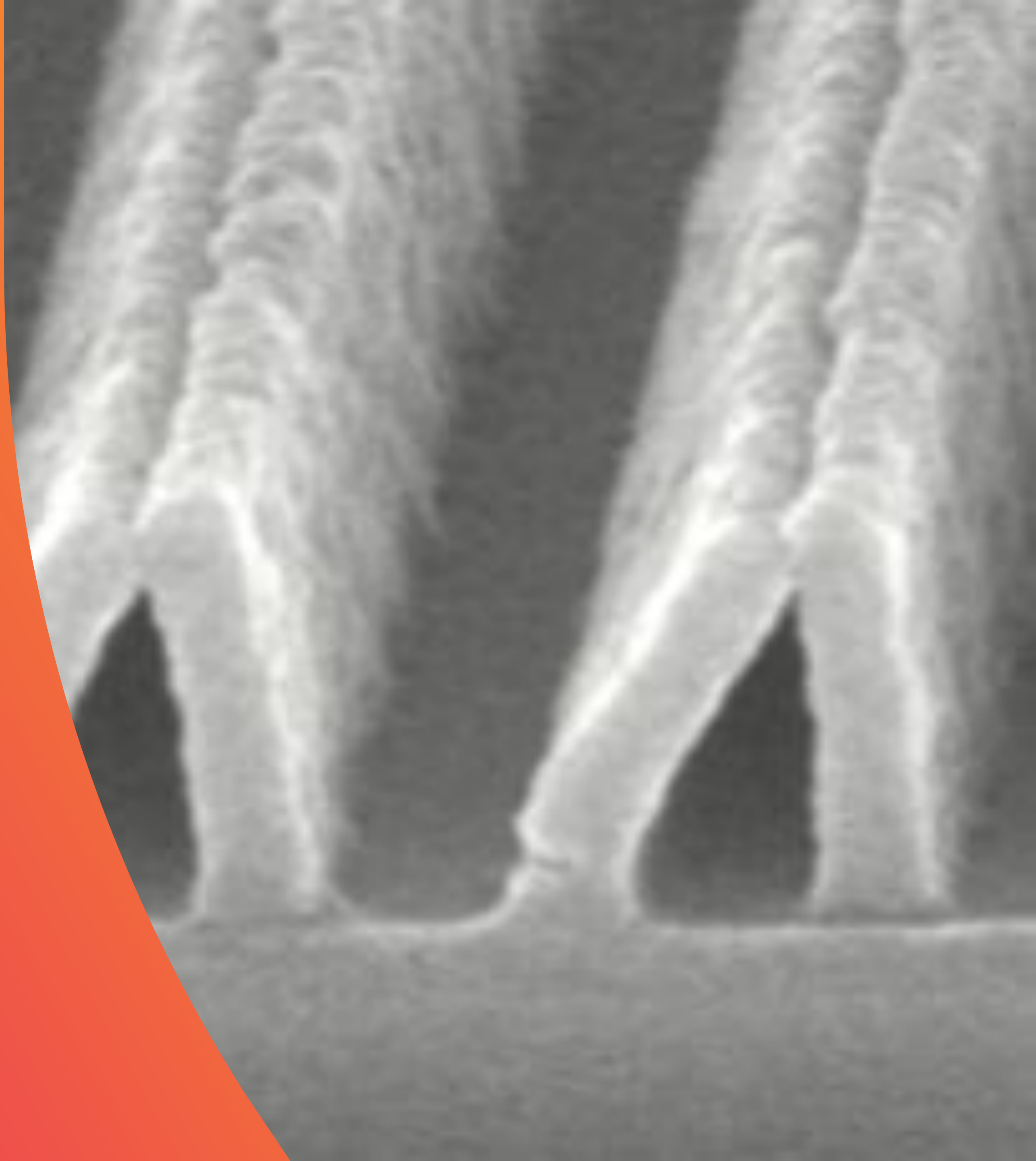
Photolithography Engineer analyzes and implements dose correction in scanner



4

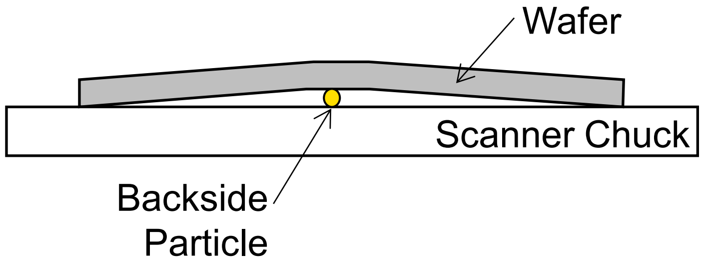


Examples of Common Defects in Photolithography

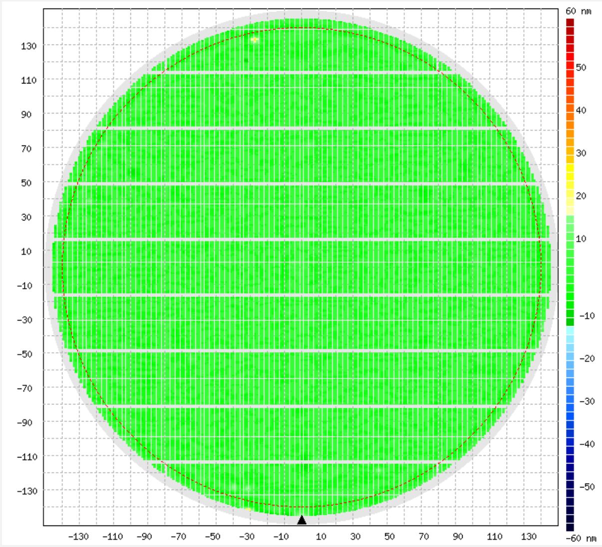


Focus Spot

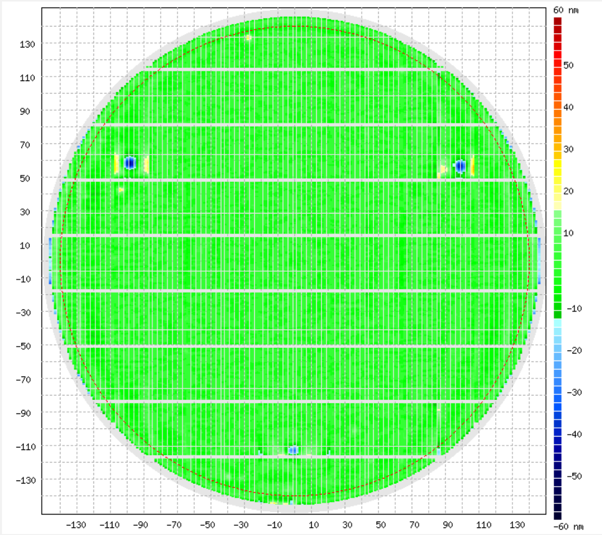
- Description
  - Very specific high spots on wafer
  - Parts of the wafer surface tilt/elevate slightly closer to the scanner lens, resulting in out-of-focus features during photo exposure in the elevated area.
- Possible Cause
  - This is typically a particles issue:
    - Tool Impurities
    - Wafer Backside Particle/contamination left on the wafer backside from a previous step or an incomplete wet clean
  - Particles could settle onto chucks on scanner
  - Particles as small as 0.1µ can cause focus spots!



Focus spot map examples



No focus spots of concern



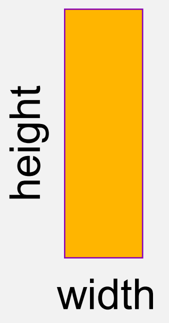
Focus spots of concern. Need to rework wafer and clean table to remove contamination.

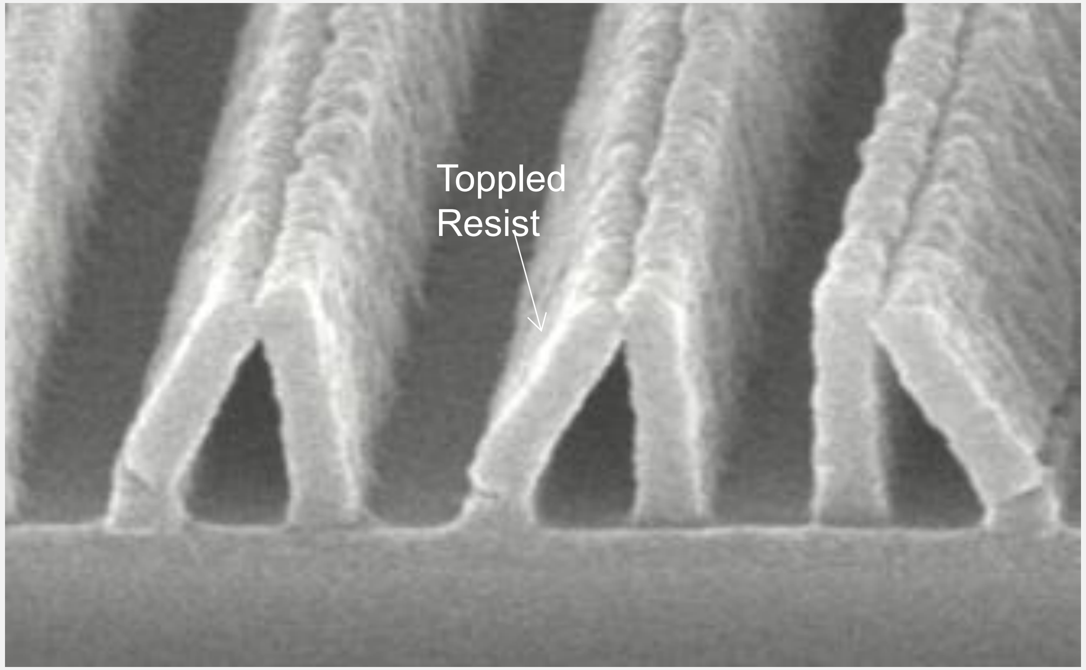
Resist Toppling

- Description
  - Resist lines that topple (collapse). This issue can cause a blocked etch in the subsequent dry etch process.

- Possible Cause
  - Capillary forces during the Develop process
    - Surfactants may be added in the Develop process to reduce surface tension
  - Poor resist adhesion to substrate
  - High resist aspect ratio (ratio of height to width) is susceptible to toppling
    - Rule of thumb: Resist aspect ratios of 3 or more are more prone to toppling so need to keep aspect ratios low

Aspect Ratio (AR) = height/width





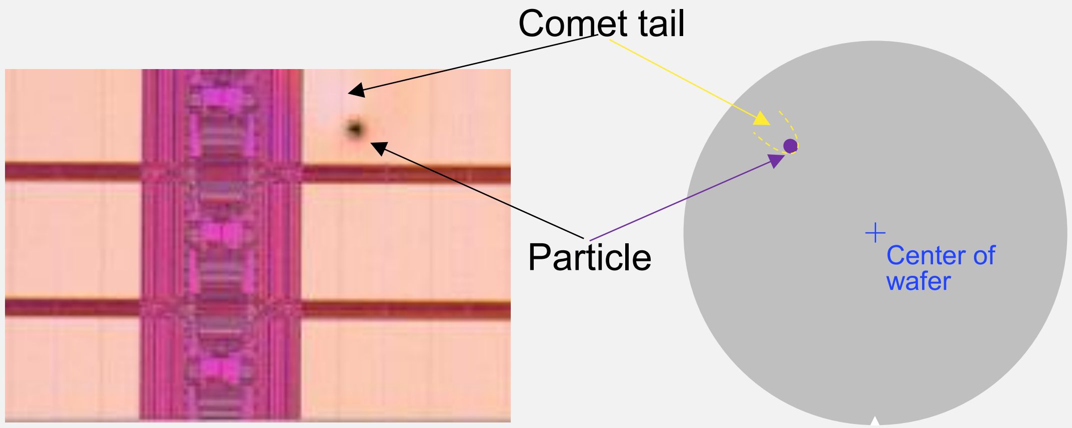
Toppled resist example

FM (Foreign Material)

- Description
  - Seen as a foreign material or particle with a trailing streak commonly referred to as a “comet tail”
  - This defect results in non-uniform resist thickness
  - The comet tail forms during the spin coat process due to centrifugal forces

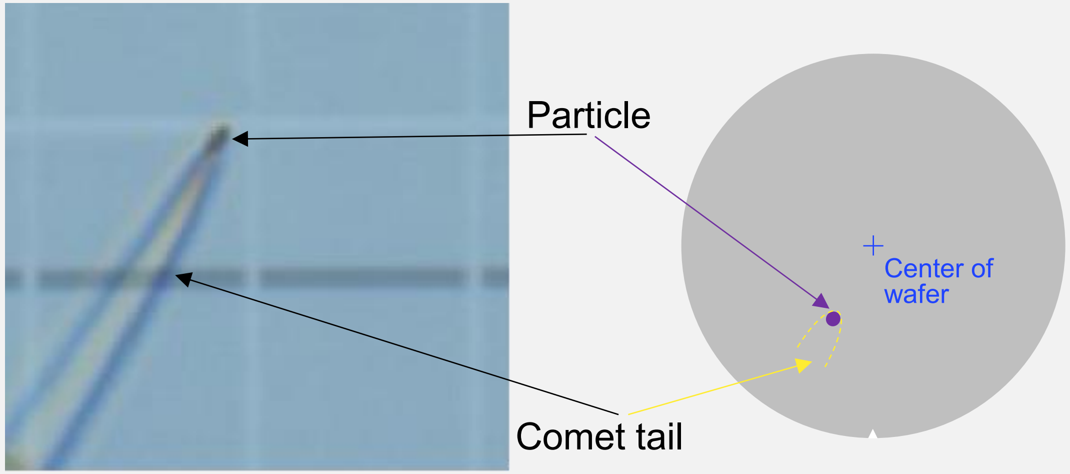
- Possible Cause
  - Contamination in the resist
  - Contamination on wafer
  - Contamination from the track

Foreign Material defect examples



Close-up of defect

Location of defect on wafer



Close-up of defect

Location of defect on wafer

Key Terminology Glossary

micron

Glossary

Term or acronym	Definition/description
CD	Critical Dimension. The measurement of a patterned feature like a line width, the space between lines, or a diameter.
CD SEM	Critical Dimension Scanning Electron Microscope. Tool that precisely measures critical dimensions.
Develop	The process in photo where, for positive resist, the exposed resist is removed and the unexposed resist is left on the wafer. Alternatively, for negative resist, the unexposed resist is removed and the exposed resist is left on the wafer.
DOF	Depth of Focus. The range of focus within which an acceptable image is formed.
Dose	The amount of light energy that is incident on the resist (usually expressed in millijoules per square centimeter).
DUV	Deep Ultraviolet. Range of UV wavelengths below the visible spectrum.
EUV	Extreme Ultraviolet. Very short wavelength (13.5 nm) advanced lithography technology.
Field	A pattern of one or more die that make up a reticle and are exposed at one time on the wafer in one shot.
hp	Half-Pitch. The average of the line and space for repeated features.
HMDS	Hexamethyldisilazane. A chemical used in the Vapor Prime step. HMDS enhances photoresist adhesion by displacing water vapor from the surface.
Immersion Photolithography	Advanced photo technology in which the space between the lens and the wafer is filled with liquid (typically DI water) instead of air. Immersion photolithography was introduced to achieve the effect of increasing the numerical aperture (NA) of the system without requiring a larger lens.
LCL	Lower Control Limit. Term used in Statistical Process Control (SPC).
NA	Numerical Aperture. This number characterizes the ability of a lens or optical system to collect light and focus an image. A higher NA value allows the optical system to capture light from wider angles which improves resolution.
Overlay	Overlay is the placement of one layer relative to another. This is critical in semiconductor manufacturing where precise stacking of structures is required to connect the different components effectively.
PEB	Post Exposure Bake. A bake that follows exposure. Step is necessary to complete the chemical reactions that are initiated during exposure.
Photoresist	A combination of solvents, photoactive chemicals and polymers. When exposed to light through a mask, photoresist undergoes a chemical change that makes selected regions either soluble or insoluble in a developer solution, enabling precise pattern transfer for semiconductor manufacturing.

Glossary

Term or acronym	Definition/description
Photosensitive	Chemicals that undergo chemical reactions in response to exposure to light.
n_f	Refractive Index. A quantity that indicates how much light slows down as it passes through a medium.
Registration	Measurement of the offset between the new resist pattern and a prior critical structure of interest.
Resist	See Photoresist
Reticle	Also called Mask or Photomask. Used in Photolithography to expose a temporary pattern on the photoresist
Scanner	The machine that exposes the resist-coated wafer to a pattern using UV or EUV light via a scanning motion across the field.
Soft Bake	A low temperature bake that follows application of resist to solidify the resist in preparation for exposure.
Stepper	The predecessor to scanners where the entire field is exposed at one time.
TMAH	Tetramethyl Ammonium Hydroxide. Chemical used for most develop processes in photo.
Track	The machine that dispenses chemicals on the wafer and heats/cools the wafer.
UCL	Upper Control Limit. Term used in Statistical Process Control (SPC).
UV	Ultraviolet. Invisible electromagnetic radiation with wavelengths shorter than 380-400 nm (violet).
Vapor Prime	The step that precedes resist application to help the resist adhere to the wafer, the chemical HMDS is used.
Wavelength	The distance between peaks (or valleys) of a wave. The light wavelengths used in semiconductor photolithography are measured in nm.

Resources

Outside References for Further Learning

1. Chris Mack, Lithoguru
   - Lithography Training - Chris Mack

2. ASML Technology Overview
   - ASML technology | Supplying the semiconductor industry

3. SPIE Advanced Lithography
   - SPIE Advanced Lithography + Patterning

4. NNCI is an NSF funded initiative across many universities with cleanroom facilities
   - National Nanotechnology Coordinated Infrastructure (NNCI)

Educator Hub

micron