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Introduction to Fabrication

Reviewed 2025

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Introduction to Fabrication - Goal and Objectives

In this introductory course participants will learn the basics of semiconductor fabrication at the wafer level.

Objectives:

1. Become familiar with general terms used in semiconductor manufacturing
2. Understand the purpose of the ten different fab areas that support manufacturing:
    1) Photolithography
    2) Dry Etch
    3) Wet Process
    4) Chemical Mechanical Planarization
    5) Chemical Vapor Deposition
    6) Physical Vapor Deposition
    7) Diffusion
    8) Implant
    9) Metrology
    10) Real-time Defect Analysis
3. Understand the step-by-step fabrication process for basic CMOS technology

Target Audience

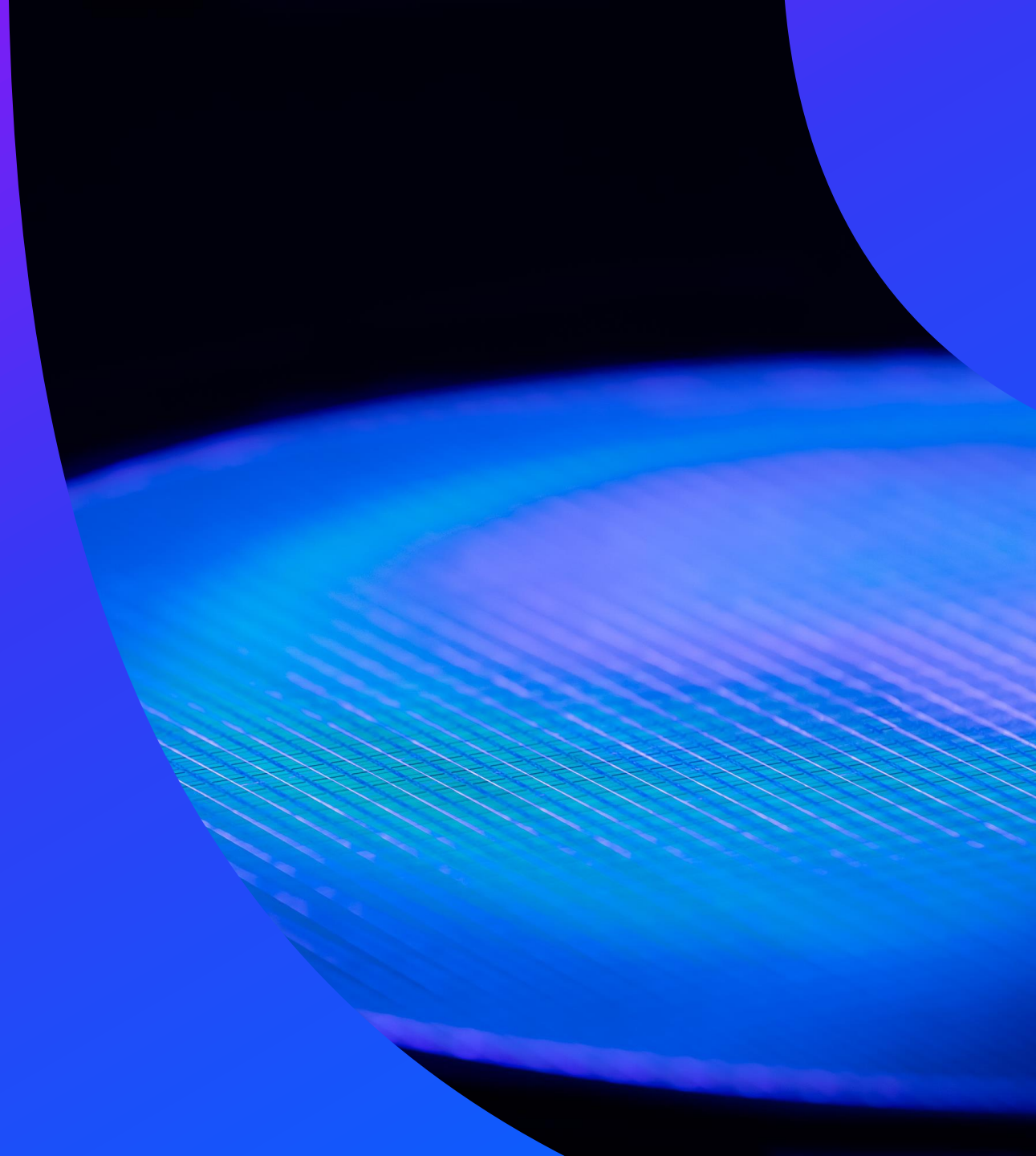
- This Introduction to Fabrication module covers the basics of semiconductor fabrication at the wafer level.
- Interns, NCGs (New College Grads), and new employees in technical roles need to understand these concepts
- Examples of critical target audience roles at Micron that utilize these concepts:
  - Process Technicians
  - Equipment Technicians
  - Process Engineer
  - Equipment Engineer
  - Process Integration Engineer
  - Product Engineer
  - Characterization Engineer
  - Yield Enhancement Engineer
  - Test Engineer
  - Probe Engineer
  - Reliability Engineer
  - Quality Engineer
  - Design Engineer
  - Verification Engineer

Pro tip

Everyone interviewing at Micron can use this presentation to prepare for the interview by learning foundational information about memory. Check out the candidate guides for Engineering, Technician and Business roles.

- Micron engineering candidate guide
- Micron technician candidate guide
- Micron business candidate guide

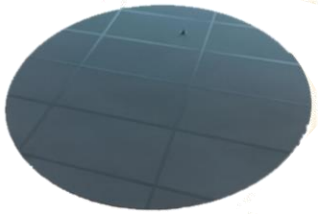
Introduction to Fabrication



Fabrication

Fabrication is the process of building circuits on a silicon wafer in a **cleanroom** environment where all aspects of production (temperature, power, chemistries, moisture, contamination, etc.) are tightly controlled.

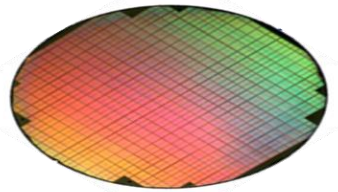
Silicon wafers are purchased from Vendors



Bare silicon 300mm wafer

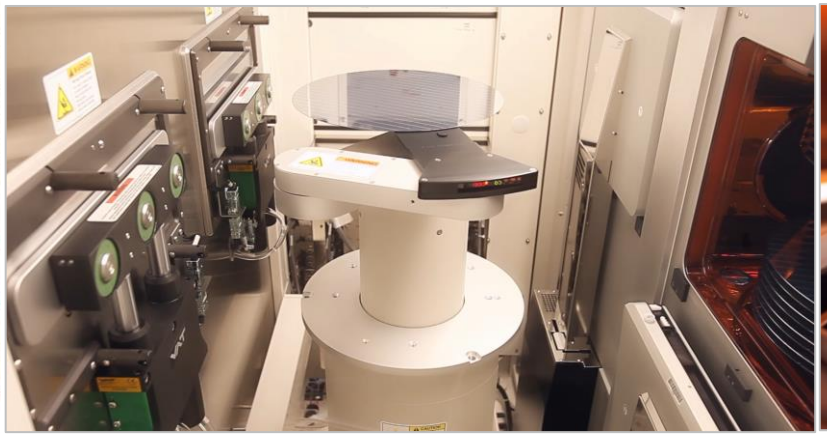
Fabrication (a.k.a. Manufacturing)

How long does it take to complete fabrication? (45-140 days)

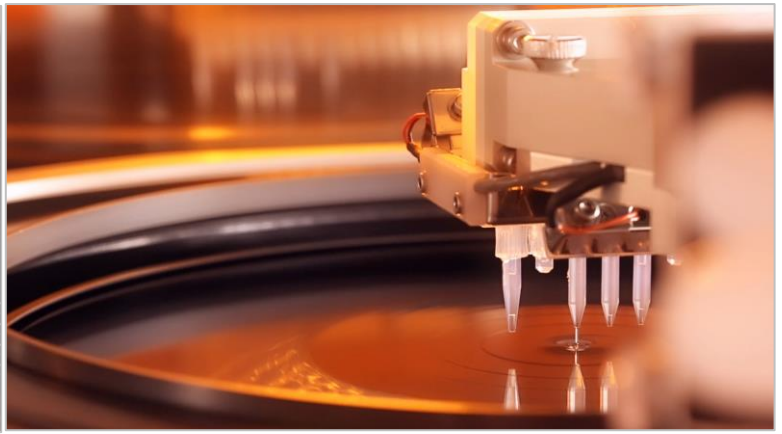


Completed wafer ready for Probe and Final Parametric testing

Picture inside a cleanroom fab



Picture inside a tool: robot that handles wafers



Picture inside a tool: dispensing photoresist in a photolithography tool

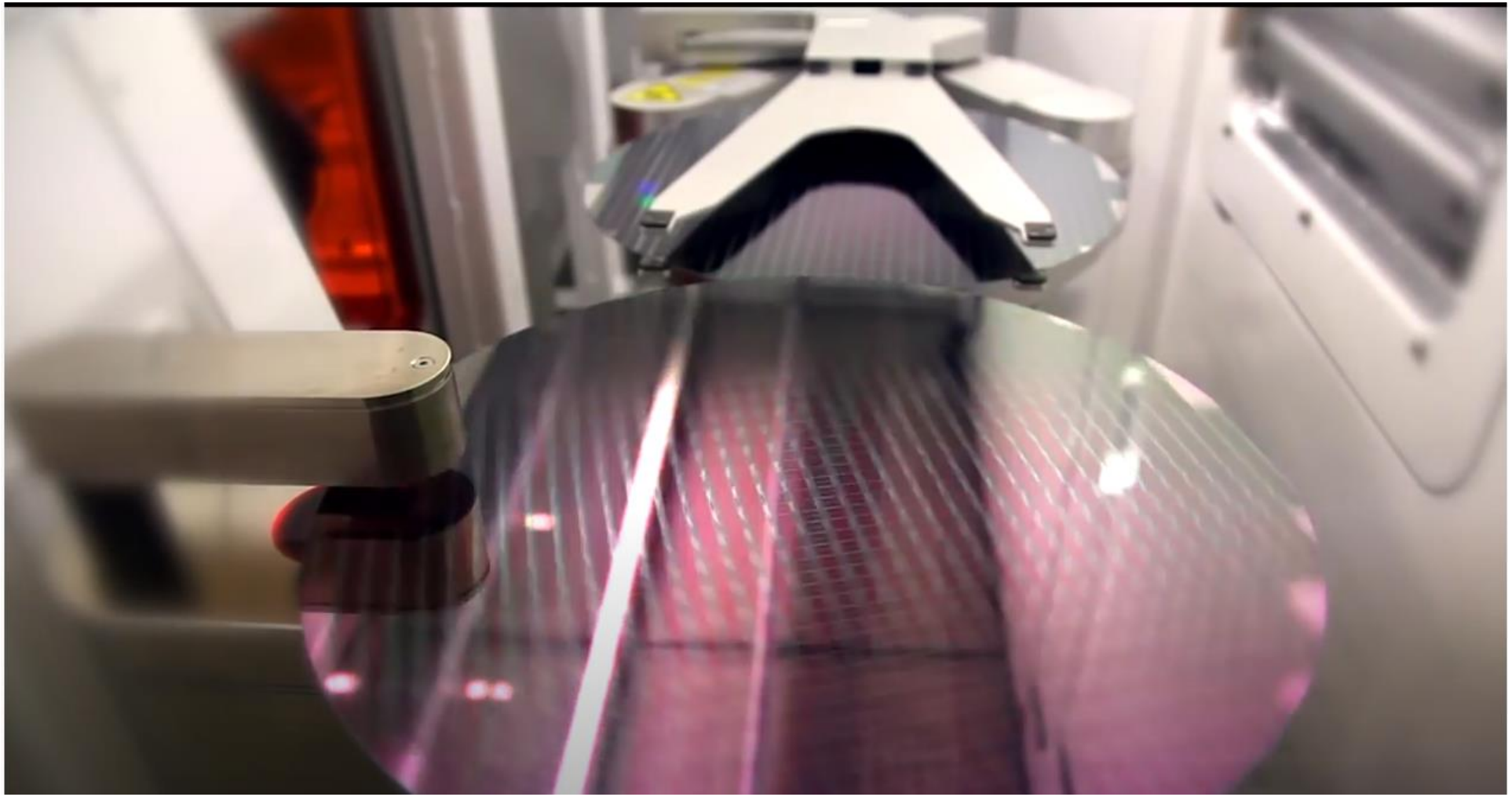
Semiconductor manufacturing is done in cleanrooms

View of a fab cleanroom from the ceiling, on the path of the AMHS (Automated Material Handling System)

There are hundreds of tools/equipment in a semiconductor fab

View of a tool in a fab cleanroom

Automation inside a tool



Picture inside an equipment tool: robot that handles wafers

Cleanrooms & Classification Standards

Q: What Is a Cleanroom?

A: It is a room that has HEPA (High Efficiency Particulate Air) filtration to remove particles from the air. Cleanrooms are used for manufacturing where high levels of cleanliness and sterility are required. Common applications of the cleanroom include manufacturing of medical devices, pharmaceuticals, and semiconductors.

ISO 14644-1 Cleanroom Standards							
ISO Class	Maximum Particles per m^3						FED Standard*
	≥0.1µ	≥0.2µ	≥0.3µ	≥0.5µ	≥1µ	≥5µ	
ISO 4	10,000	2,370	1,020	352	83		Class 10
ISO 5	100,000	23,700	10,200	3,520	832	29	Class 100

*US Fed standard in particles per ft^3 superseded in 2021 by ISO standard using particles per m^3.

Q: Why do we wear smocks in the fab?

A: To protect wafers from human and other contamination

Semiconductor Memory Manufacturing Flow

This document focuses on this part

Start Material: Silicon is purified and formed into wafers (outside Micron).

Wafer-Level Fabrication: Electronic devices (transistors, resistors, capacitors, etc.) are fabricated on the silicon wafers, and are then interconnected together into complete circuits.

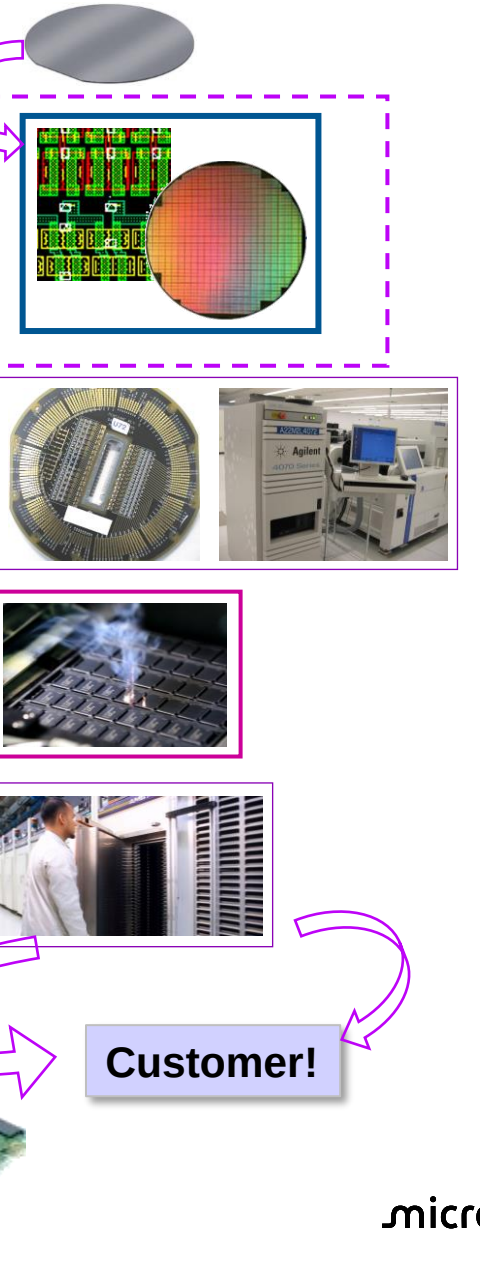
Probe: Each die is tested for functionality, failing die are flagged. Failure data (bins) is collected for yield improvement.
Param: Wafer-level electrical data is collected to characterize and improve the process.

Packaging: Die that pass Probe are separated from the wafer and assembled into packages.

Final Test and Burn-In: Packaged parts are tested for functionality. Some parts are given additional tests under harsh conditions to verify reliability.

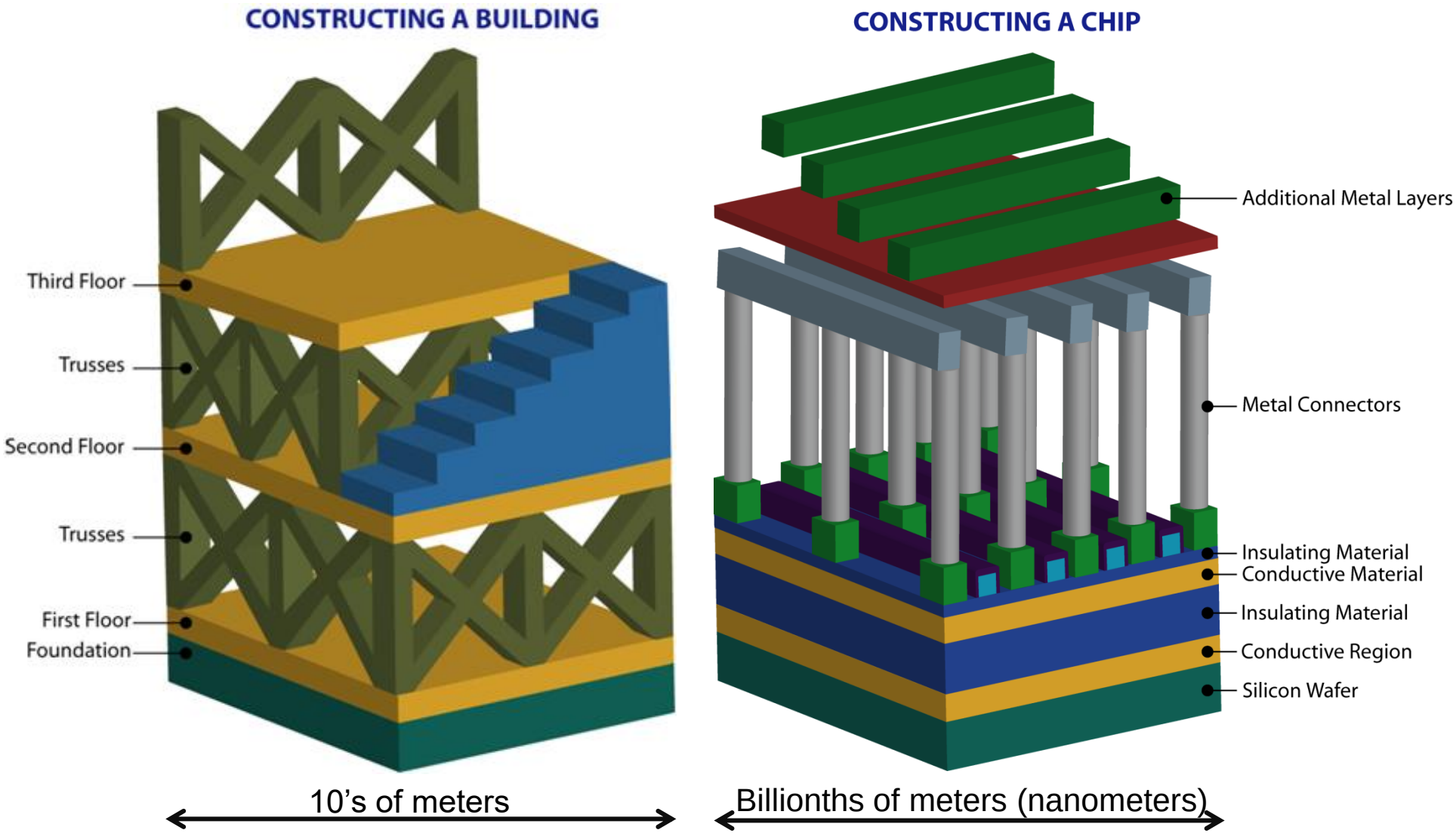
Module Assembly and Testing: Some DRAM packaged parts are placed into modules and further tested for functionality and reliability.

System/SSD Testing: NAND packaged parts may be placed into SSDs or Composite drives and further tested for performance.



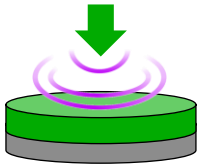
Construction Analogy

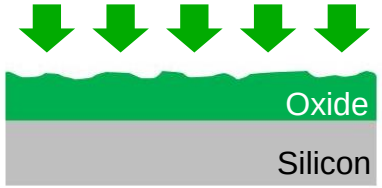
- The wafer fabrication process is similar to the construction of a building, except on a MUCH smaller scale.
- We start out with plans or designs and then build the foundation followed by many interconnecting layers (or floors).



Wafer Processing Areas – Five Basic Actions

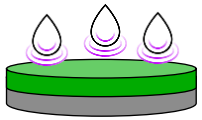
Add Material





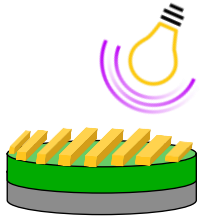
- Diffusion
- CVD (chemical vapor deposition)
- PVD (physical vapor deposition)
- Wet Process (electroplating)

Remove/Etch Material



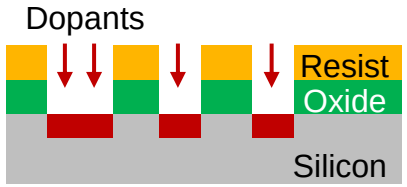
- Dry Etch
- Wet Process
- CMP (chemical mechanical planarization)

Create Patterns



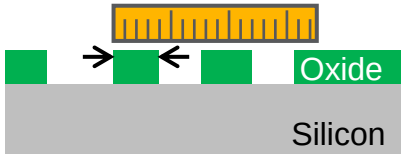
- Photolithography

Change Electrical Properties



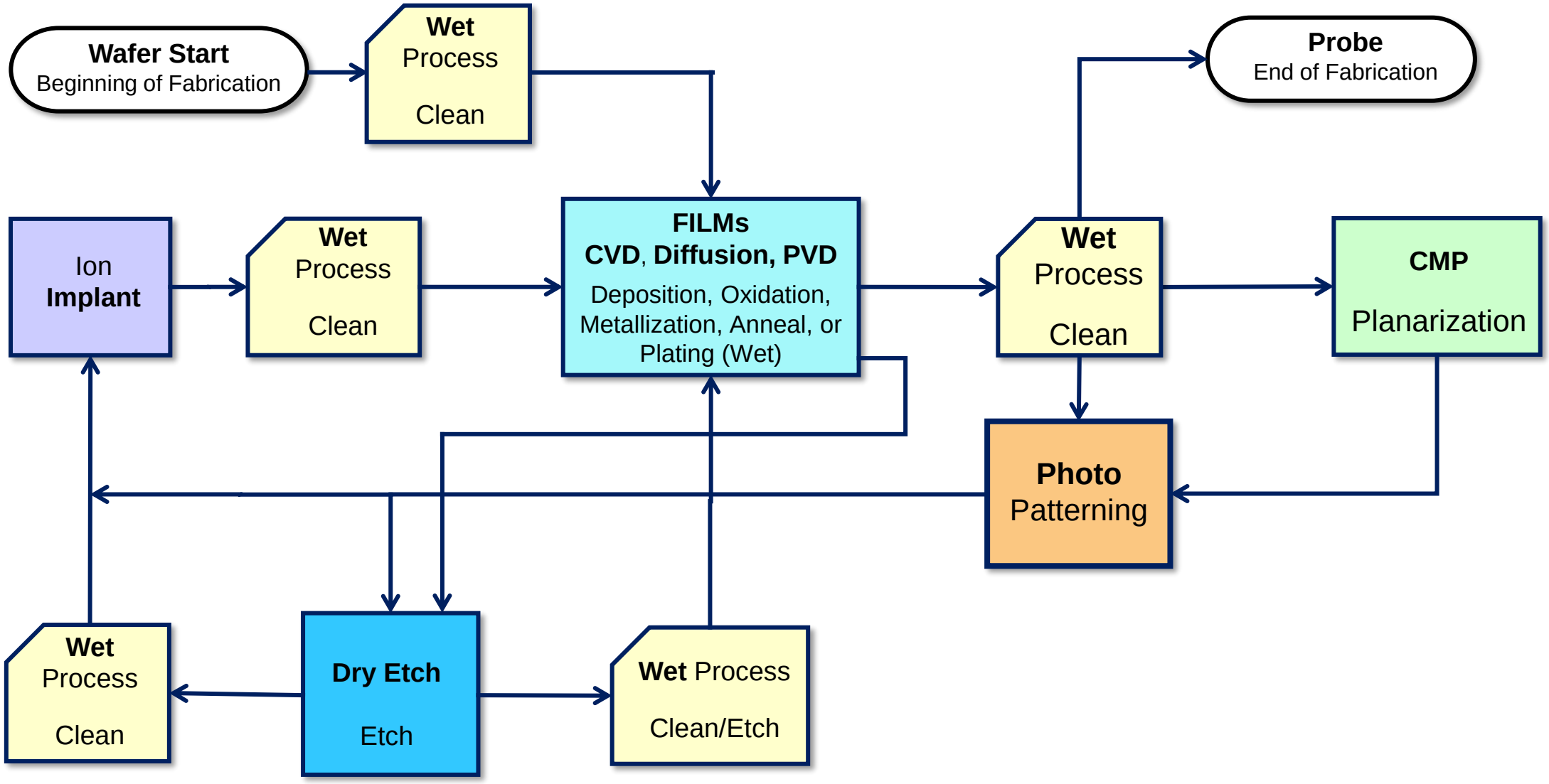
- Implant

Measure/Inspect

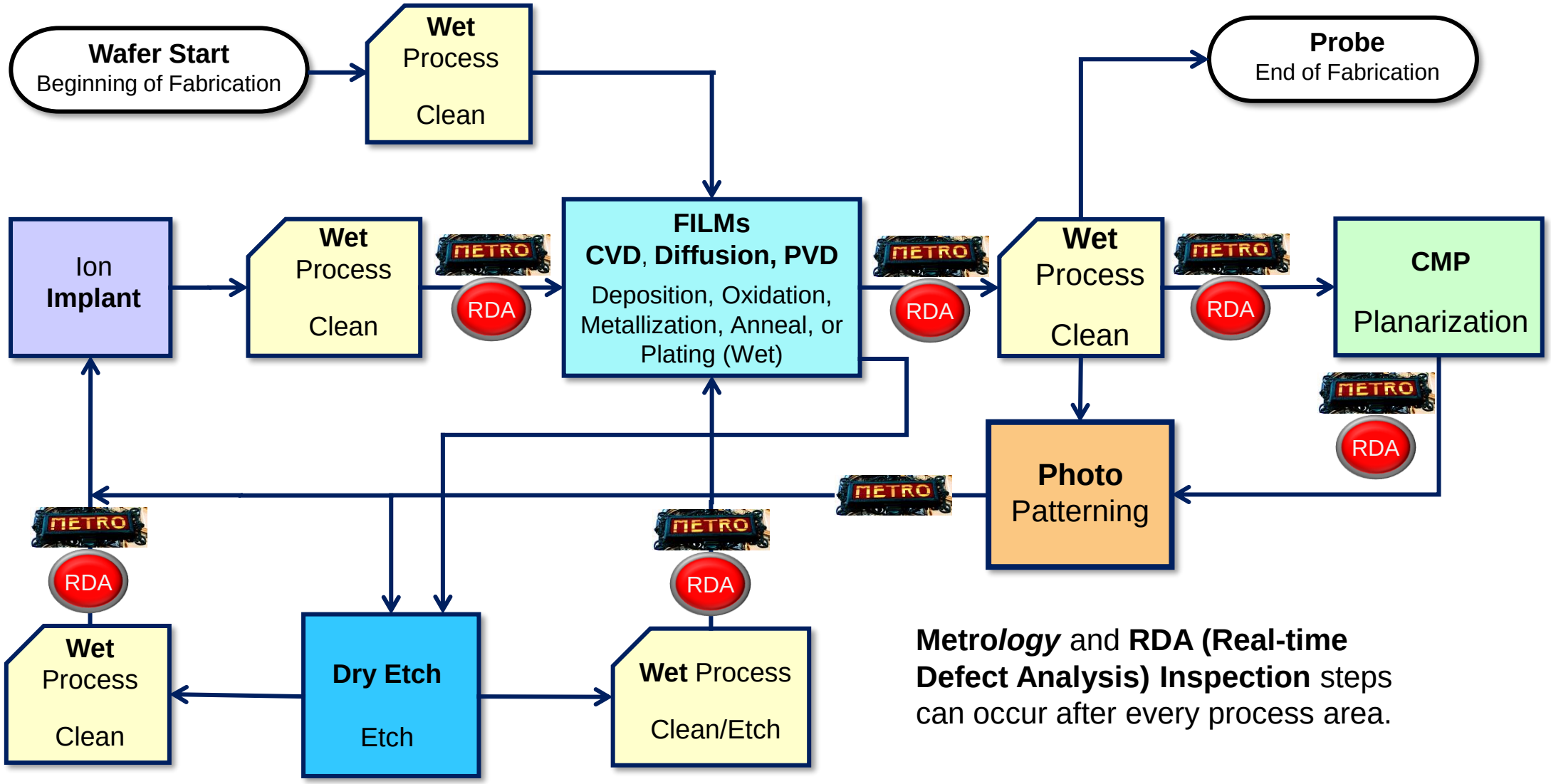


- Metrology
- RDA (real-time defect analysis)

Simplified Wafer Processing Flow



Simplified Wafer Processing Flow



Metro*logy* and **RDA (Real-time Defect Analysis) Inspection** steps can occur after every process area.

Wafer Process Traveler and Recipes

A **Traveler** is the sequential list of every step needed to make a memory chip. Years ago, it was printed on cleanroom paper and “traveled” along with the box of wafers. Nowadays tracking is all performed online.

A Traveler may have more than a thousand steps!

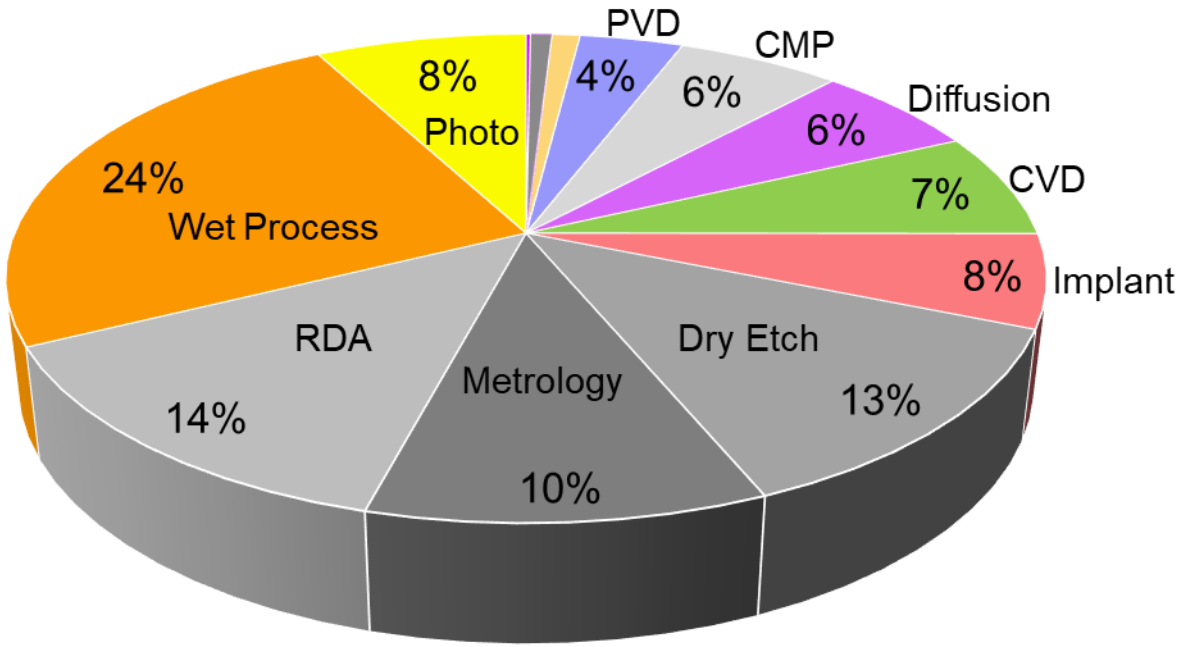
Each Traveler step belongs to one of the 10 Fab areas.

Each Traveler step has a **Recipe** associated with it. The Recipe contains detailed instructions to process the wafer (for example: temperature, pressure, chemicals or gases used, dilution of chemicals, amount of time, etc.)

Step #	Traveler Step	Fab Area
161	TG - GATE HARDMASK DEPOSITION	CVD
162	TG - GATE PHOTO PATTERN	PHOTO
163	TG - GATE PHOTO ALIGNMENT	METROLOGY
164	TG - GATE CRITICAL DIMENSION	METROLOGY
165	TG - GATE DRY ETCH	DRY ETCH
166	TG - GATE DRY STRIP	WET PROCESS
167	TG - GATE WET CLEAN	WET PROCESS
168	TG - GATE CRITICAL DIMENSION	METROLOGY
169	TG - GATE STRESS	METROLOGY
170	TG - GATE PROFILE	METROLOGY
171	TG - GATE INSPECTION	RDA
172	TG - GATE SPACER WET CLEAN	WET PROCESS
173	TG - GATE SPACER OXIDE DEPOSITION	CVD
174	TG - GATE SPACER OXIDE DRY ETCH	DRY ETCH
175	TG - GATE SPACER OXIDE WET CLEAN	WET PROCESS
176	TG - GATE SPACER CRITICAL DIMENSION	METROLOGY

Breakout of Steps by Functional Area

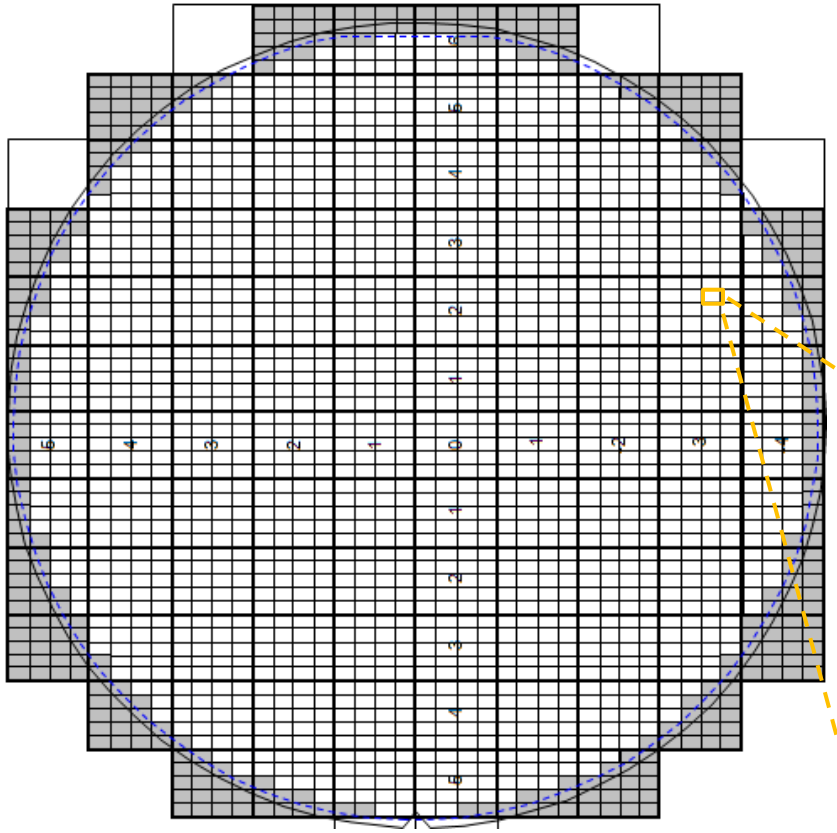
- There are 10 primary “functional areas” of the fab:
  - **CMP**: Chemical Mechanical Planarization
  - **CVD**: Chemical Vapor Deposition
  - **Diffusion**
  - **Dry Etch**
  - **Implant**
  - **Metrology**
  - **Photolithography** (a.k.a. Photo)
  - **PVD**: Physical Vapor Deposition
  - **RDA**: Real time Defect Analysis
  - **Wet Process**



- The pie chart on the right shows a typical distribution of the number of traveler steps by each functional area.

Why do you think Wet Process is the area with the highest percentage of steps?
Hint: look at the slide titled Simplified Wafer Processing Flow

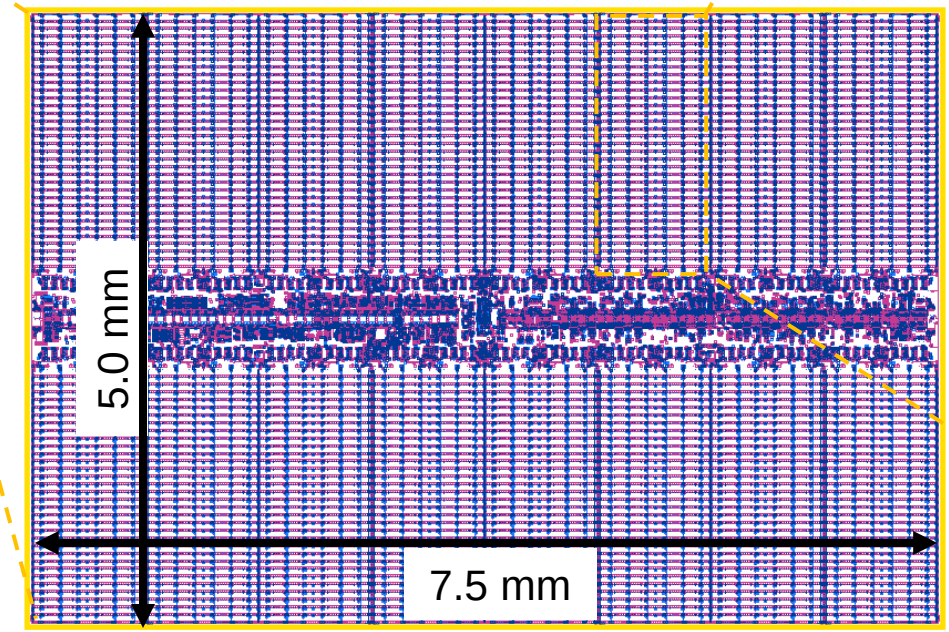
Zoom In to 3D Model



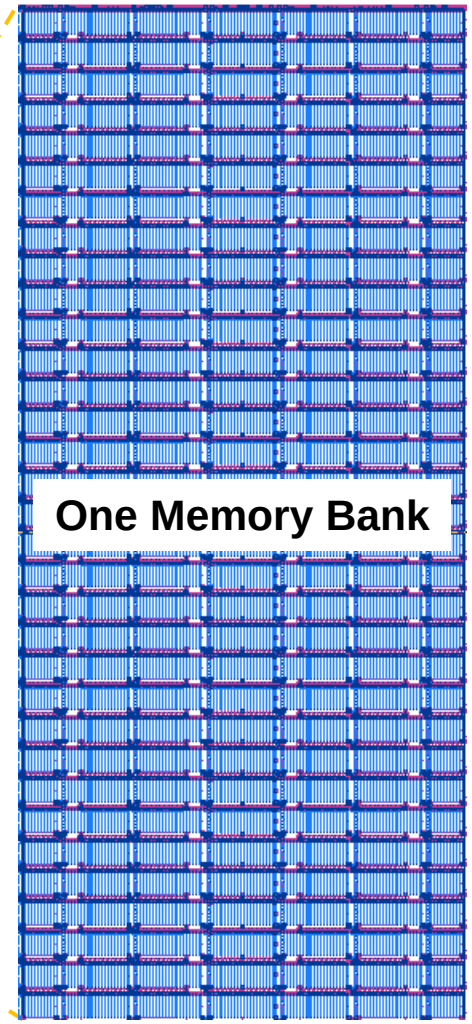
Wafer Map

Over 1000 die per wafer

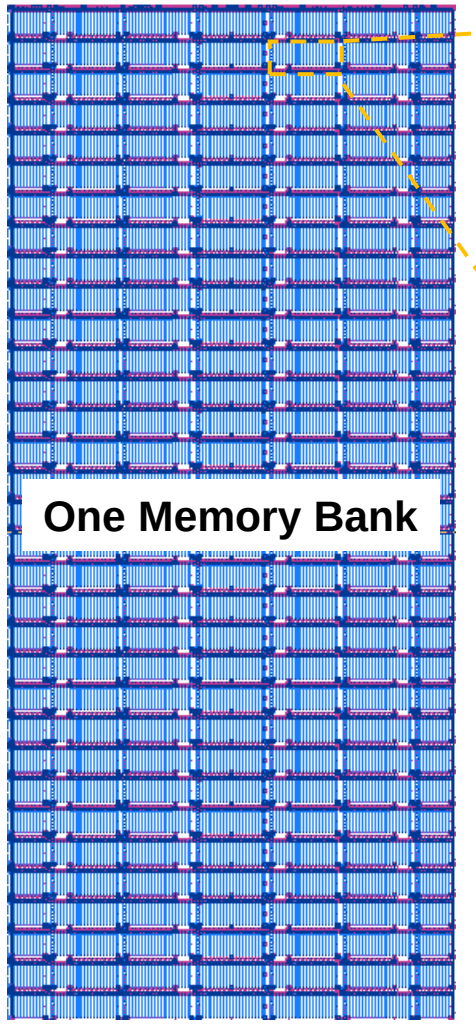
- 3D models are used in this presentation to explain the fabrication process step by step
- These two slides will help to orient the location and scale of the 3D models that are used to describe the traveler flow.

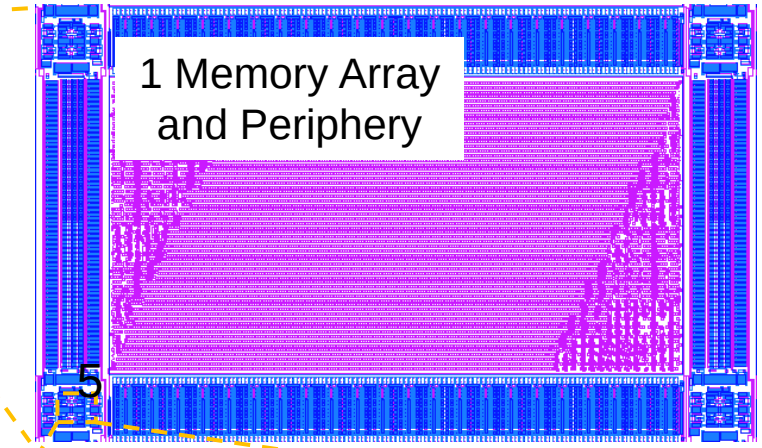


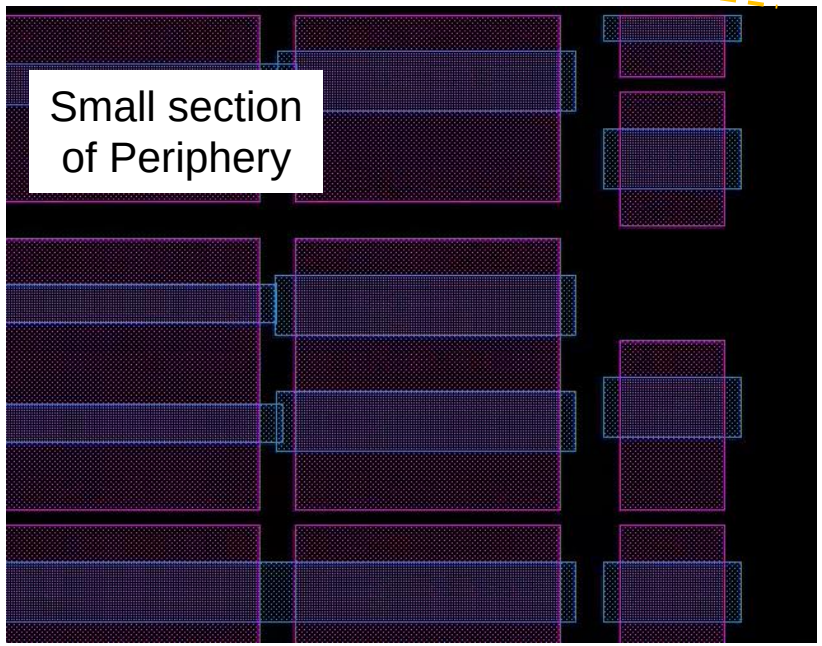
One DRAM Die



Zoom In to 3D Model (continued)







3D Model of a Small
Section of CMOS Periphery

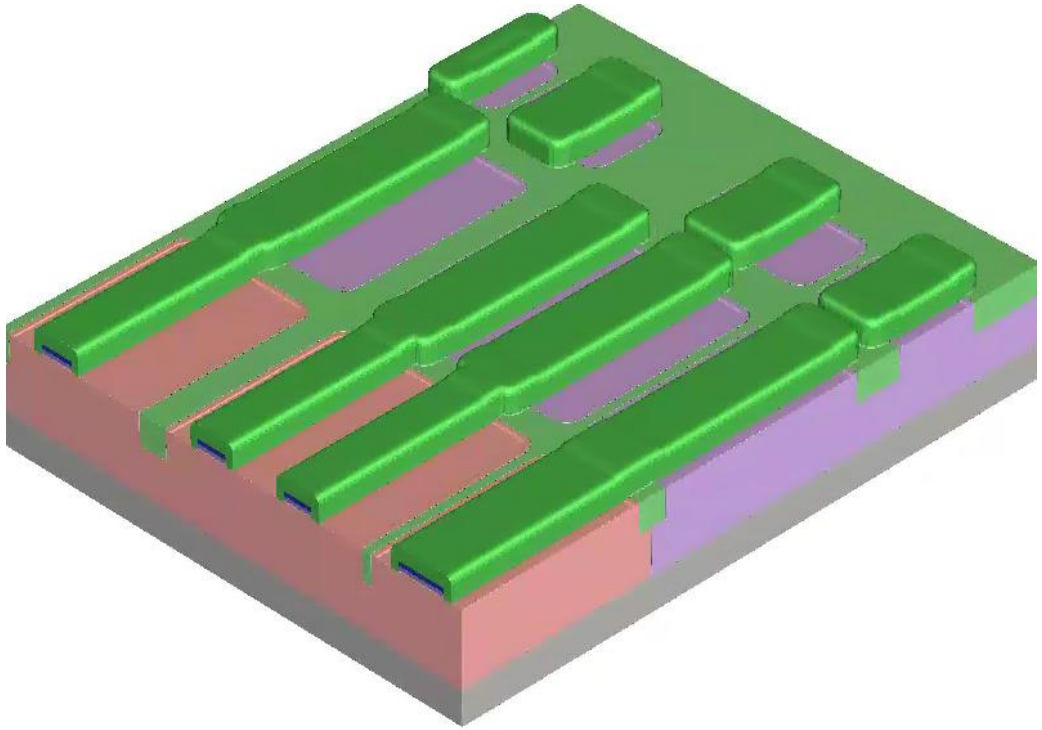


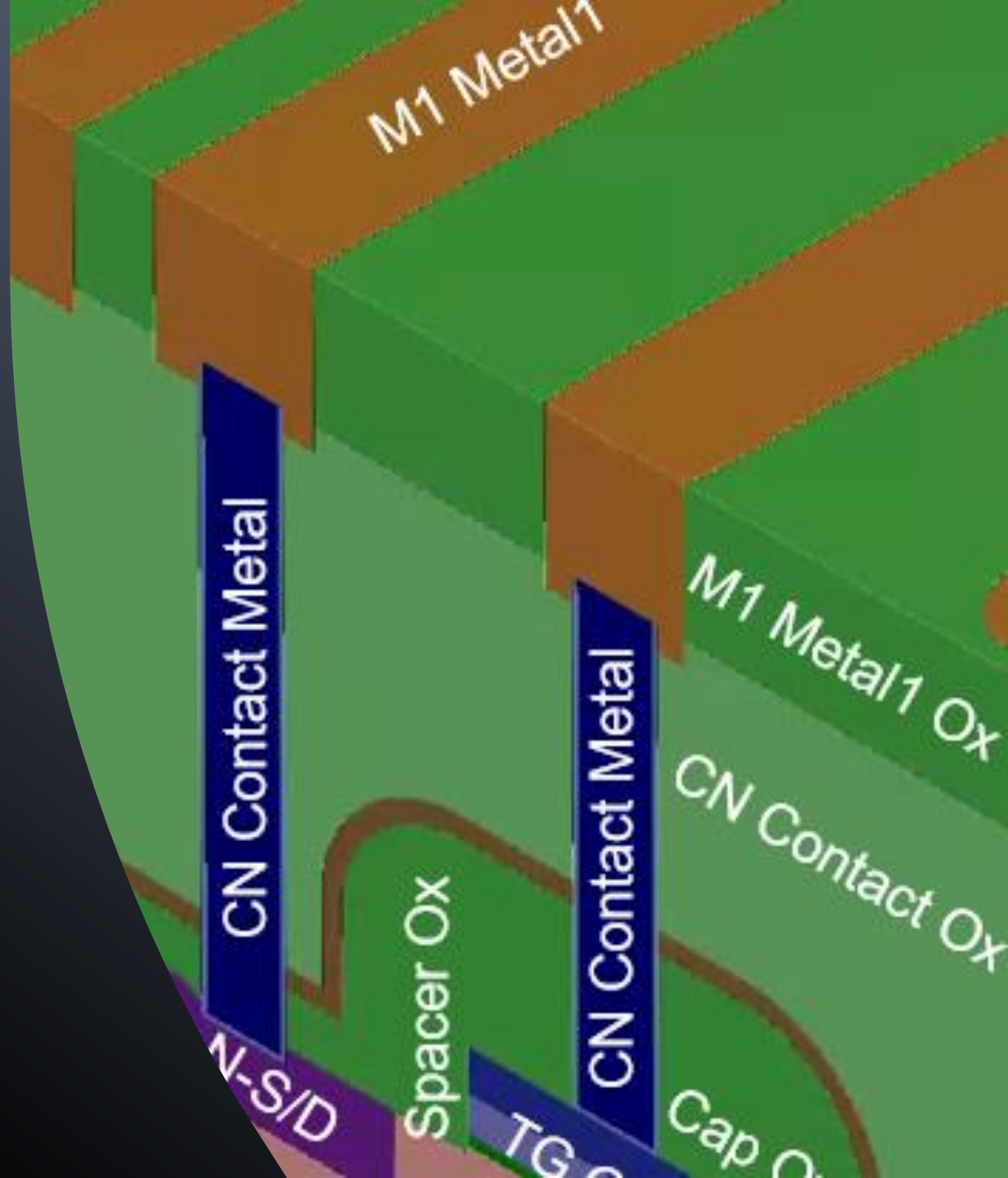
Photo Mask Levels

- During the fabrication process, patterns are created on the wafer using a series of photomasks.
  - Each mask has a unique pattern
  - A typical DRAM or NAND flow may have dozens of different masks
- Micron convention is to assign a 2-digit alphanumeric code to each mask.
- The table below lists the masks that we will use for our simplified CMOS flow.

Code	Description
NW	N-Well (for PMOS devices)
PW	P-Well (for NMOS devices)
AA	Active Areas
TG	Transistor Gates
NA	N-Source/Drain (for NMOS devices)
PA	P-Source/Drain (for PMOS devices)
CN	Contacts (Transistors to Metal1)
M1	Metal1 Interconnects
BP	Passivation and Bond Pads

Basic CMOS Process Flow (Traveler)

micron



Basic CMOS Traveler

- In the next slides we will show a simplified traveler used to build CMOS transistors (NMOS and PMOS transistors) along with contacts and a metal routing layer.
- As new traveler steps are introduced, we will provide a brief description of the Fab Areas that perform those steps

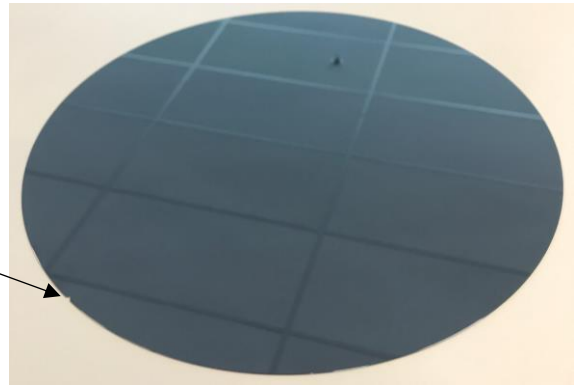
Step #	Traveler Step	Fab Area
1	WAFER START	SUPPORT
2	PAD OXIDE GROWTH	DIFFUSION
3	NITRIDE DEPOSIT	DIFFUSION
4	NW N-WELL PHOTO	PHOTO
5	NW N-WELL IMPLANT	IMPLANT
6	NW RESIST STRIP	DRY ETCH
7	PW P-WELL PHOTO	PHOTO
8	PW P-WELL IMPLANT	IMPLANT
9	PW RESIST STRIP	DRY ETCH
10	AA HARDMASK DEPOSITION	CVD
11	AA ACTIVE AREAS PHOTO	PHOTO
12	AA HARDMASK DRY ETCH	DRY ETCH
13	AA STI DRY ETCH	DRY ETCH
14	AA RESIST STRIP	WET PROCESS
15	AA STI OXIDE DEPOSIT	CVD
16	AA STI OXIDE CMP	CMP

*Metrology, RDA and Wet Process cleans not listed

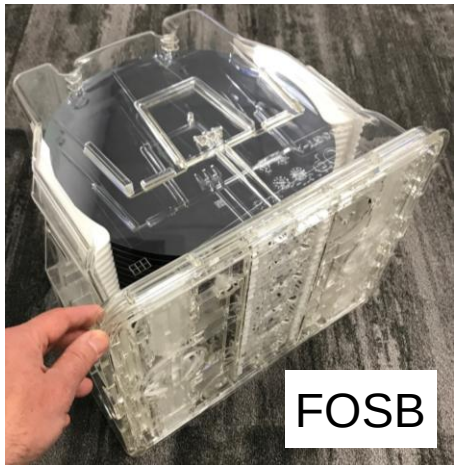
CMOS = Complimentary Metal Oxide Semiconductor Transistor
PMOS = P-Channel Metal Oxide Semiconductor Transistor
NMOS = N-Channel Metal Oxide Semiconductor Transistor

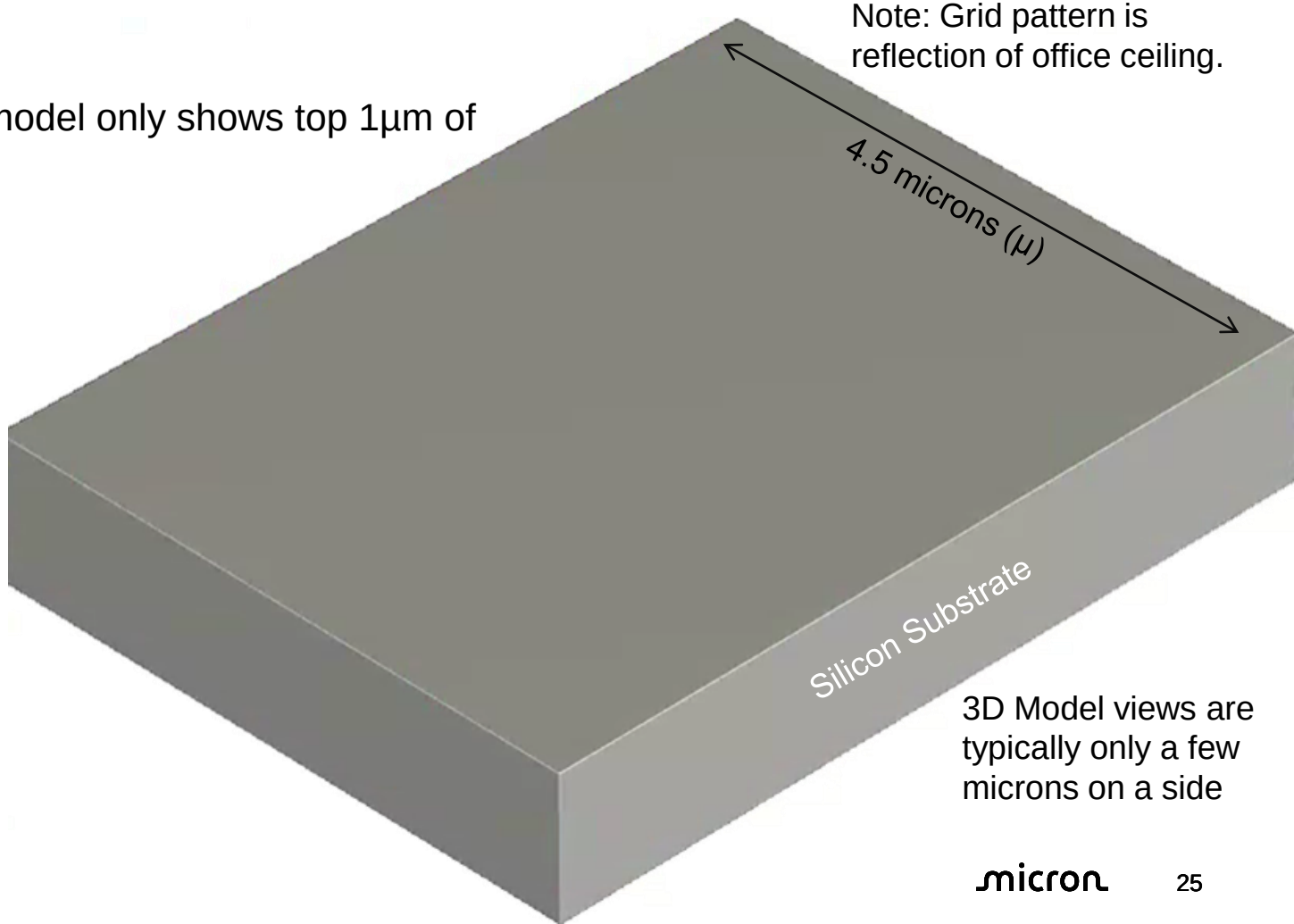
WAFER START with BARE SILICON SUBSTRATE

- Double-side polished bare silicon wafers (with alignment “notch”), also called Silicon Substrates, are received from our external suppliers in 25-wafer Front-Opening Shipping Boxes (FOSB)
  - Wafers are transferred into a Front-Opening Unified Pod (FOUP) in which they will reside as they move from tool to tool during their whole processing “life” within the fab cleanroom
  - Typical Wafer Specs:
    - Thickness = less than 1 mm (3D model only shows top 1µm of Si thickness)
    - Diameter = 300 mm
    - Resistivity = lightly doped P-type



Note: Grid pattern is reflection of office ceiling.





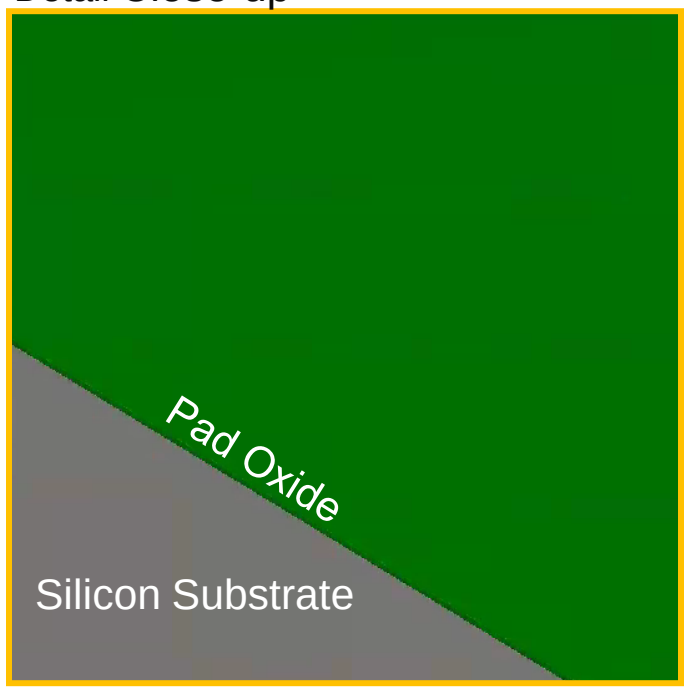
3D Model views are typically only a few microns on a side

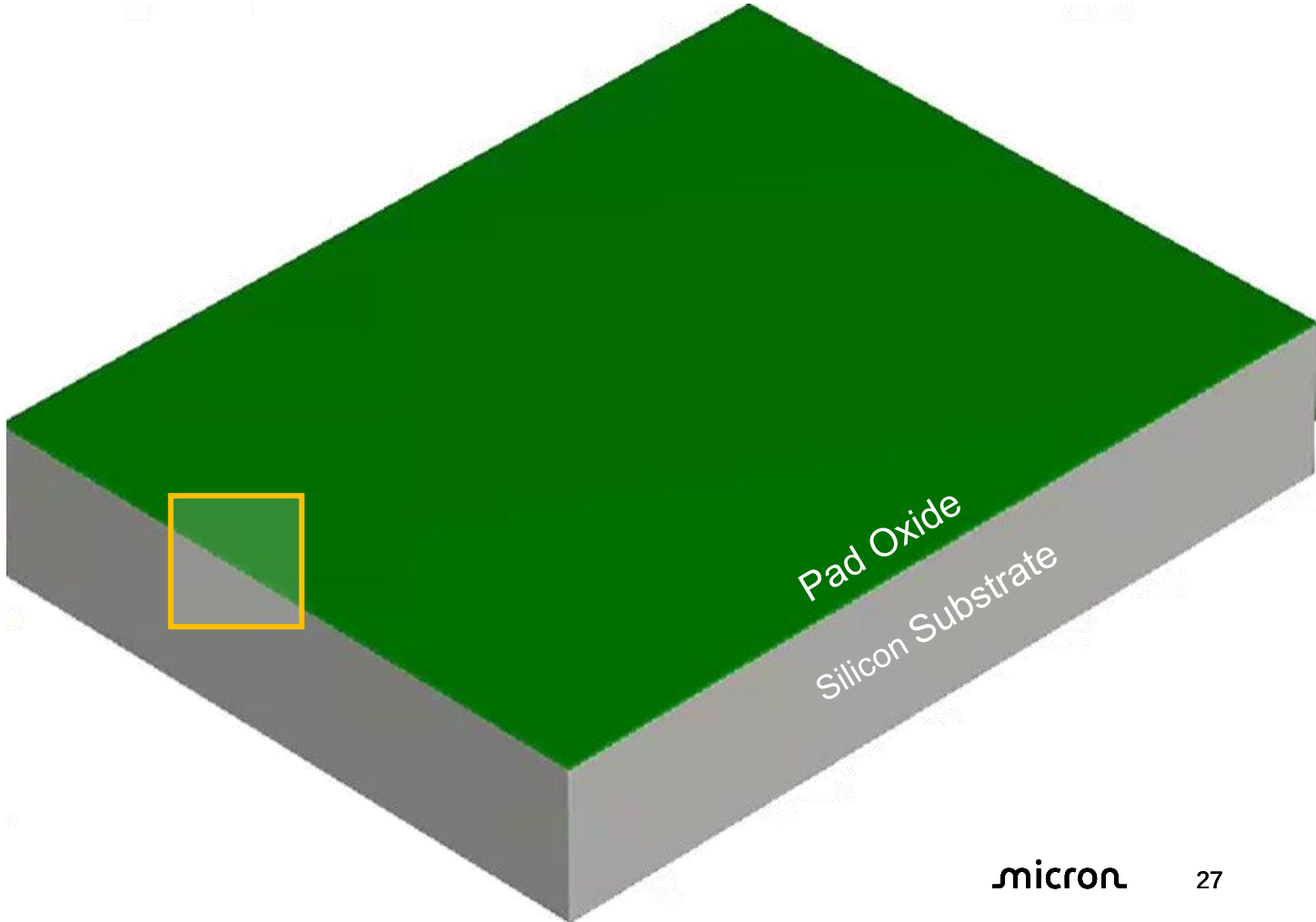
…for the record… 300mm is the size of a record

PAD OXIDE GROWTH [DIFFUSION]

- In the **Diffusion Area** a thin film of silicon dioxide is grown on the surface of the wafer to protect the silicon substrate from surface damage during implants and to keep the surface clean and free from defects.
- Silicon dioxide is usually referred as “oxide” and is an insulator or dielectric
- This specific oxide in this location of the traveler is sometimes called “Pad Oxide”

Detail Close-up

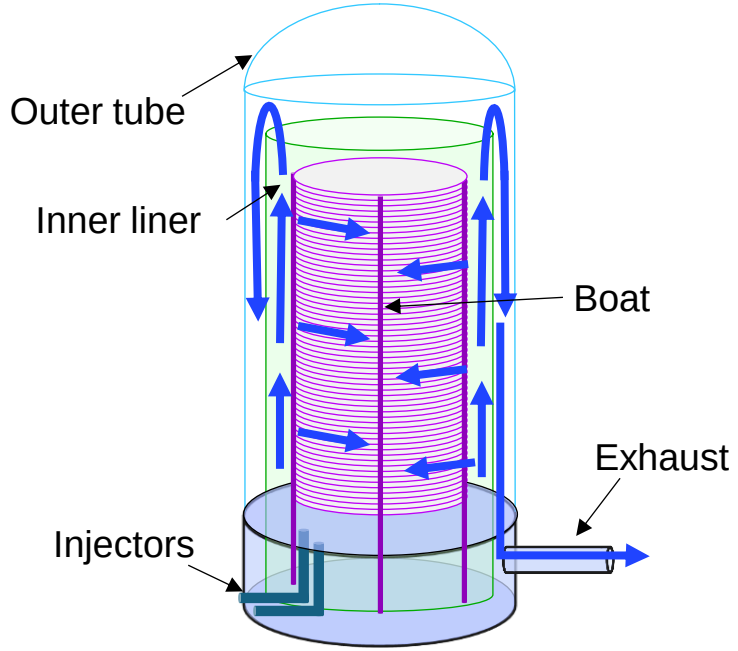




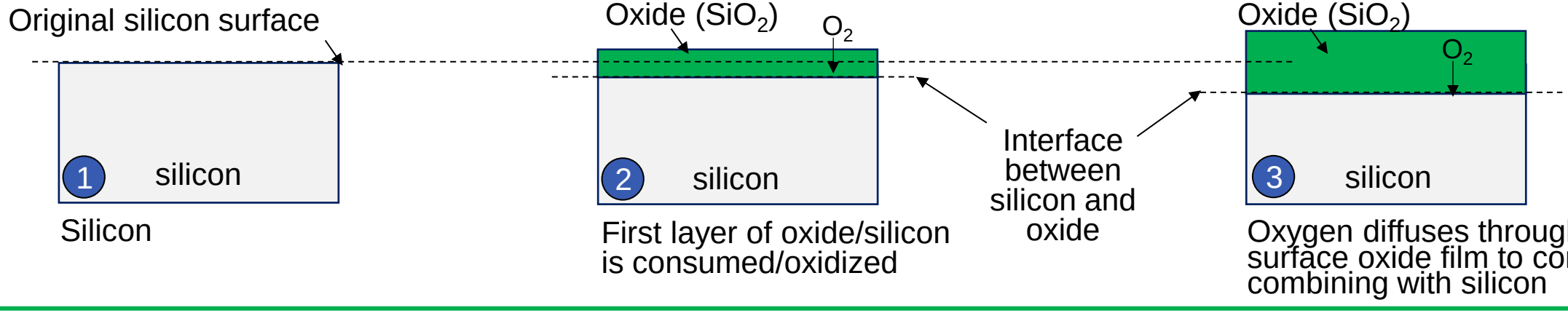
Oxidation (Diffusion)

- The Diffusion area of the fab consists primarily of vertical furnace tubes where many wafers can be processed at a time (a batch process – upwards of 125-wafers at a time)
- Different processes take place in Diffusion, including:
  - **Oxidation** – introduce oxygen to grow a high-quality silicon dioxide (SiO_2) layer on exposed silicon (process shown below)
  - **Deposition** – introduce gases that combine to form a film that is deposited on wafer (similar to CVD)
  - **Heat treatment** – needed to repair damage or achieve certain electrical results

Photo and schematic of a Diffusion vertical furnace tube



Oxidation Process

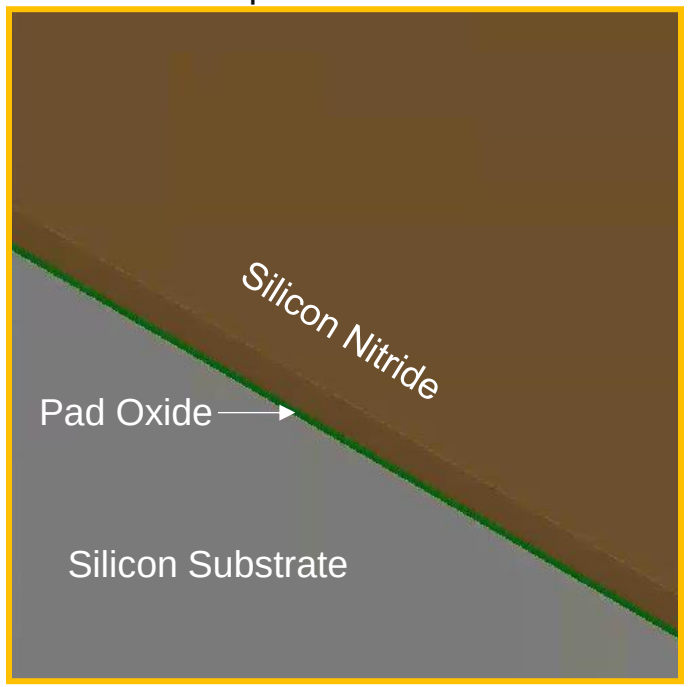


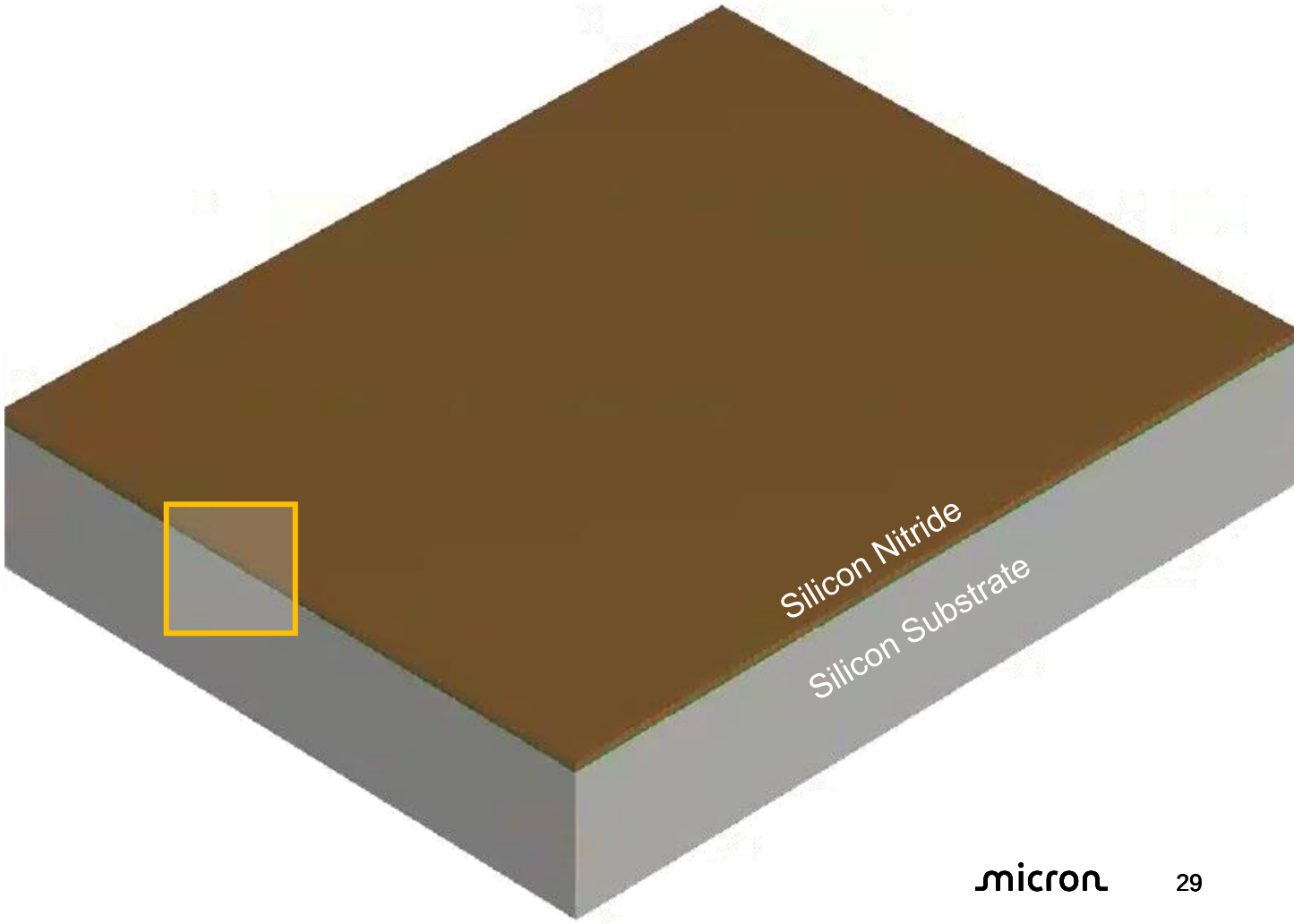
CVD = Chemical Vapor Deposition

NITRIDE DEPOSIT [DIFFUSION]

- In the **<u>Diffusion Area</u>** a thin film of silicon nitride (Si_3N_4) is deposited on top of the Pad Oxide. This silicon nitride film will be used later in the flow as a stop layer for a polishing process.
- Silicon nitride is usually referred as “nitride”

Detail Close-up

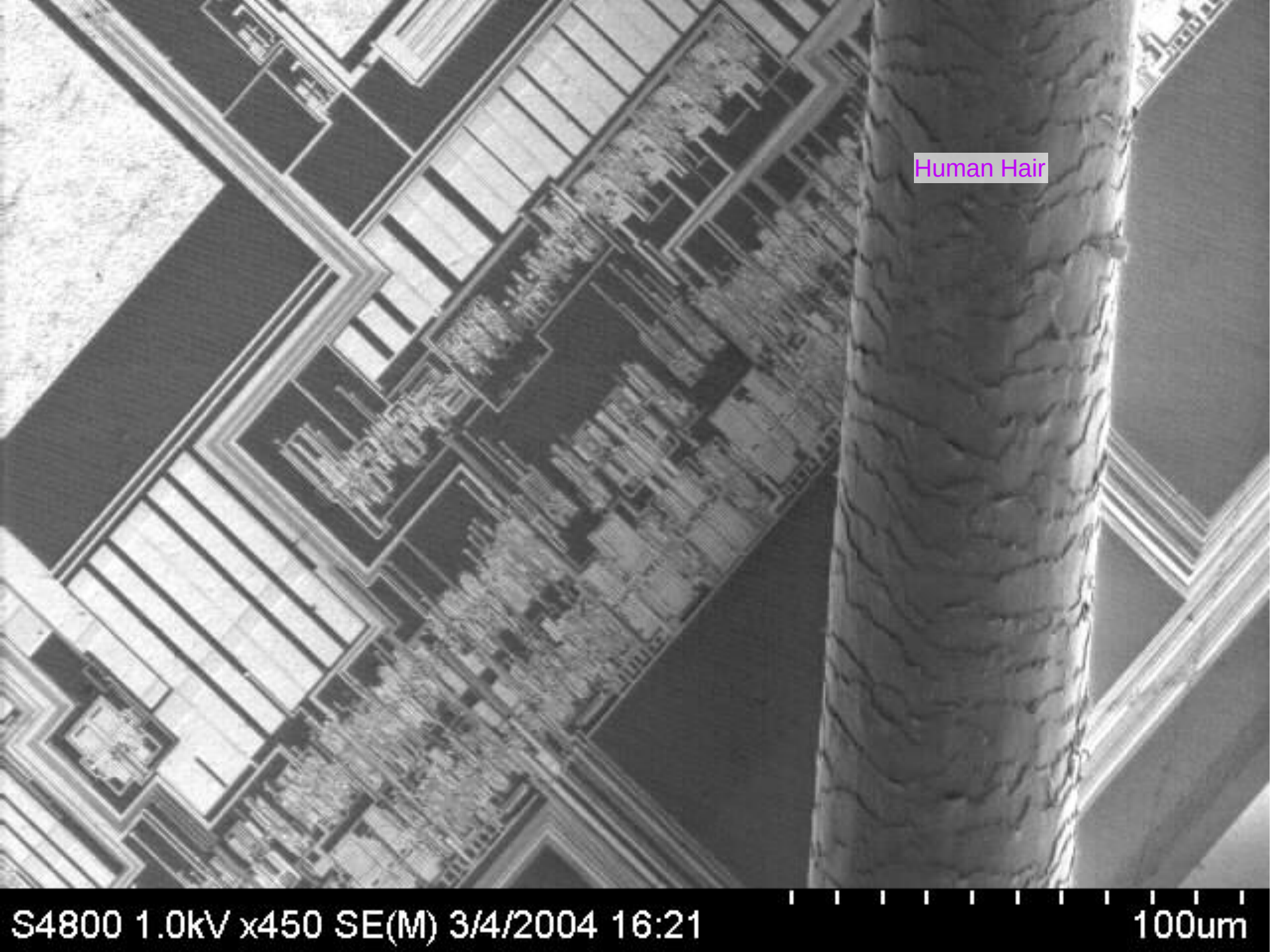




Circuit Elements with Human Hair

This hair is ~60 µ wide.

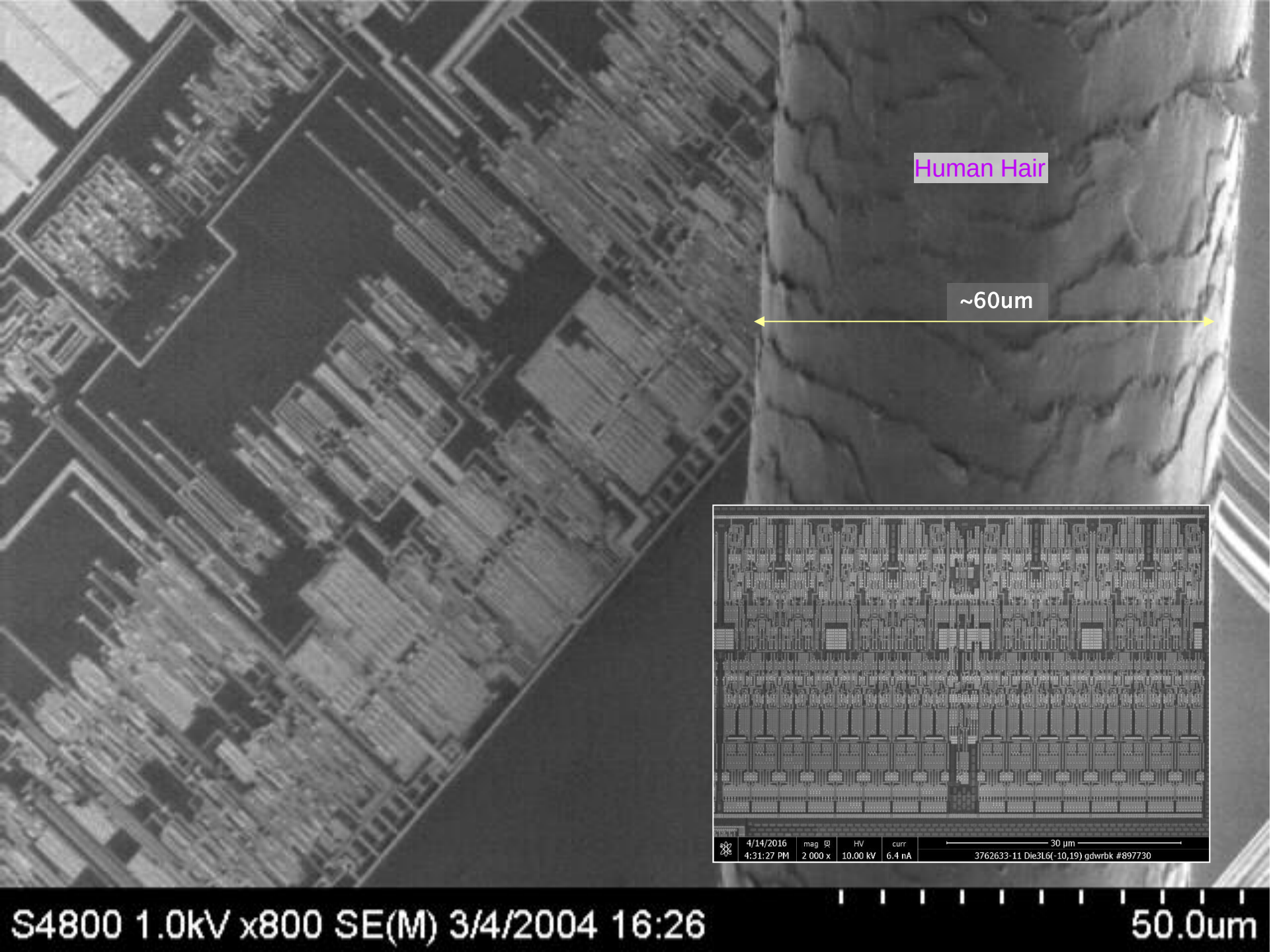
Hair may range 40-120 µ wide.



Circuit Elements with Human Hair

This hair is ~60 µ wide.

Hair may range 40-120 µ wide.



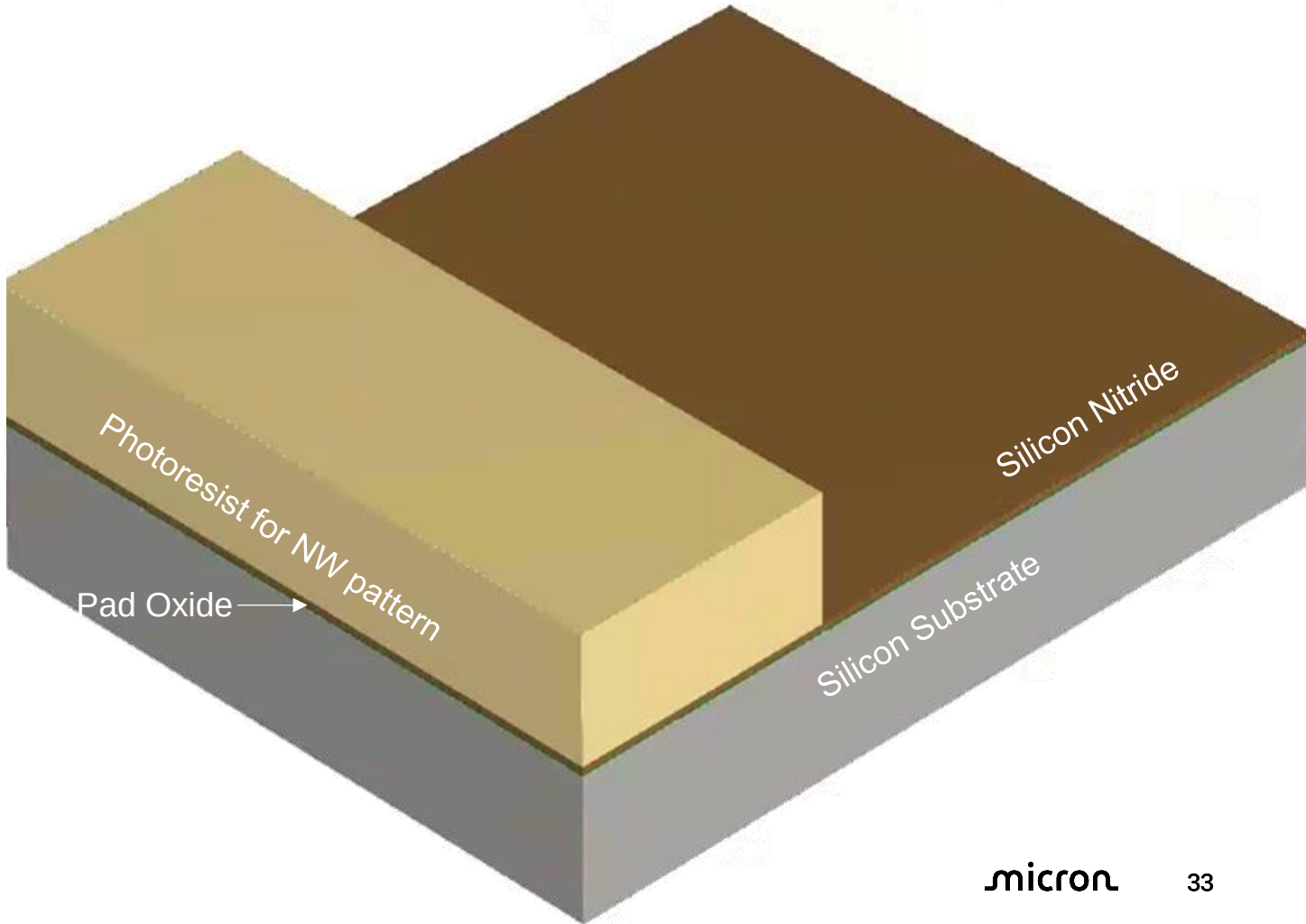
Circuit Elements with Human Hair

This hair is ~60 µ wide.

Hair may range 40-120 µ wide.

NW N-WELL PHOTO PATTERN [PHOTO]

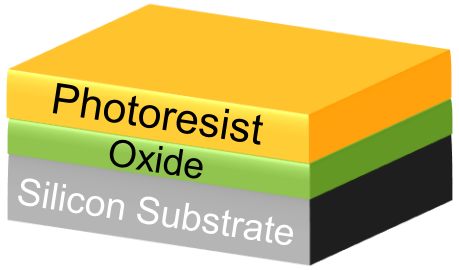
- In the **Photolithography Area** the “NW” reticle or mask is used to define a pattern in photoresist. The pattern will open certain areas where N-Wells are needed for the formation of PMOS transistor devices.
- Metrology:
  - Resist Thickness: ~ very thick to block implant



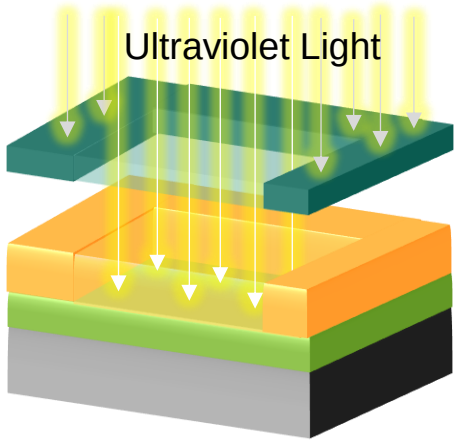
PMOS = P-Channel Metal Oxide Semiconductor Transistor

Photolithography

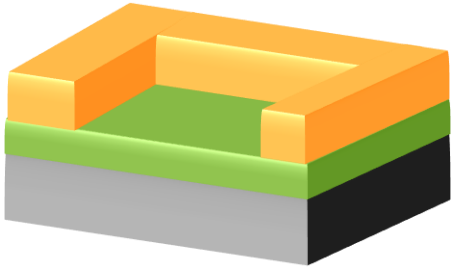
- The Photolithography area defines a temporary pattern that other areas (usually Dry Etch or Implant) use as a mask to create the structures needed on the wafer.
- The temporary pattern is created on a photosensitive film called photoresist (or resist).
- Patterns created on the wafer follow the five steps shown below.
- The first three steps shown are performed in the photo-lithography area
- Different light wavelengths are used in the industry. The smaller the wavelength the smaller the features that can be printed. Example: Immersion 193nm can print features down to 37nm and EUV can print ~15nm
- Modern Travelers have several dozen photolithography levels
- Photoresist is “sacrificial” as only used temporarily to define patterns and once used any remaining resist is removed or stripped.

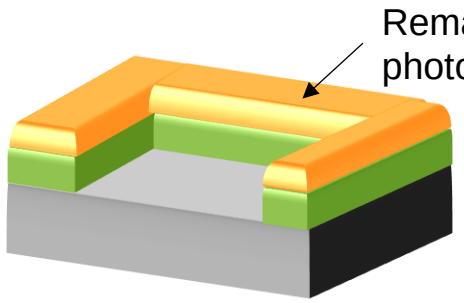


1. Apply Photoresist

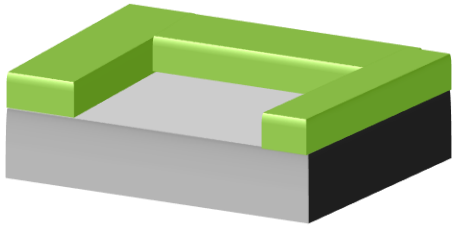


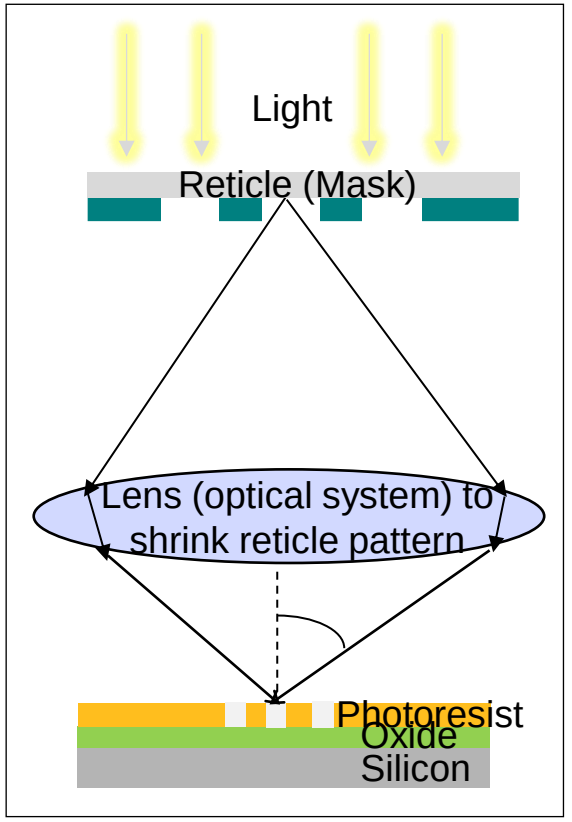
2. Expose Photoresist


3. Develop (remove exposed photoresist)



4. Etch (or Implant)

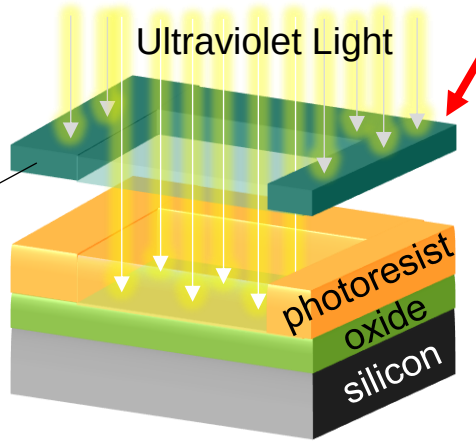

5. Strip Photoresist

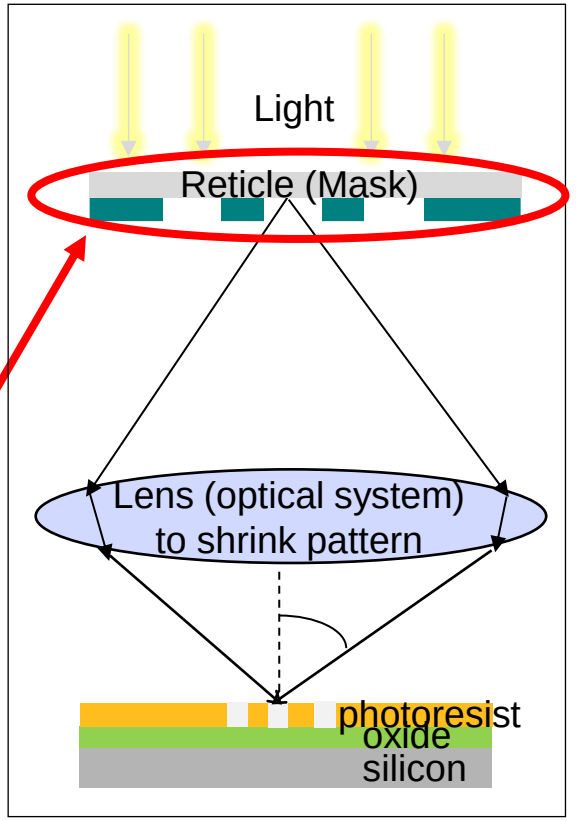


EUV: Extreme Ultraviolet Lithography

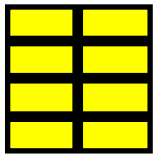
Reticles

- Reticles, also called Masks, are used in the Photolithography scanner to expose a temporary pattern on the surface of the silicon wafer.
- The reticle is a quartz plate with a chrome and other layers deposited across one side, into which patterns are exposed and etched in reticle fabrication.
- The patterns are 4 times larger on the reticle and the optical lens system reduces those to their desired size on the wafer.

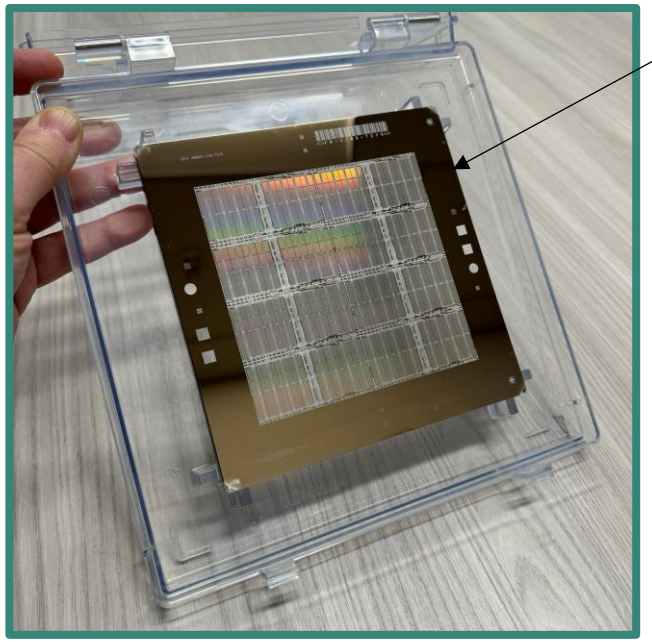


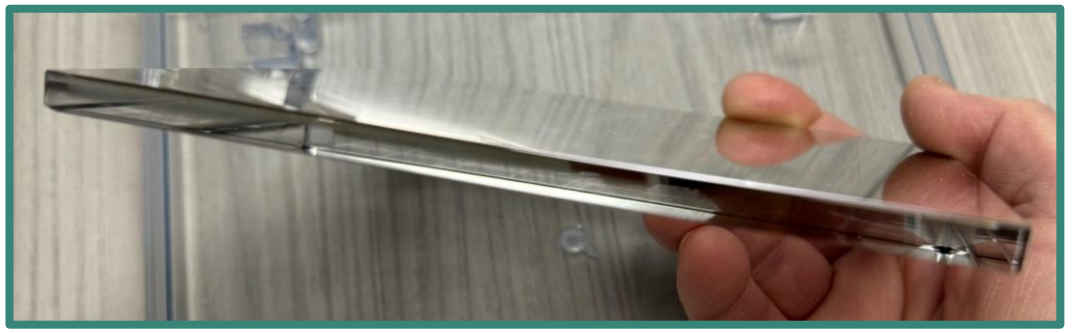


- Reticles typically have die patterned in an x by y array.
- The reticle shown here has a 2 die x 4 die layout.



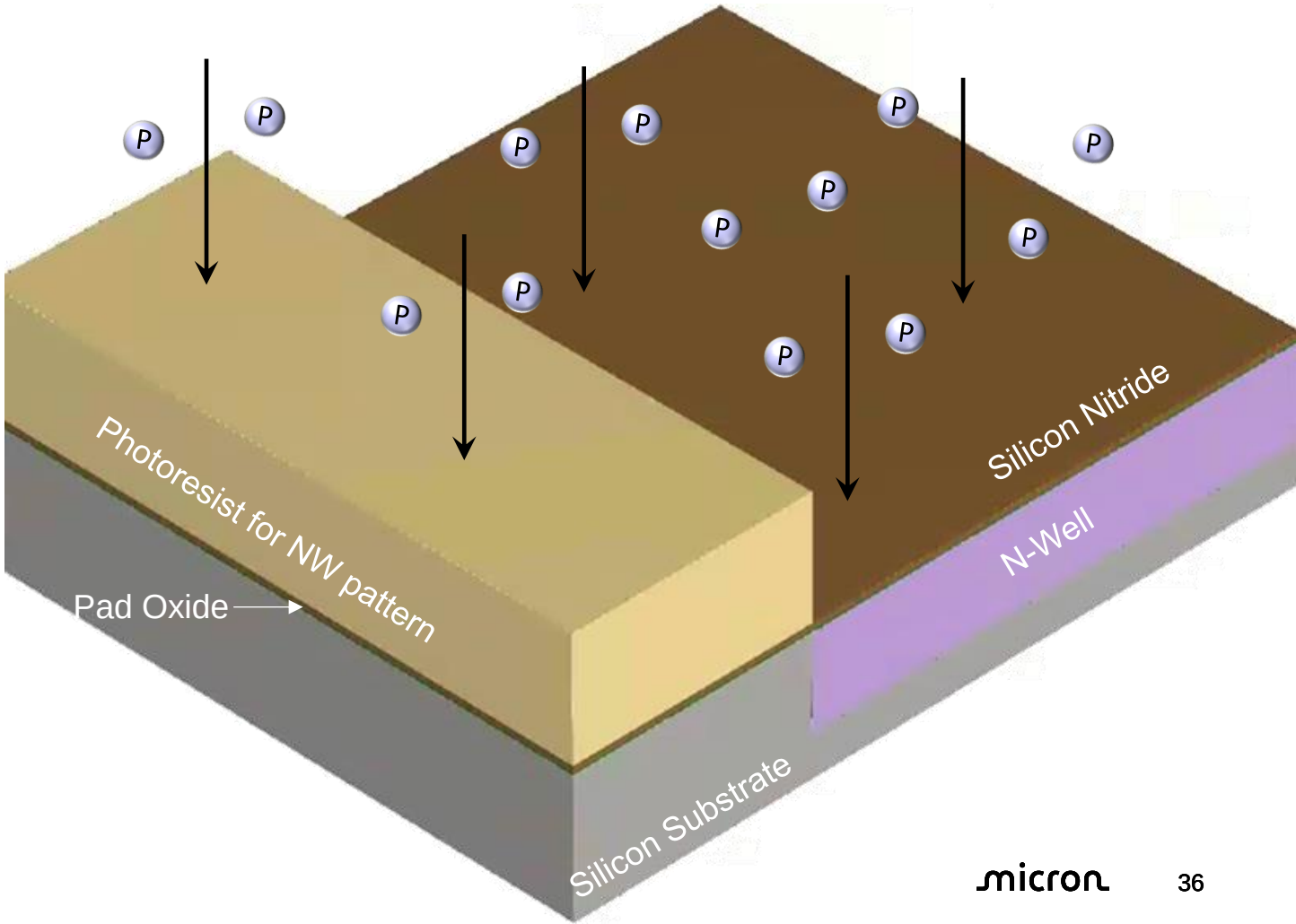
- The spaces in between die are used for inline process monitoring structures as well as electrical devices that can be tested inline or at the end of wafer processing.





NW N-WELL IMPLANT [IMPLANT]

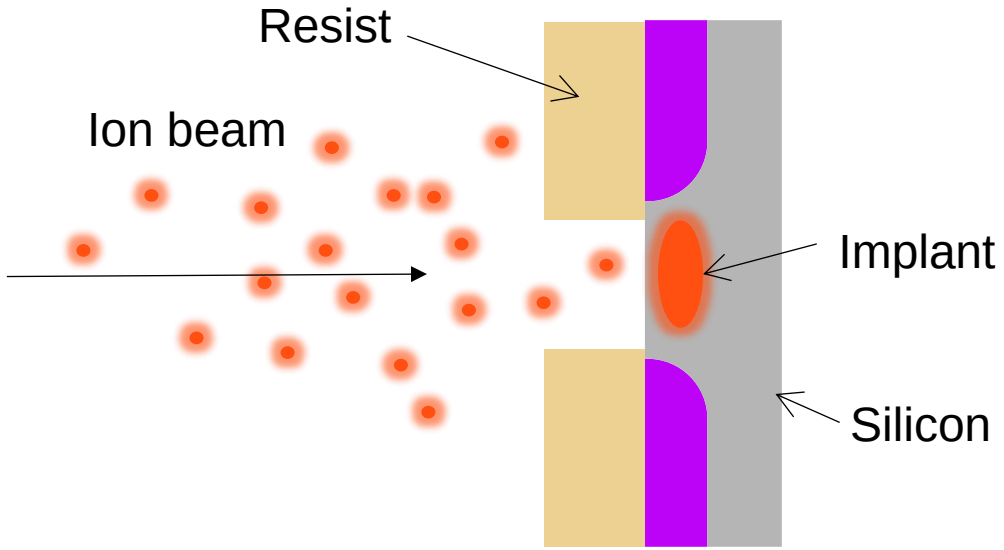
- In the **Implant Area** an ion implanter shoots phosphorous ions deep into the silicon to create an N-Well. The N-Well will provide the background doping needed to form PMOS transistors. The thick photoresist prevents the ions from entering the wafer in areas where N-Wells are not needed.
- Doping is explained in the following slides.
- Metrology:
  - Implant Depth: deep implant
  - Implant Dose: Low (needed for transistor characteristics)

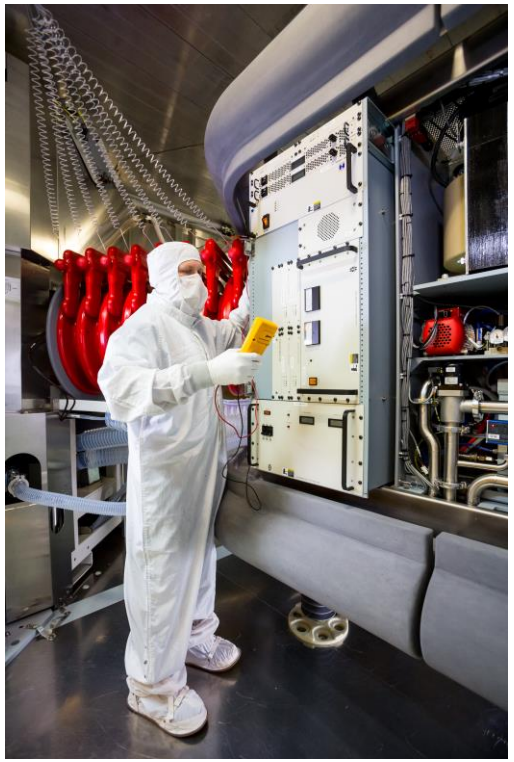


PMOS = P-Channel Metal Oxide Semiconductor Transistor

Ion Implantation

- Dopants are introduced into the silicon via a high-energy beam of ions that is directed at the wafer surface.
- The electrical properties of the silicon wafer are modified by “doping” with selected impurities.
- The most common dopants are boron, phosphorous, and arsenic.
- In most cases, a photo pattern using thick resist is used to prevent the dopants from entering unwanted areas of silicon.

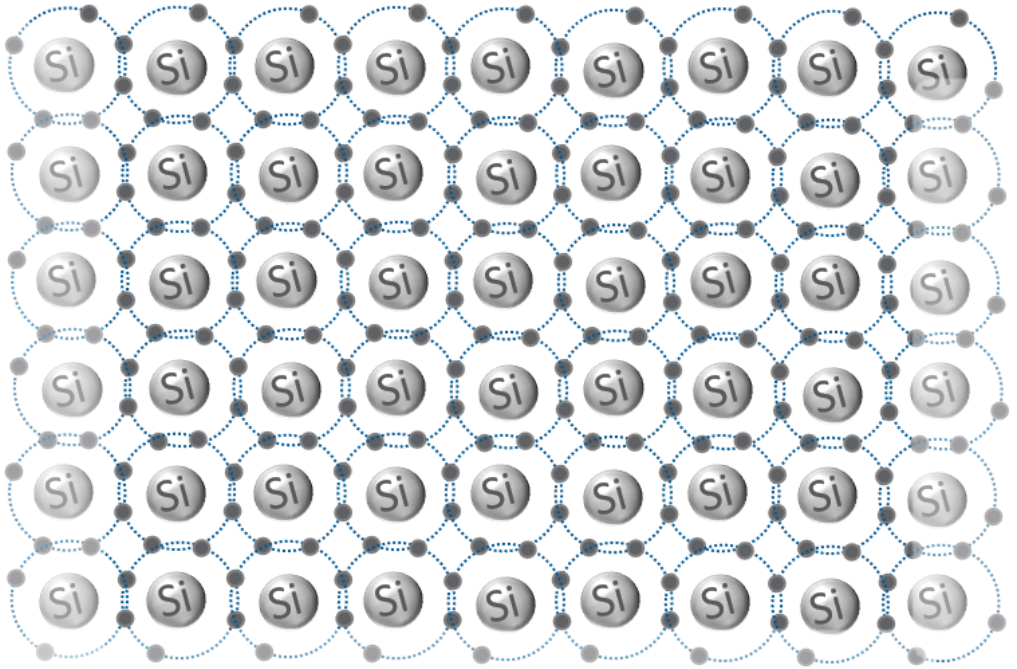




Picture of preventive maintenance work on an Implant tool

Ion Implantation & Heat Treatment

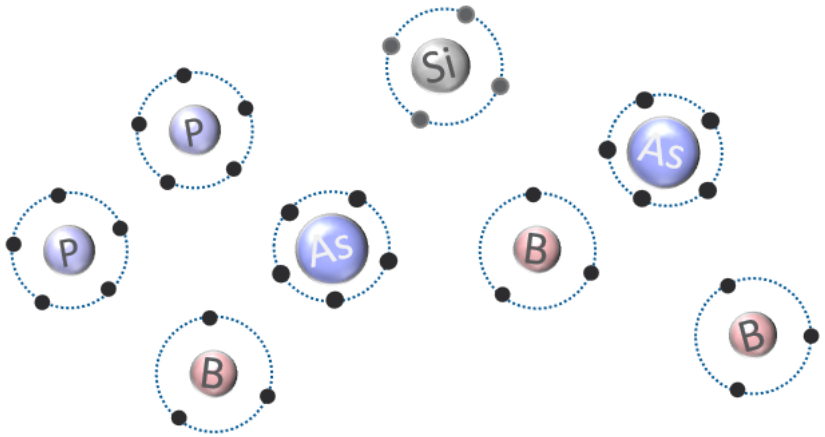
- After all dopants are introduced/implanted, wafers are generally run through a high temperature heat treatment to **anneal** initial CMOS implants



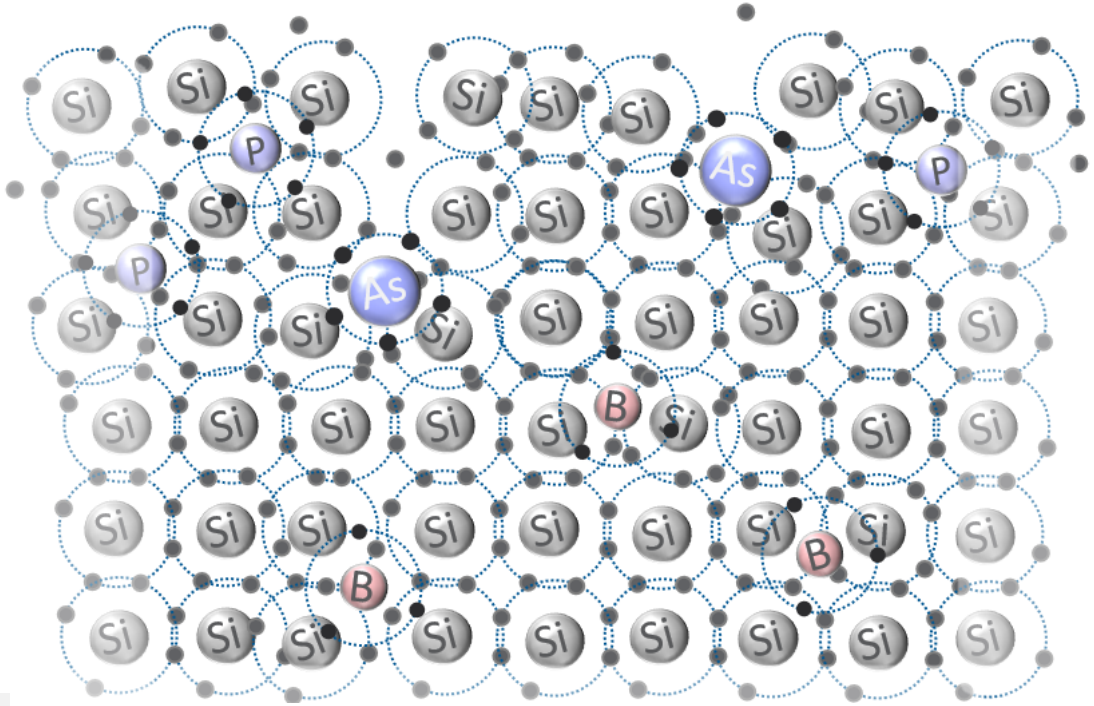
CMOS = Complimentary Metal Oxide Semiconductor Transistor

Ion Implantation & Heat Treatment

- After all dopants are introduced/implanted, wafers are generally run through a high temperature heat treatment to **anneal** initial CMOS implants



Before Anneal



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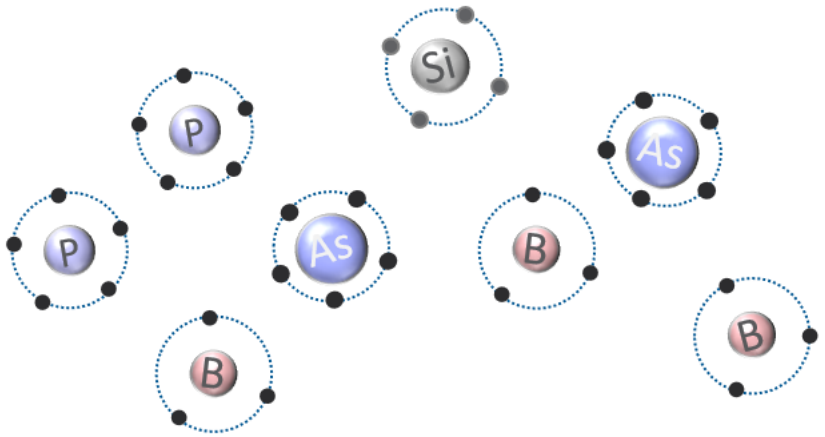
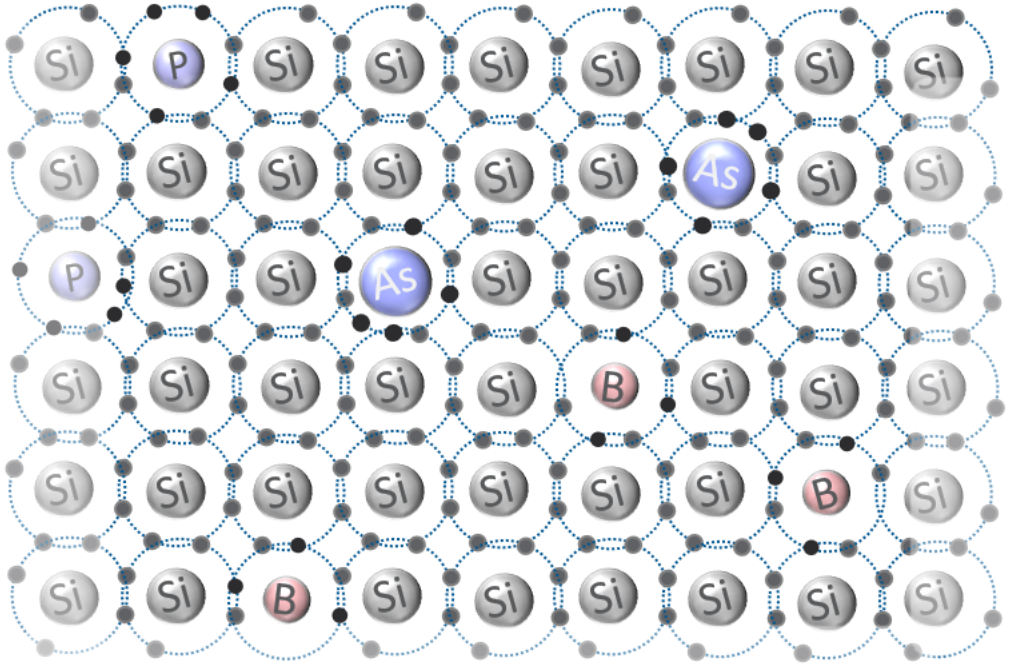


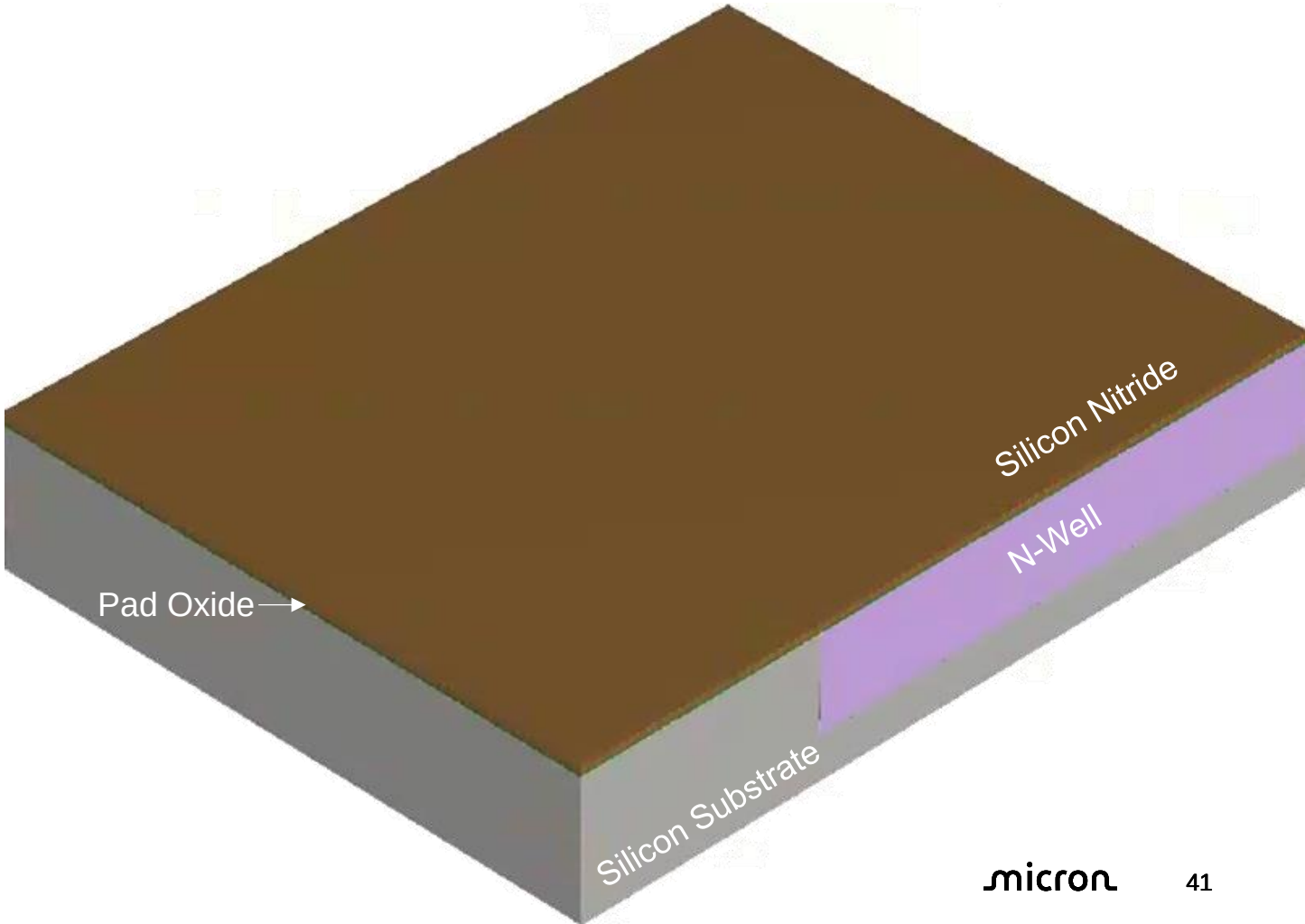
After Anneal



CMOS = Complimentary Metal Oxide Semiconductor Transistor

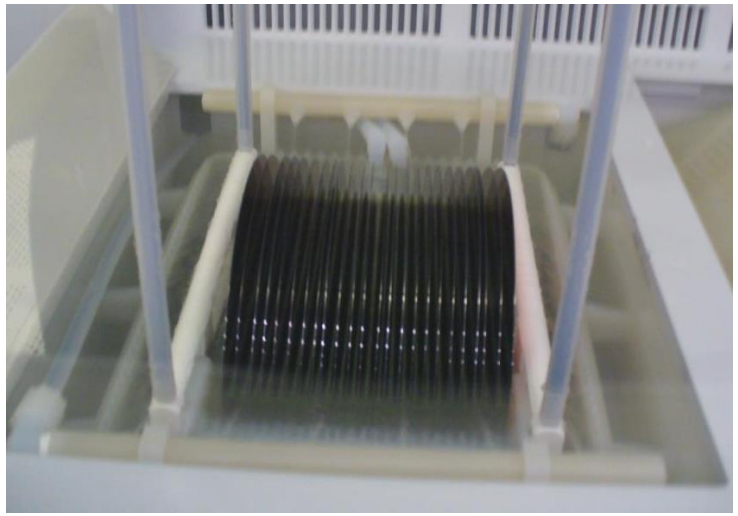
NW RESIST STRIP [WET PROCESS]

- In the **Wet Process Area** plasma and wet chemistry are used to remove the photoresist after the implant is complete.
- Metrology:
  - There should be no residual resist left on the wafer.



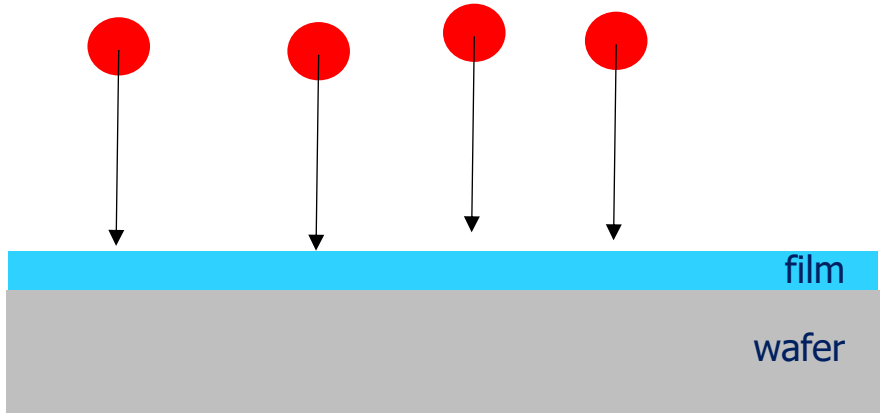
Wet Process – Wafer Cleaning

- The Wet Etch area uses chemical baths and de-ionized water to remove films and clean wafers to reduce defectivity.
- After every patterning operation, one or more wet process steps are used to remove the leftover photoresist and clean up residual organics, particles, and other forms of contamination.
- Wet process steps make up the largest percentage of the traveler.
- Multiple different chemistries are used to “selectively” remove some materials while leaving critical layers untouched.



Typical Wet Etch Process:

1. Wafer is immersed in or sprayed with wet chemicals



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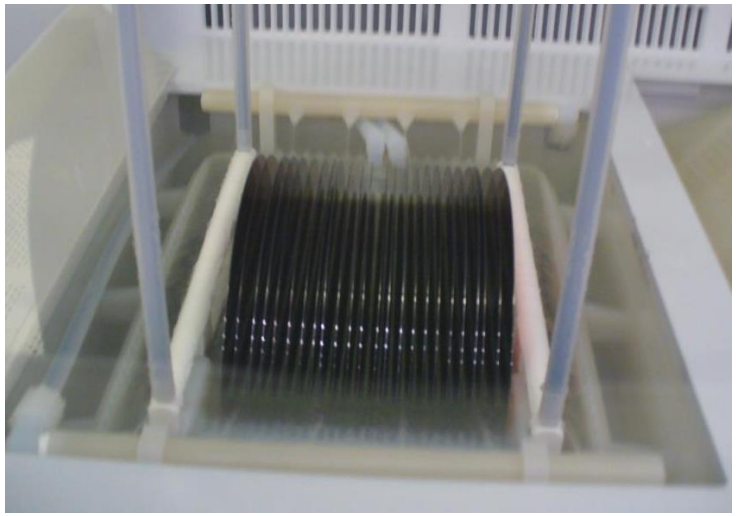
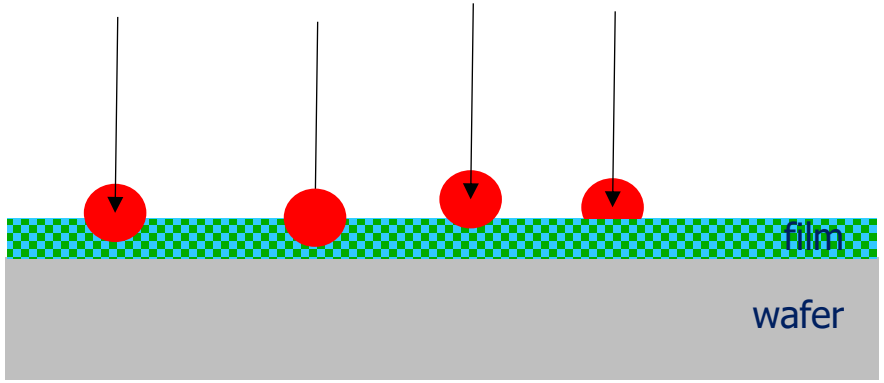


Typical Wet Etch Process:

1. Wafer is immersed in or sprayed with wet chemicals
2. Wet chemicals react with solid film constituents to break them down into solution



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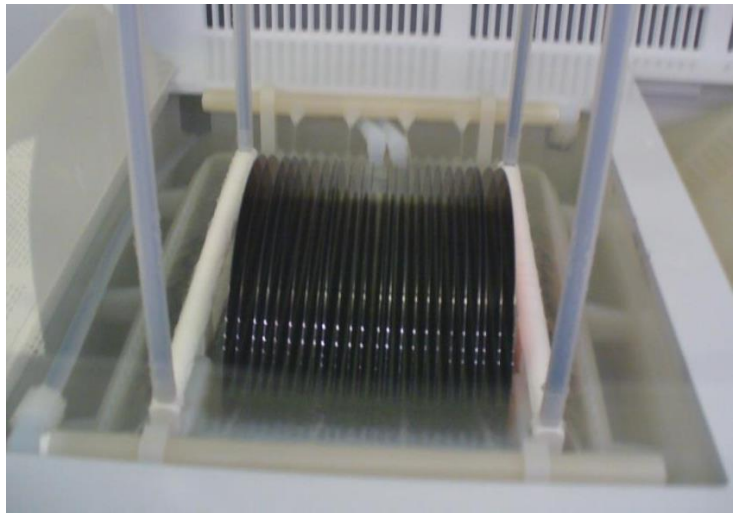

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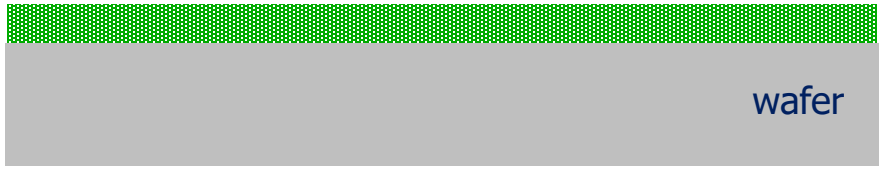

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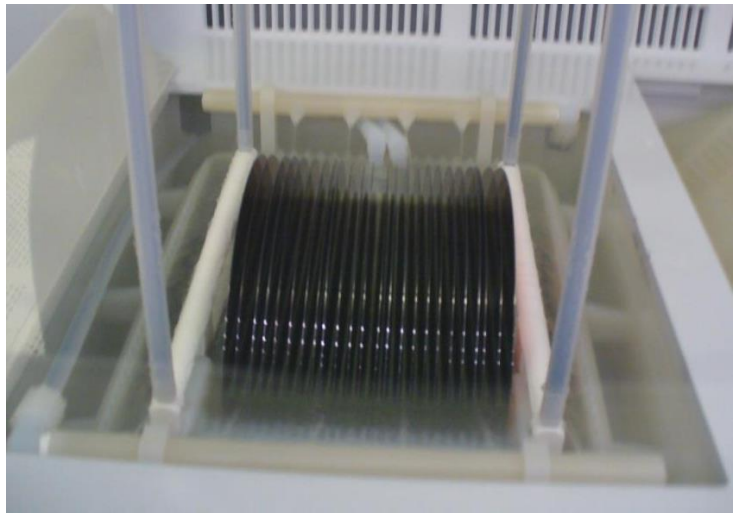
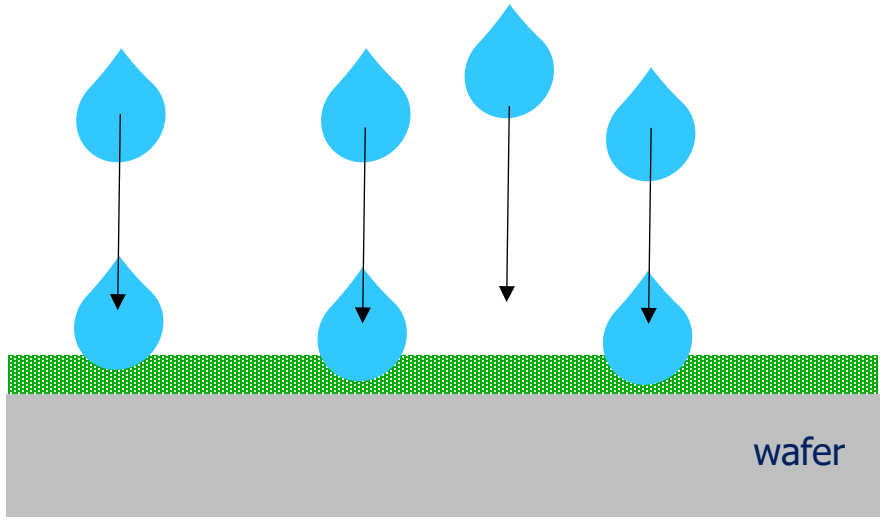


Typical Wet Etch Process:

1. Wafer is immersed in or sprayed with wet chemicals
2. Wet chemicals react with solid film constituents to break them down into solution
3. Wafer is immersed in or sprayed with DI water



DI = De-ionized Water

Wet Process – Wafer Cleaning

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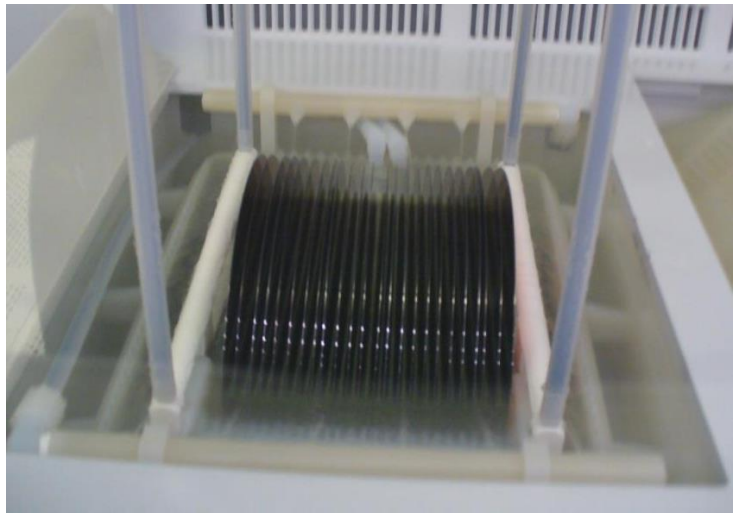
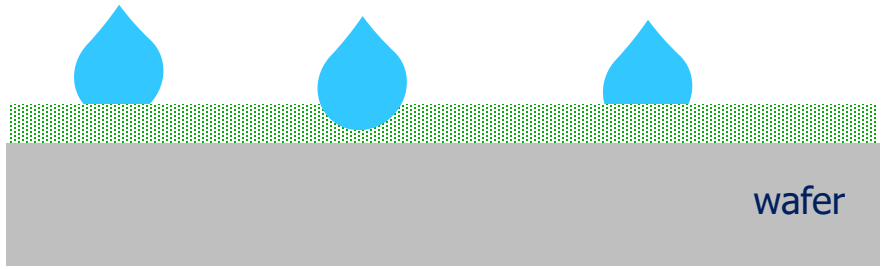


Typical Wet Etch Process:

1. Wafer is immersed in or sprayed with wet chemicals
2. Wet chemicals react with solid film constituents to break them down into solution
3. Wafer is immersed in or sprayed with DI water
4. DI water rinses away residual by-products and chemicals



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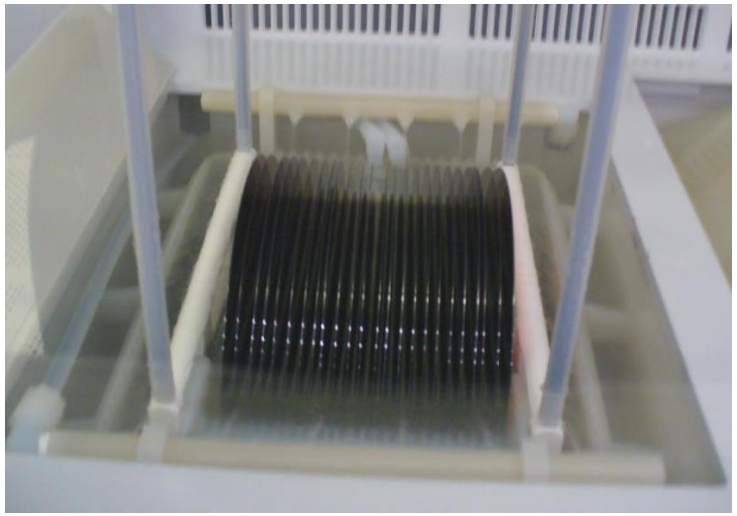


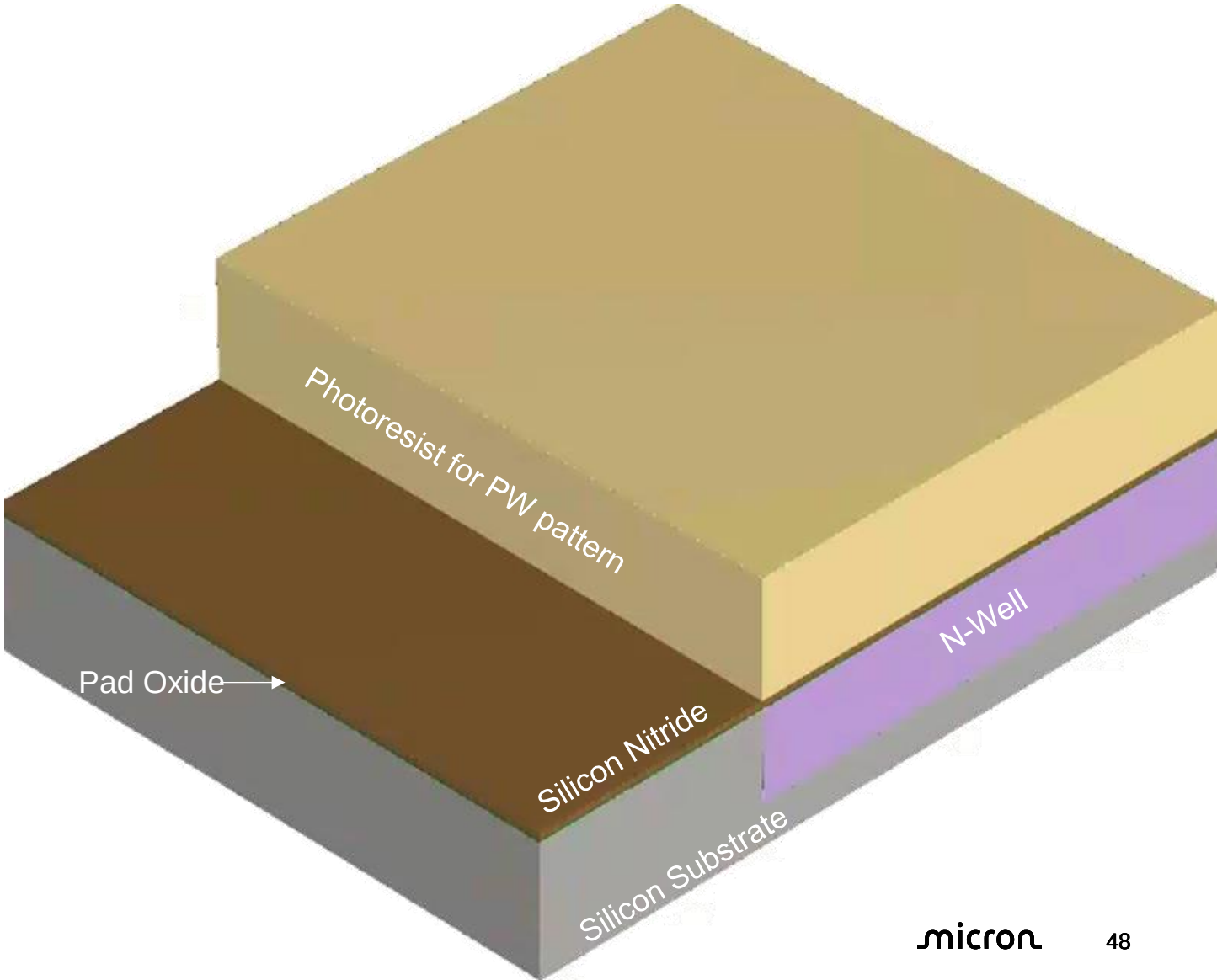
Typical Wet Etch Process:

1. Wafer is immersed in or sprayed with wet chemicals
2. Wet chemicals react with solid film constituents to break them down into solution
3. Wafer is immersed in or sprayed with DI water
4. DI water rinses away residual by-products and chemicals

DI = De-ionized Water

PW P-WELL PHOTO PATTERN [PHOTO]

- In the **Photolithography Area** the “PW” mask is used to define a pattern in photoresist. The pattern will open certain areas where P-Wells are needed for the formation of NMOS devices.
- Metrology:
  - Resist Thickness: very thick to block implant

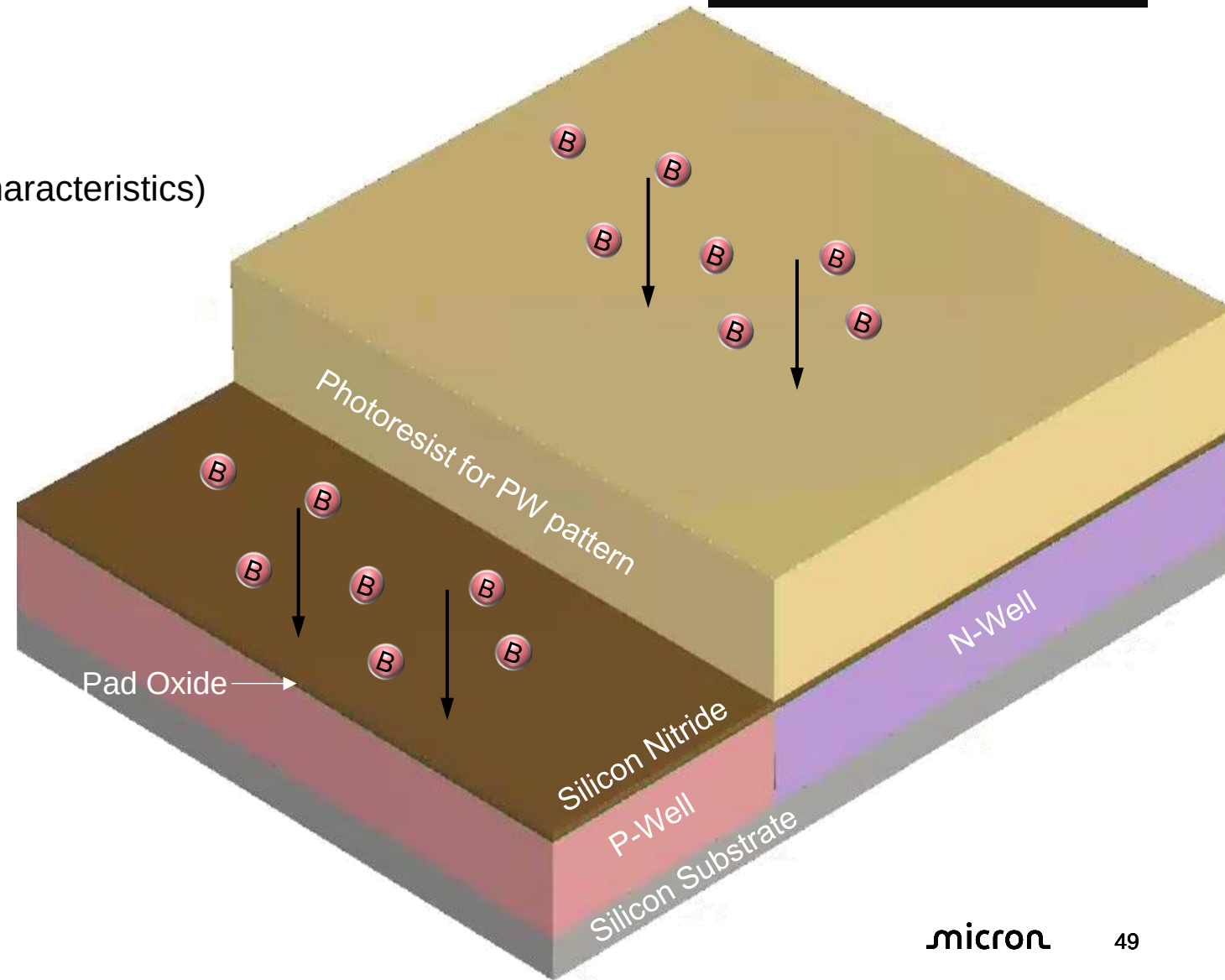


NMOS = N-Channel Metal Oxide Semiconductor Transistor

PW P-WELL IMPLANT [IMPLANT]

- In the **Implant Area** an ion implanter shoots boron ions deep into the silicon to create a P-Well. The P-Well will provide the background doping needed to form NMOS transistors. The thick photoresist prevents the ions from entering the wafer in areas where P-Wells are not needed.
- Metrology:
  - Implant Depth: deep implant
  - Implant Dose: Low (needed for transistor characteristics)

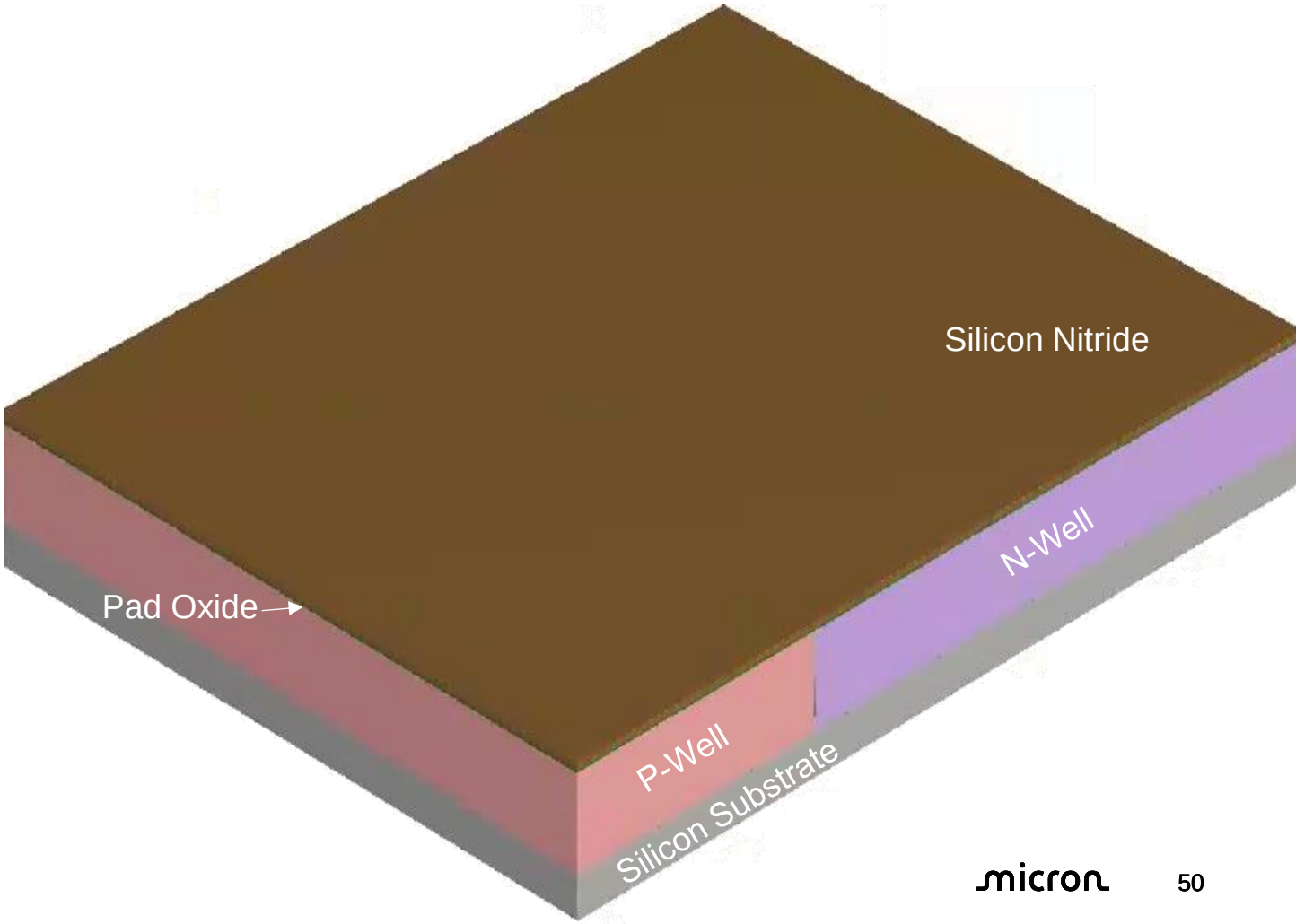
Q) What do you think is the next Traveler step?



NMOS = N-Channel Metal Oxide Semiconductor Transistor

PW RESIST STRIP [WET PROCESS]

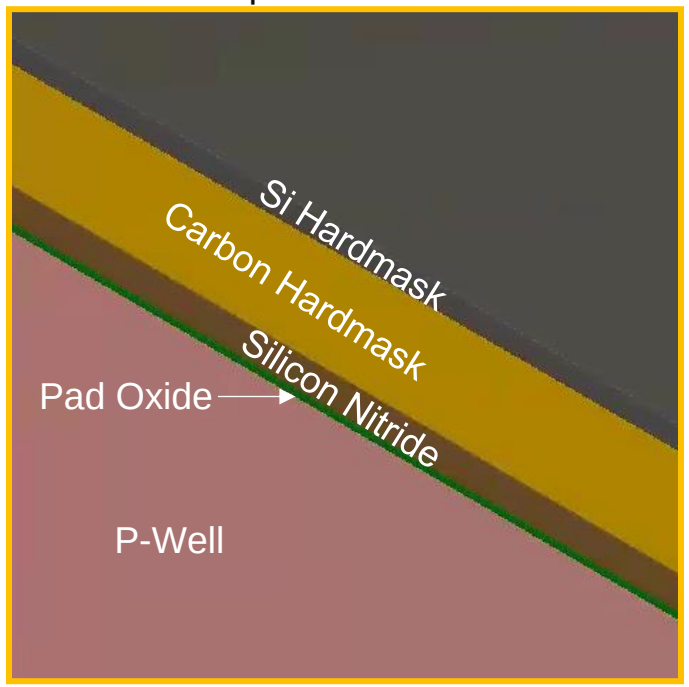
- In the **Wet Process Area** plasma and wet chemistry are used to remove the photoresist after the implant is complete.
- Metrology:
  - There should be no residual resist left on the wafer.

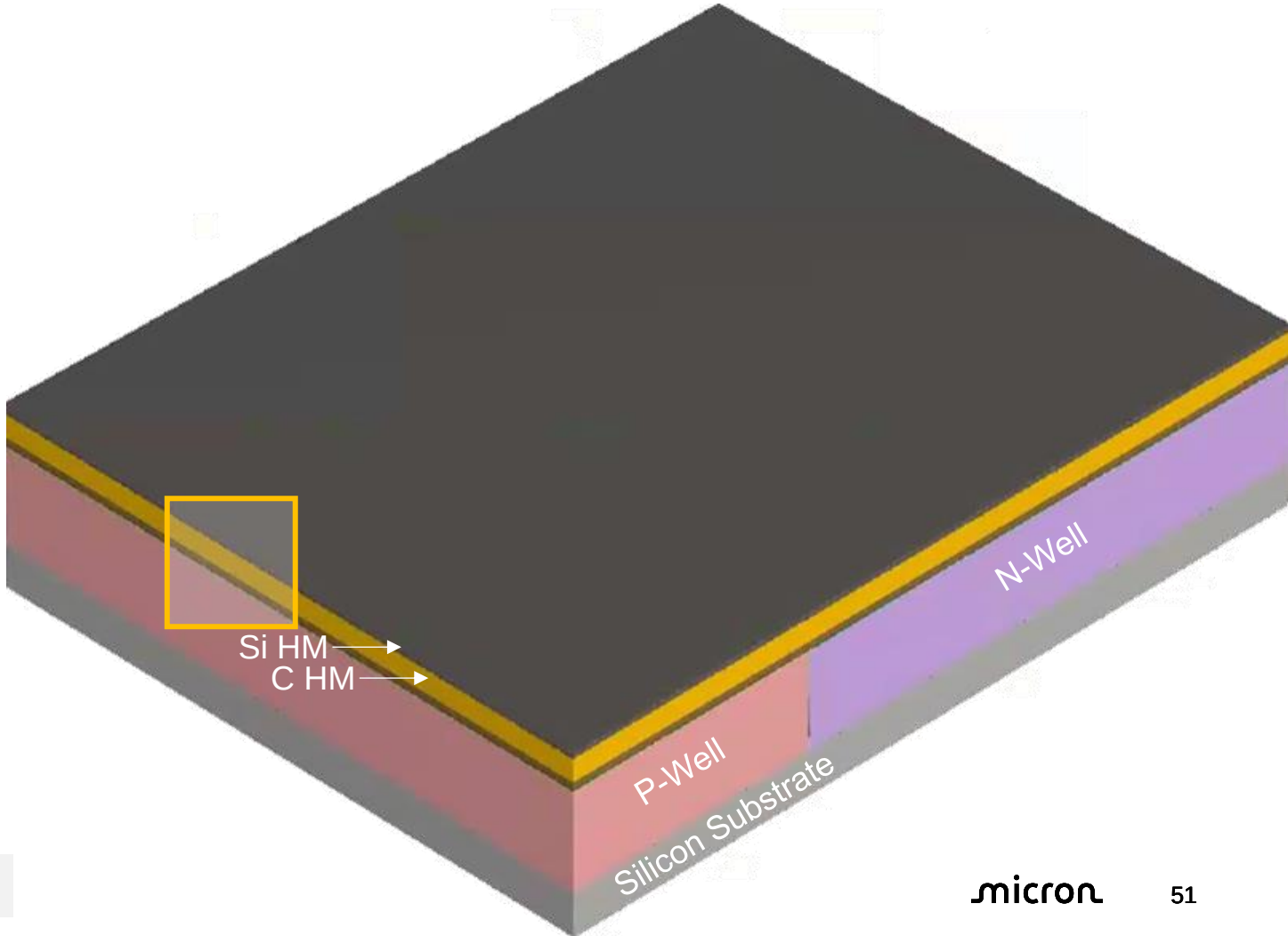


AA HARDMASK LAYERS DEPOSIT [CHEMICAL VAPOR DEPOSITION (CVD)]

- In the **CVD Area** a thick film of carbon (C) is deposited followed by a thin silicon-based (Si) film. Together these films comprise a “hardmask” which allows us to etch very small features while keeping the photoresist layer as thin as possible. Hardmasks are prevalent throughout this CMOS flow.

Detail Close-up

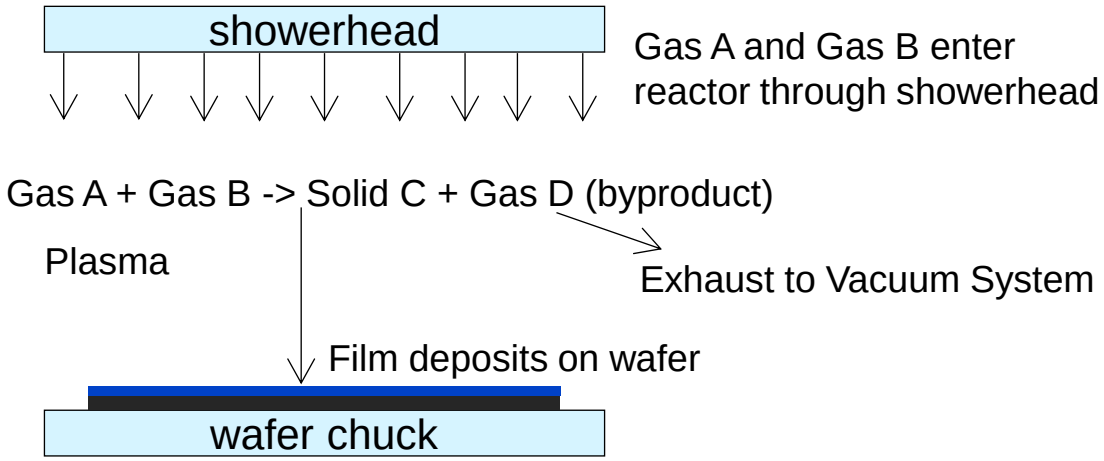




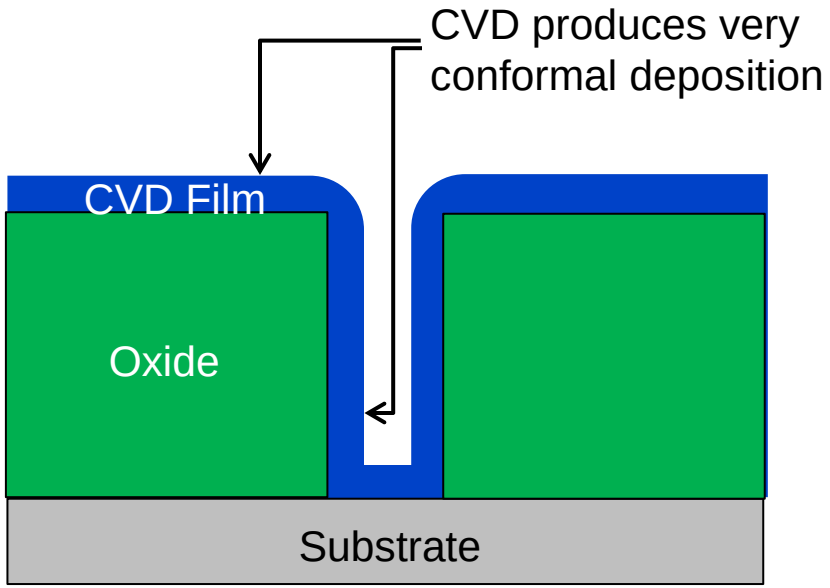
CMOS = Complimentary Metal Oxide Semiconductor Transistor

Chemical Vapor Deposition (CVD)

- CVD is used to deposit a variety of insulating and conductive films at multiple places in the Traveler.
- Gases are introduced into a chamber. A solid film, which is a product of the reaction, deposits on the wafer.
- Most CVD processes also use plasma technology (similar to dry etch).
- Compared to other deposition methods, CVD films can be very conformal, allowing us to fill very narrow holes and trenches without creating voids or gaps.



CVD Reactor – Vacuum Chamber



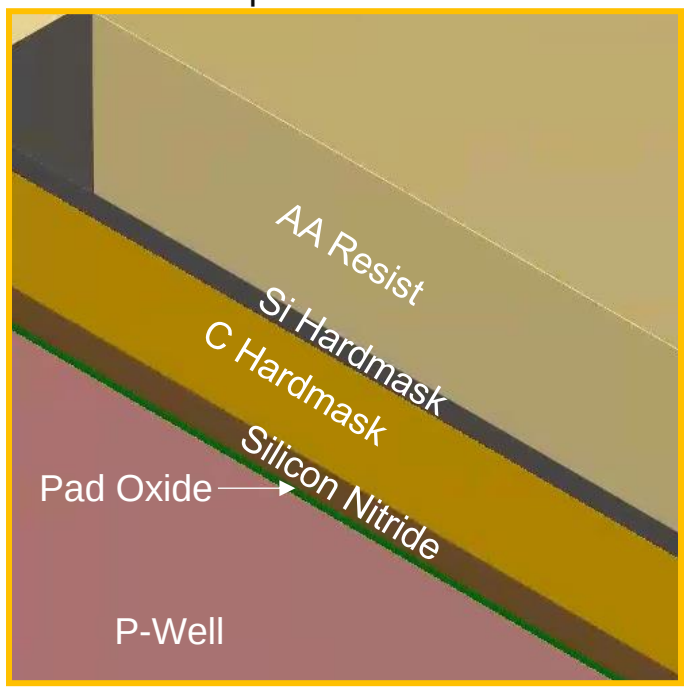
CVD Deposition

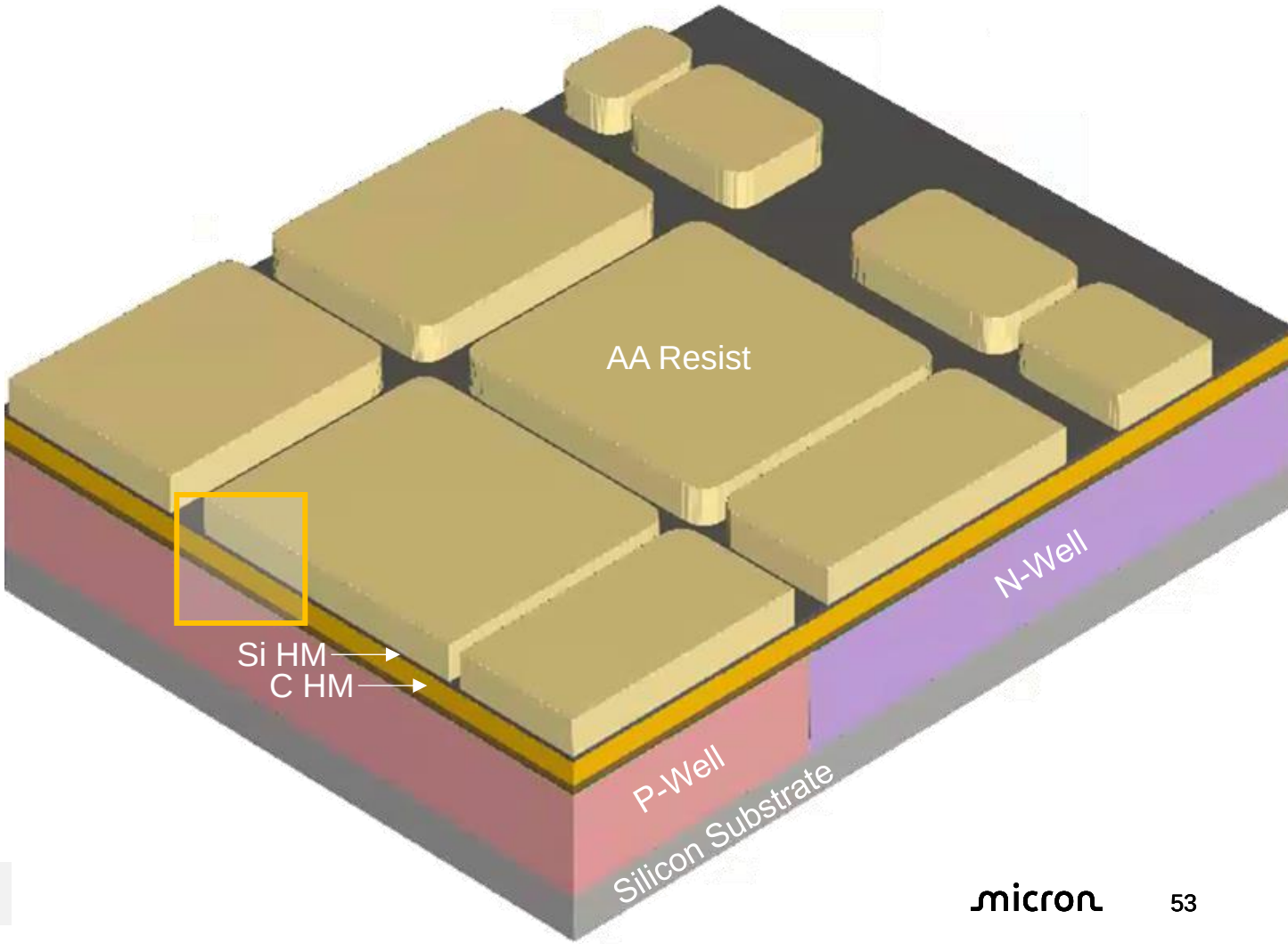
Compare with PVD

AA ACTIVE AREAS PHOTO PATTERN [PHOTO]

In the **Photolithography Area** the “AA” mask is used to define a pattern in photoresist. The pattern defines “active areas” where CMOS devices will be formed. Between the active areas, trenches will be etched into the silicon substrate to provide electrical isolation between devices.

Detail Close-up



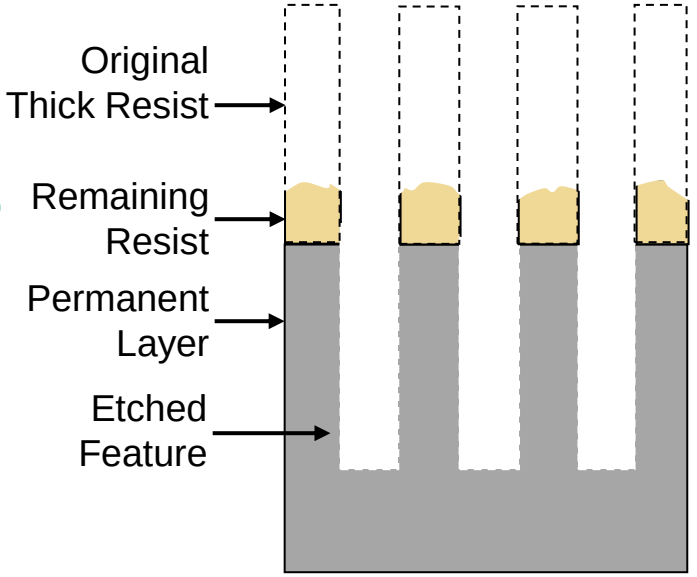


CMOS = Complimentary Metal Oxide Semiconductor Transistor

Why Hardmask?

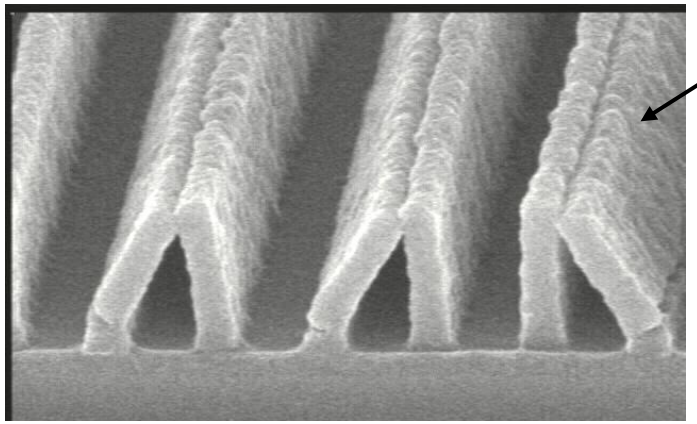
THICK Photoresist: Etch Perspective ☺

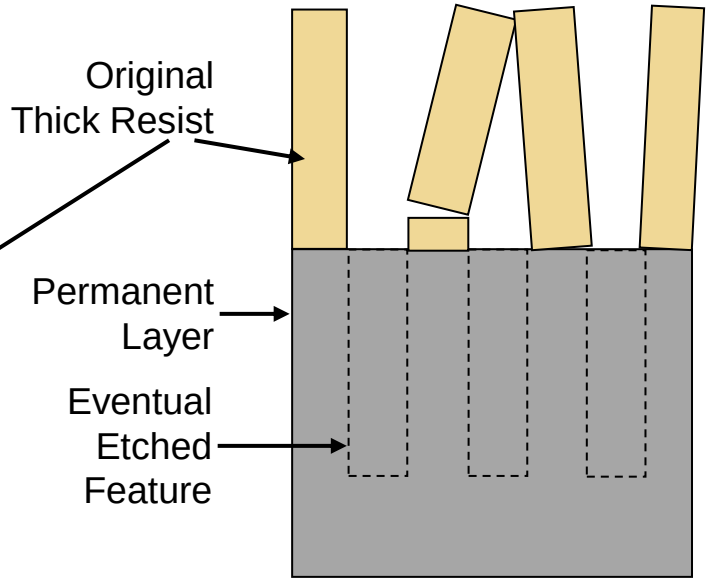
- Necessary to ensure resist is not completely eroded before the etch is complete.



THICK Photoresist: Photo Perspective ☹

- Difficult to achieve adequate Resolution and Depth of Focus.
- Resist Toppling.



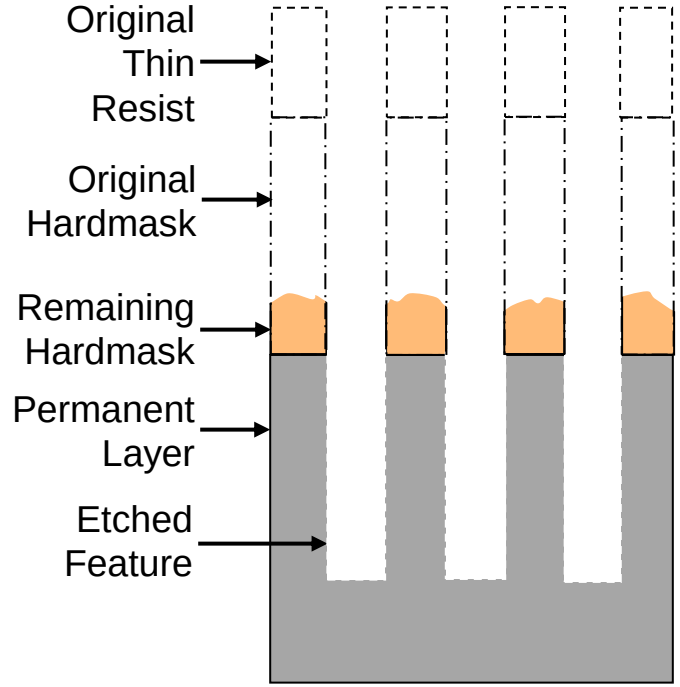


The Hardmask Approach

Photoresist: Photo Perspective ☺

Hardmask: Etch Perspective ☺

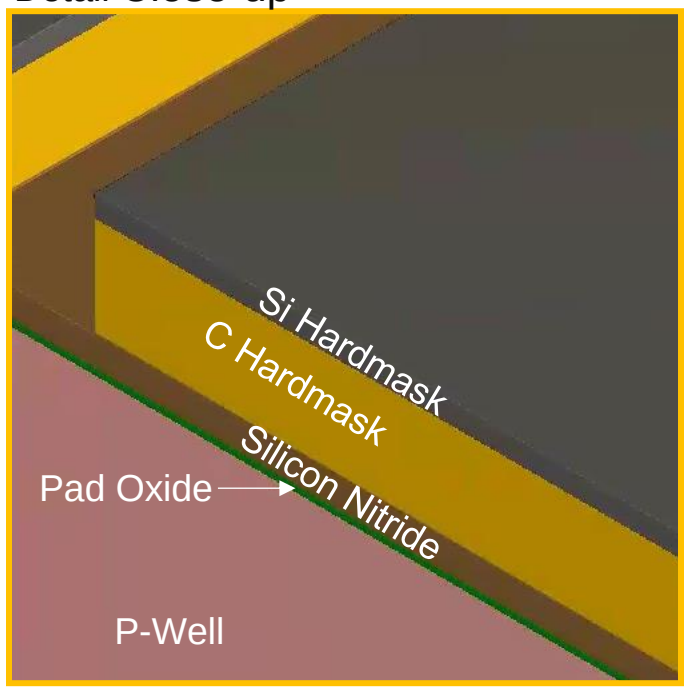
- **Thin** resist for high resolution pattern to transfer into the hardmask
- **Thick** hardmask for erosion resistance to transfer into the permanent layer

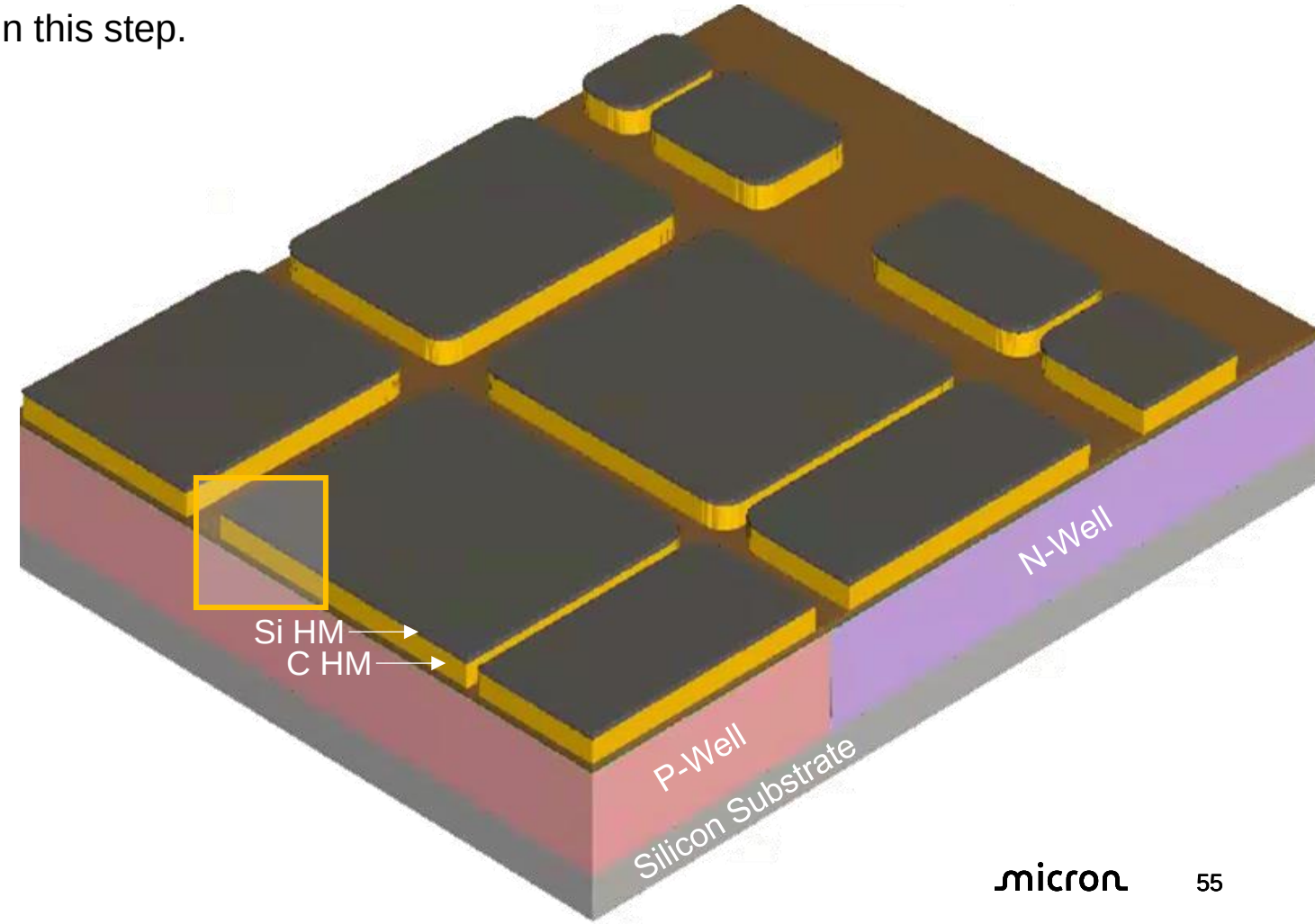


AA HARDMASK DRY ETCH [DRY ETCH]

- In the **Dry Etch Area** a plasma process is used to transfer the AA photoresist pattern into the underlying hardmask layers. The hardmask layers will provide a more robust mask for the subsequent trench etch than photoresist.
- Notes:
  - This step is also known as “Dry Develop”
  - The photoresist is completely etched away in this step.

Detail Close-up

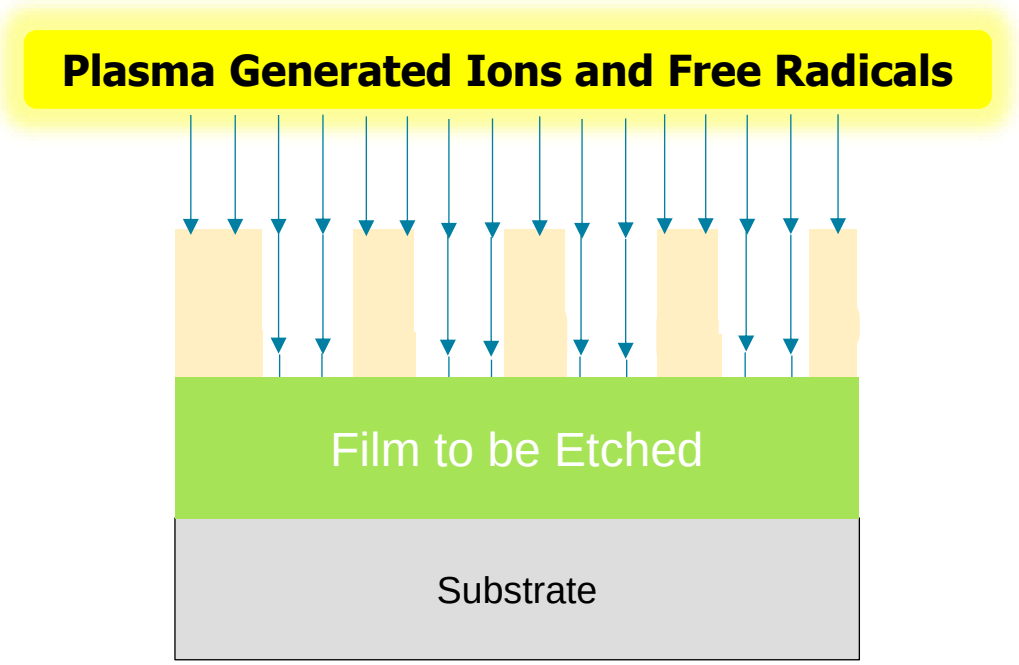


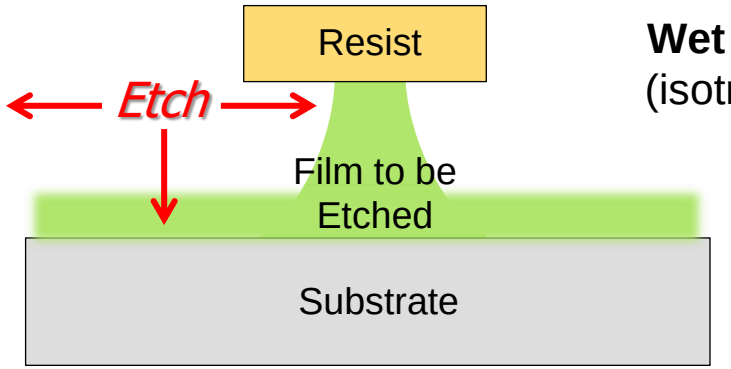


AA = Active Areas

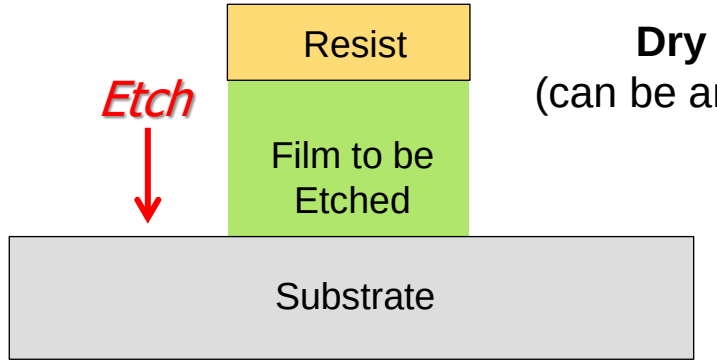
Dry Etch

- The Dry Etch area **removes** (etches) films using plasma (ionized gases). Dry Etch usually processes wafers after a temporary mask has been previously patterned, e.g. photoresist or a hardmask. The mask protects some regions of the wafer. Dry Etch only removes films from the unprotected regions. Very fine and precise patterns can be etched into films.
- Dry etch utilizes plasma technology to permanently transfer a mask pattern into the underlying layer(s).
- Wet processing can also be used for patterning, but wet process is isotropic while dry etching can be vertical (anisotropic). Dry Etch allows for much more accurate and precise feature definition.
- Dry etch can further reduce dimensions through sidewall etching or undercut, resulting in a smaller feature than what only Photo can produce (< 20 nm).





Wet Etch
(isotropic)

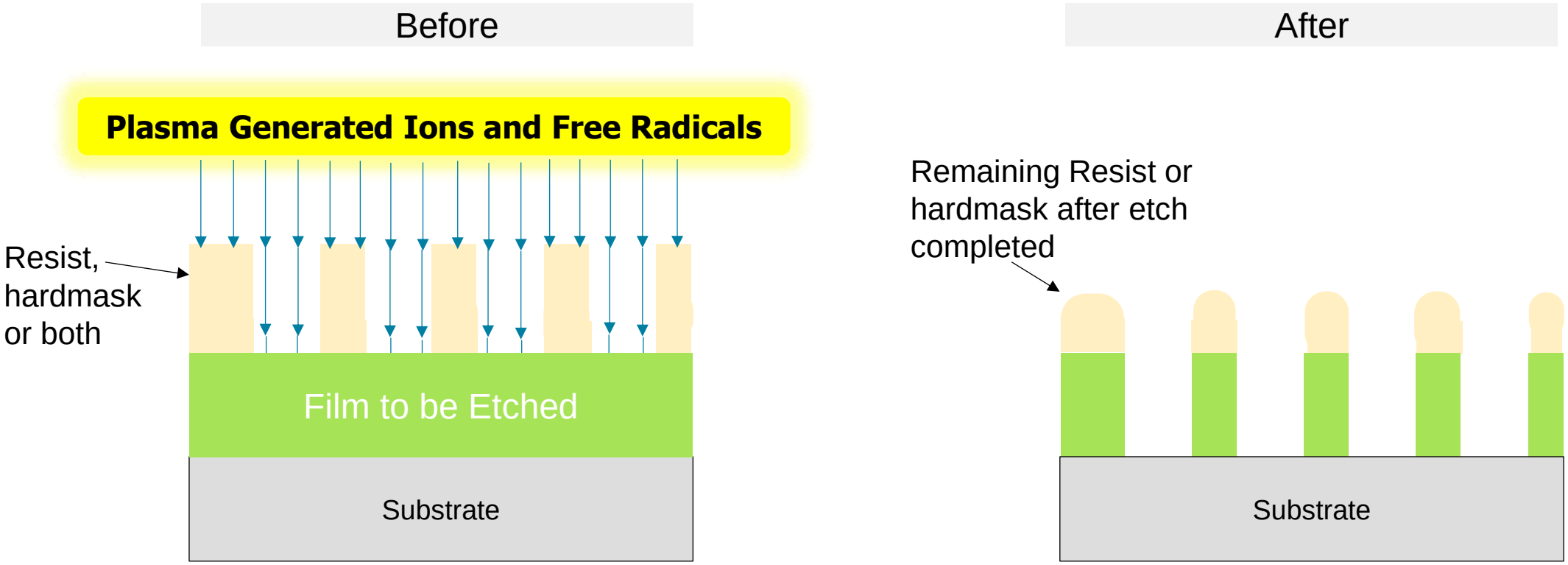


Dry Etch
(can be anisotropic)

Dry Etch

Resist (and hardmask) thickness is engineered so there is still some left after the etch is complete to ensure the film underneath is protected.

The etch step is usually followed by a “strip” step which removes the remaining resist or hardmask.

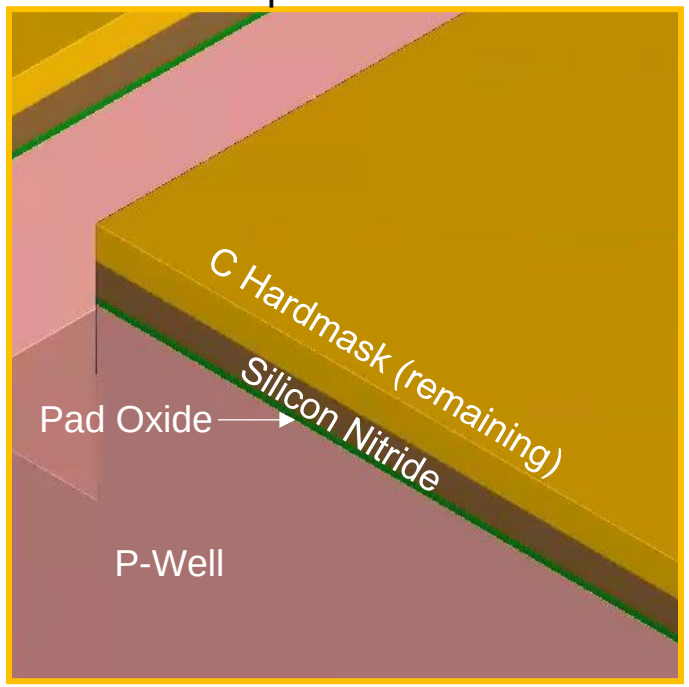


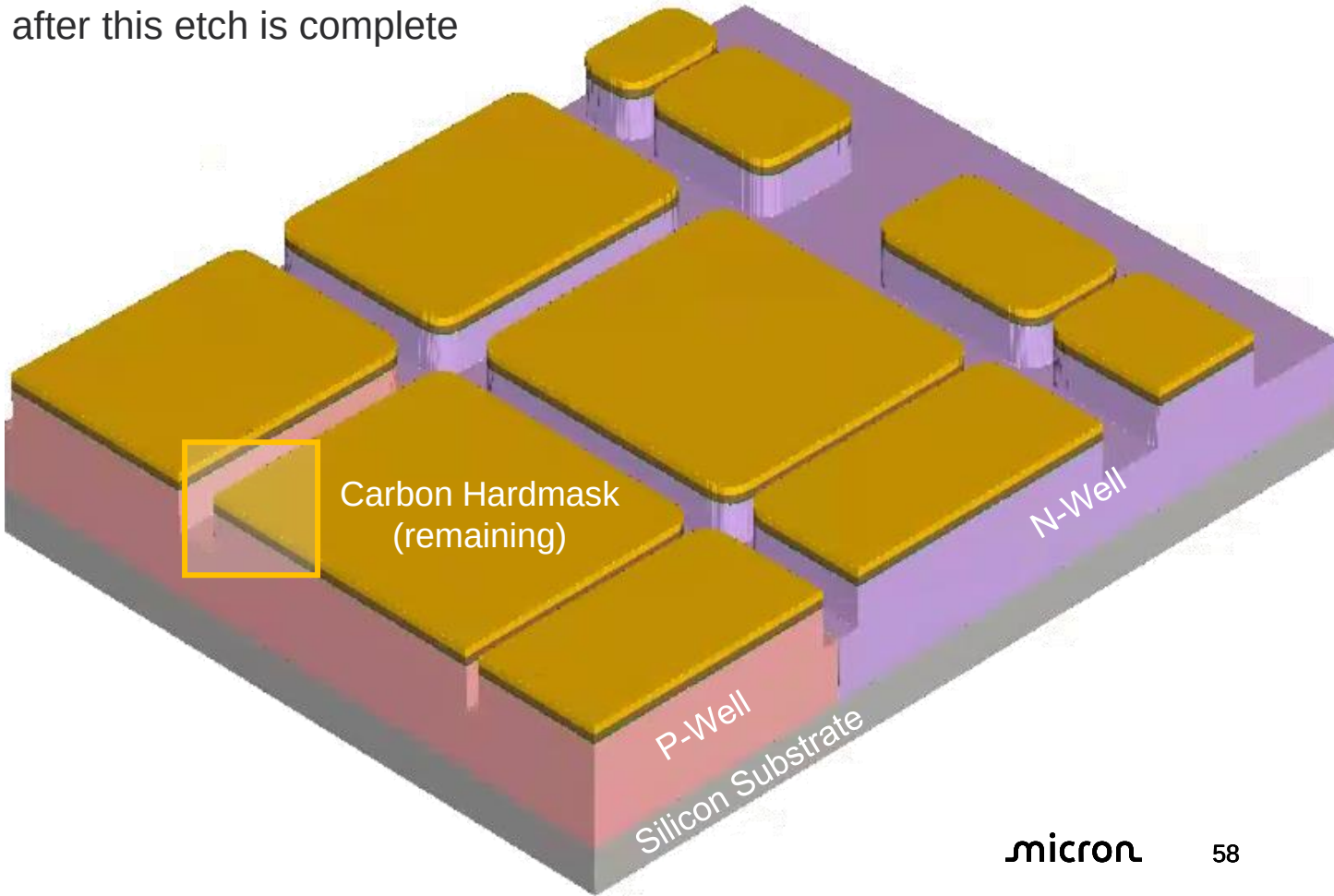
AA STI DRY ETCH [DRY ETCH]

- In the **Dry Etch Area** a second plasma process is used to etch trenches into the silicon wafer. For this process, the mask is the Si hardmask and the carbon hardmask. These trenches will be filled with oxide and will provide electrical isolation between adjacent active areas.
- Notes:
  - STI stands for “Shallow Trench Isolation”
  - Some of the carbon hardmask layer remains after this etch is complete

Q) What do you think is the next Traveler step?

Detail Close-up

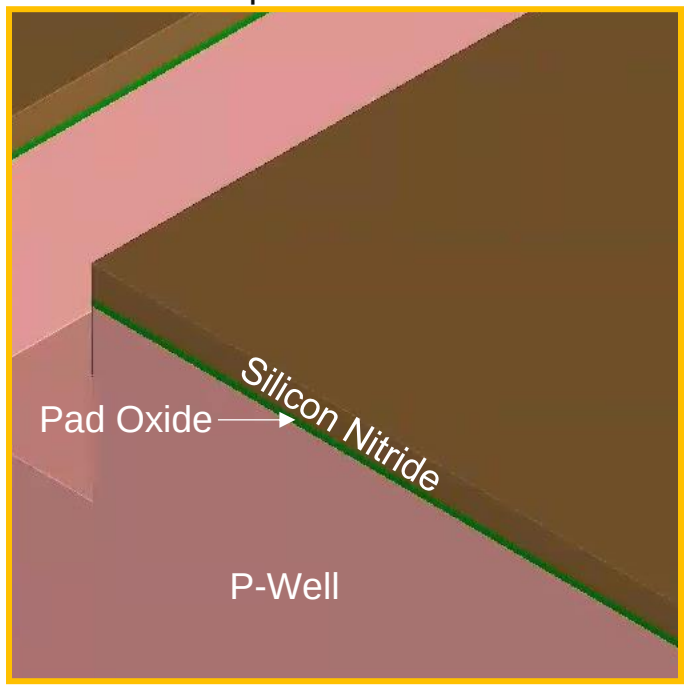


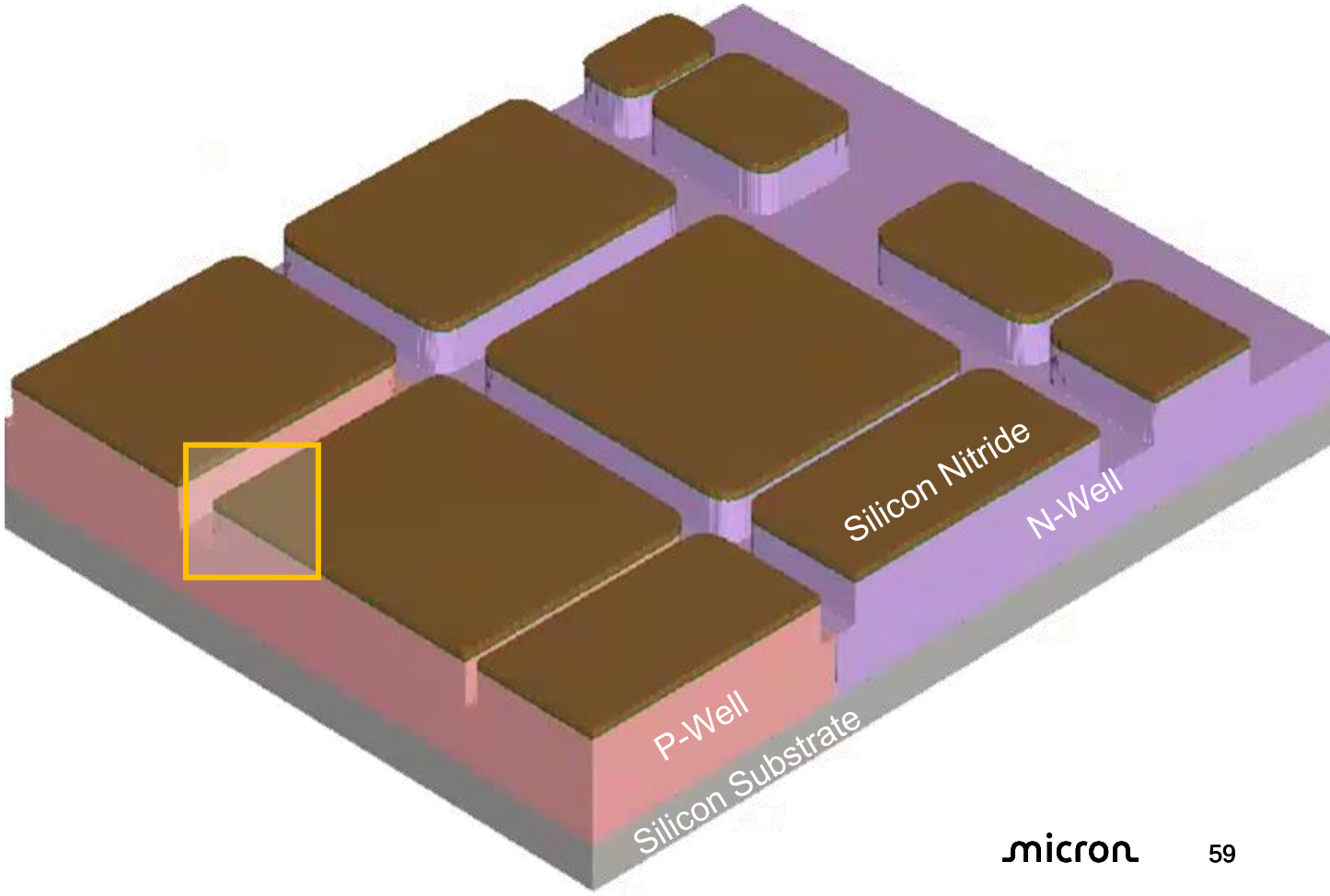


AA RESIST STRIP [WET PROCESS]

- In the **<u>Wet Process Area</u>** plasma and wet chemistry are used to remove the remaining carbon hardmask after the trench etch is complete. (similar recipe used to remove photoresist)
- Metrology:
  - There should be no residual carbon left on the wafer.

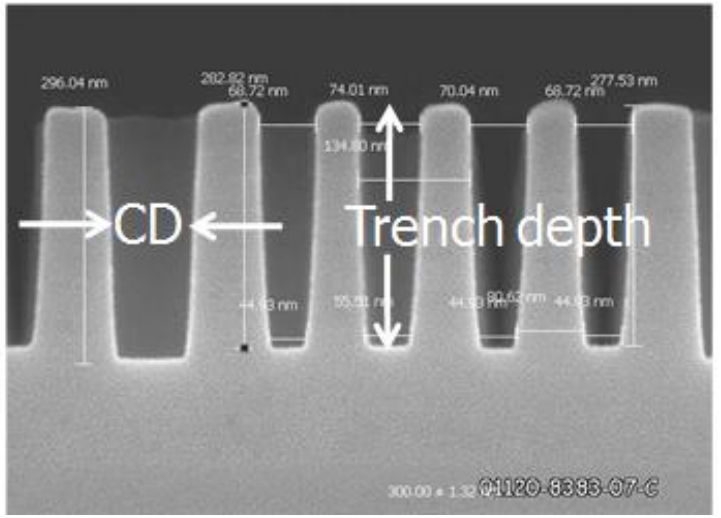
Detail Close-up

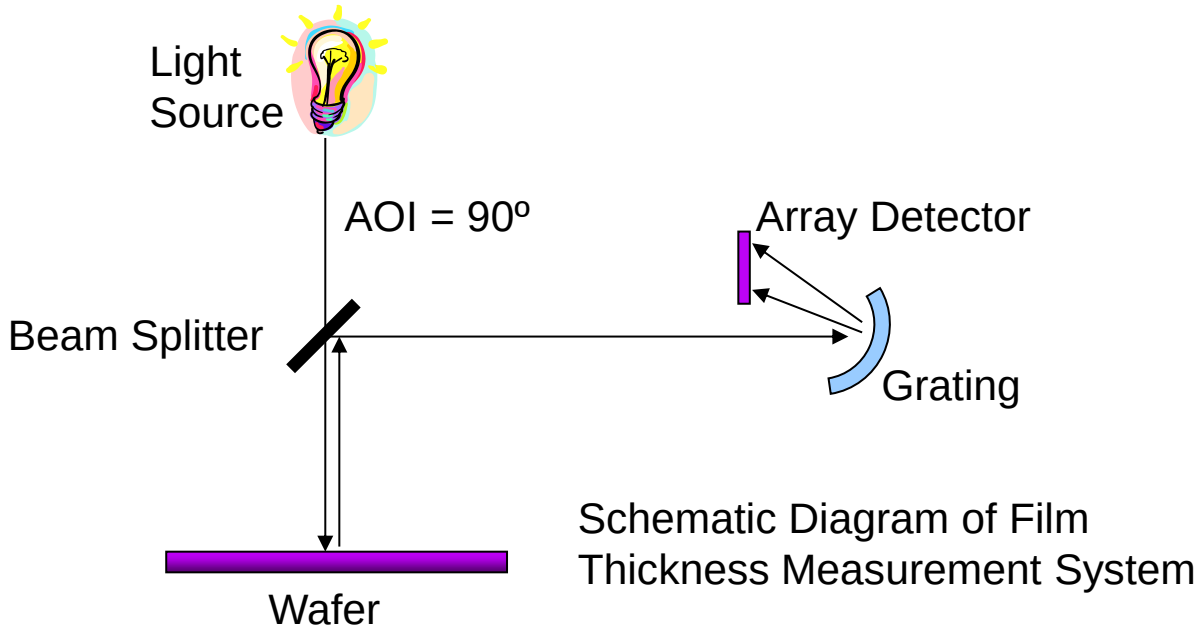




Metrology

- The Metrology area takes measurements that evaluate the results of process operations.
- Examples of measurements are film thicknesses, critical dimensions (CD's), lithography overlay, film resistivity, surface planarity, composition, and stress.
- At right is a cross-section image of a wafer where several critical dimensions (CDs) were taken using a scanning electron microscope (SEM).
- Below is a schematic diagram of a system used to measure the thickness of very thin films. This technique uses the principle of optical interference.



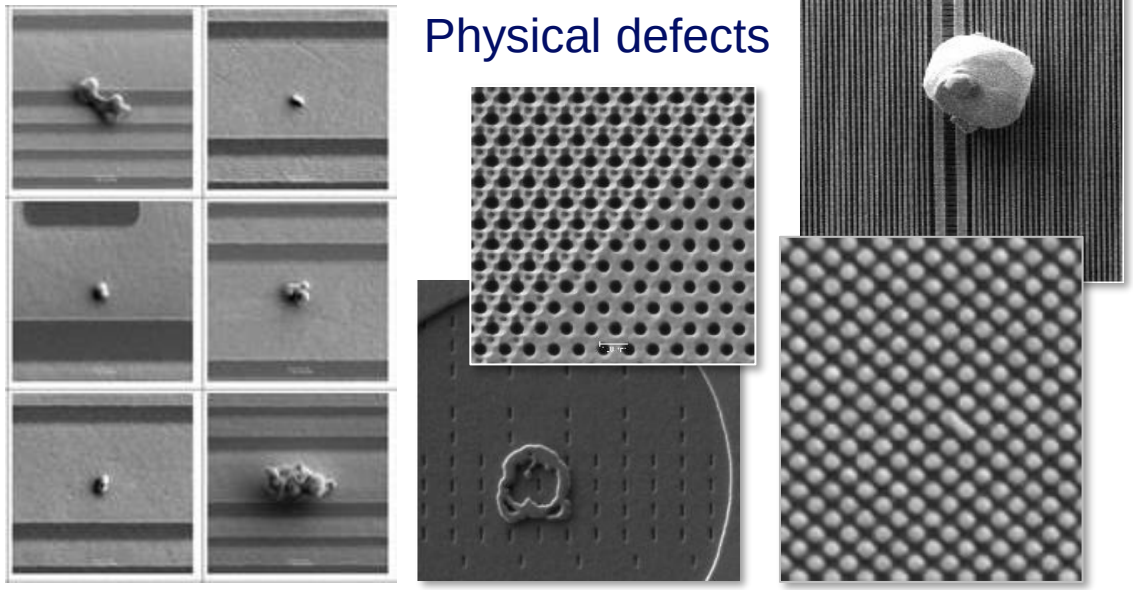


Schematic Diagram of Film Thickness Measurement System

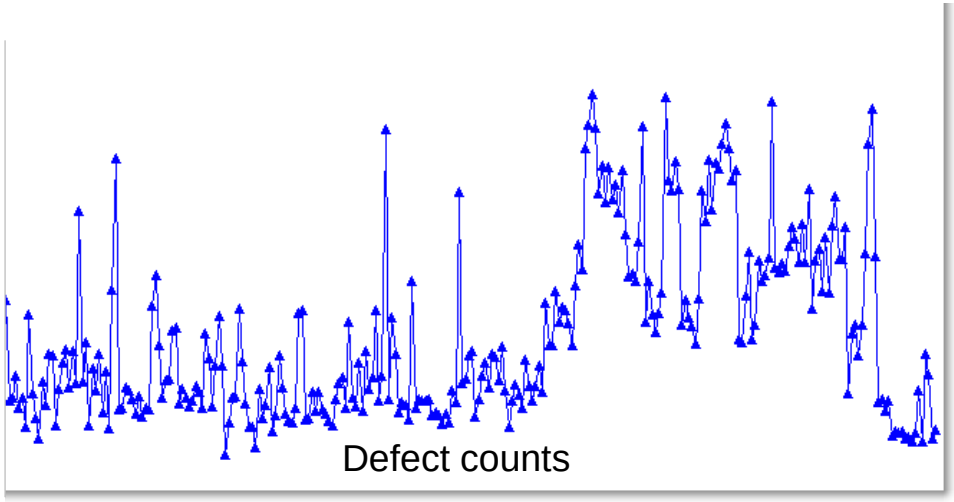
Real-Time Defect Analysis (RDA)

- The Real-Time Defect Analysis (RDA) area inspects wafers for defects at critical points in the manufacturing process.
- The RDA area monitors in-line wafers and provides critical data collection and analysis services to fab process areas
- The process areas use the information that RDA provides to reduce defectivity on the wafers

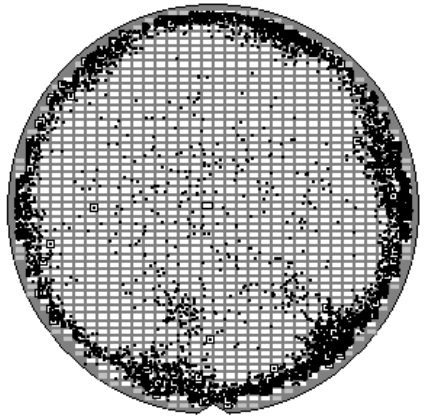
Metrology & RDA do not alter the structural or electrical characteristics. However, for processing wafers from start to finish they are our eyes to what is happening on the wafers. The information they provide is critical for design, layout, reticle, process and equipment improvements to maximize yield, quality, and performance.



Physical defects



Defect Wafer Maps



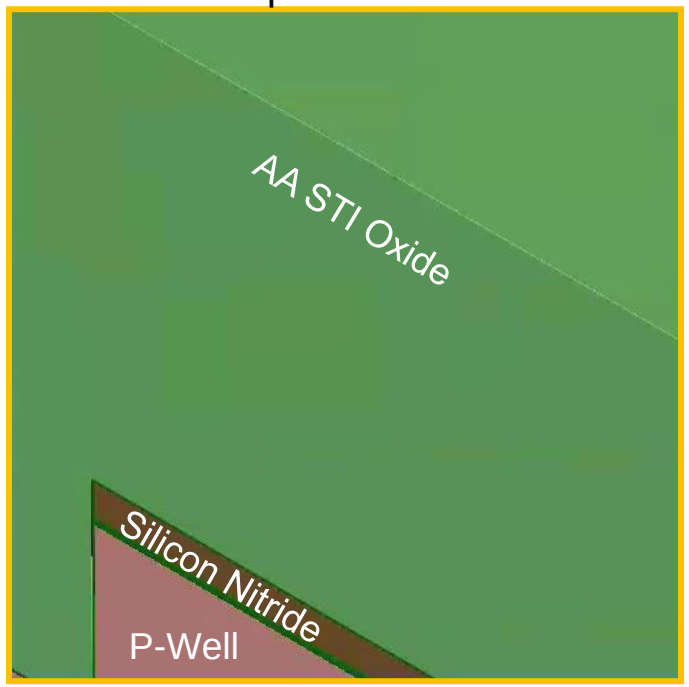
Edge ring shading

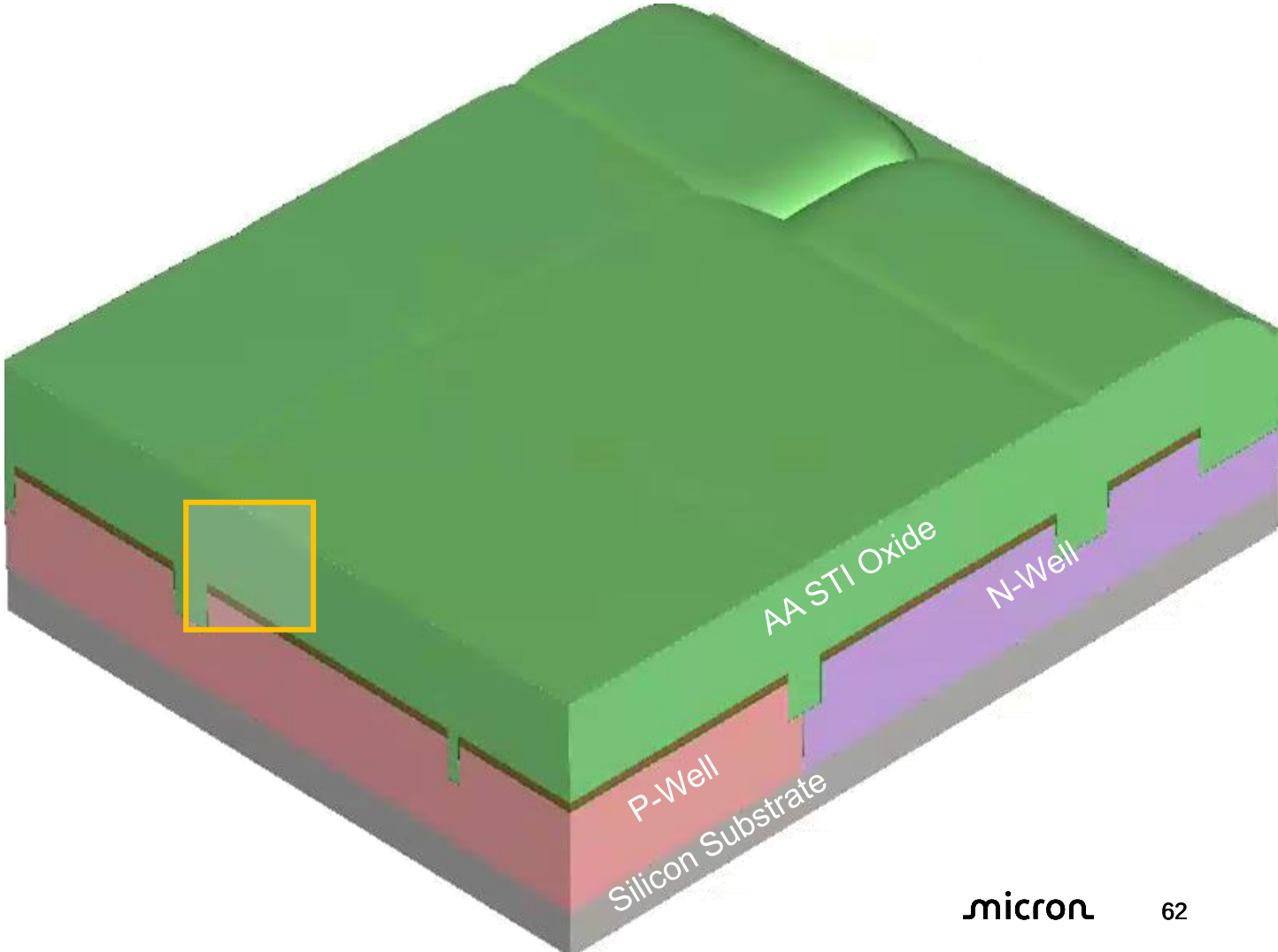
AA STI OXIDE DEPOSIT [CVD]

- In the **CVD Area** a thick film of silicon dioxide is deposited to fill the trenches. Only the oxide in the trenches is needed, so the unwanted surface oxide will be removed in the next Traveler step.

Q) What do you think is the next Traveler step?

Detail Close-up



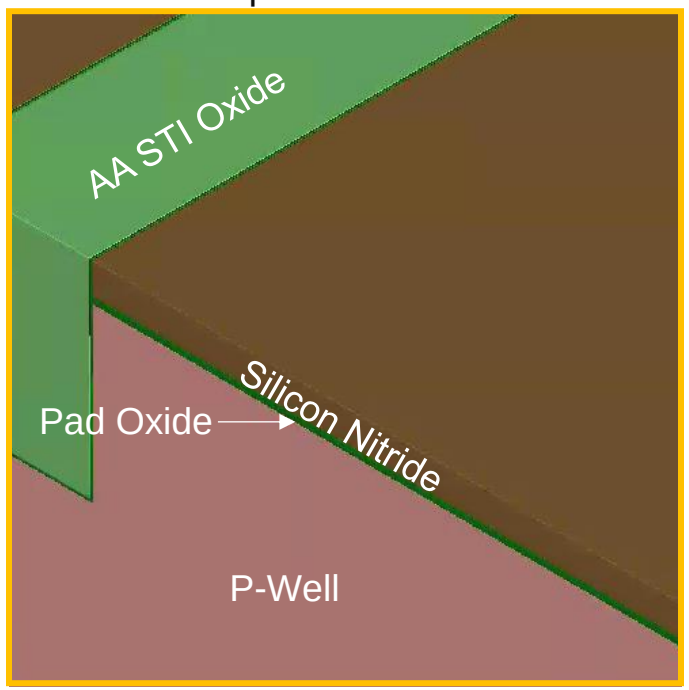


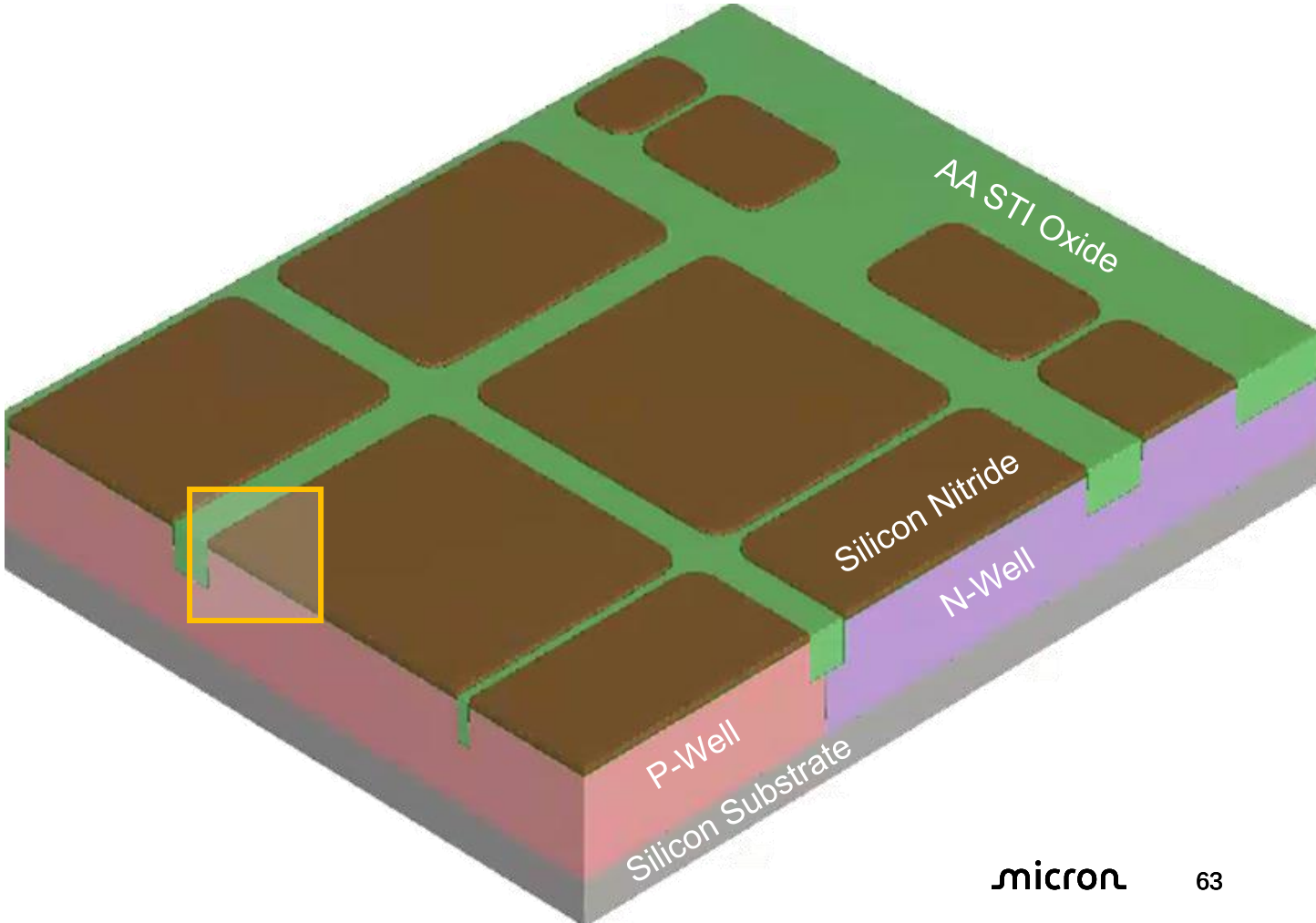
CVD - Chemical Vapor Deposition

AA STI OXIDE CMP [CHEMICAL MECHANICAL PLANARIZATION]

- In the **CMP Area** a polishing process is used to remove the unwanted oxide on the surface, leaving the trenches filled with oxide.
- Note: The silicon nitride film, deposited near the beginning of the flow, effectively stops the CMP process. This process is referred to as a “Stop on Nitride (SON)” process.

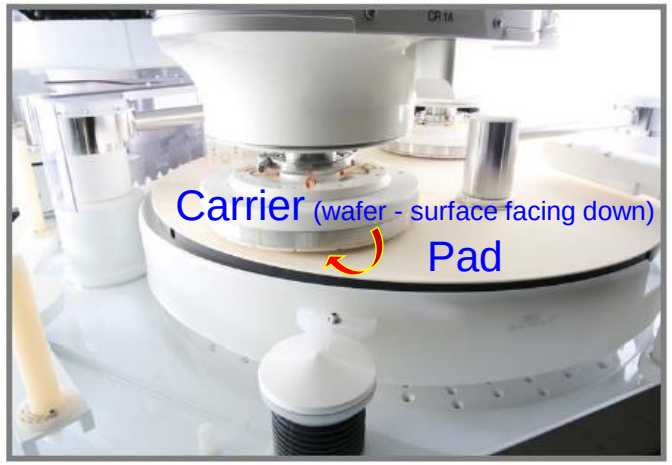
Detail Close-up



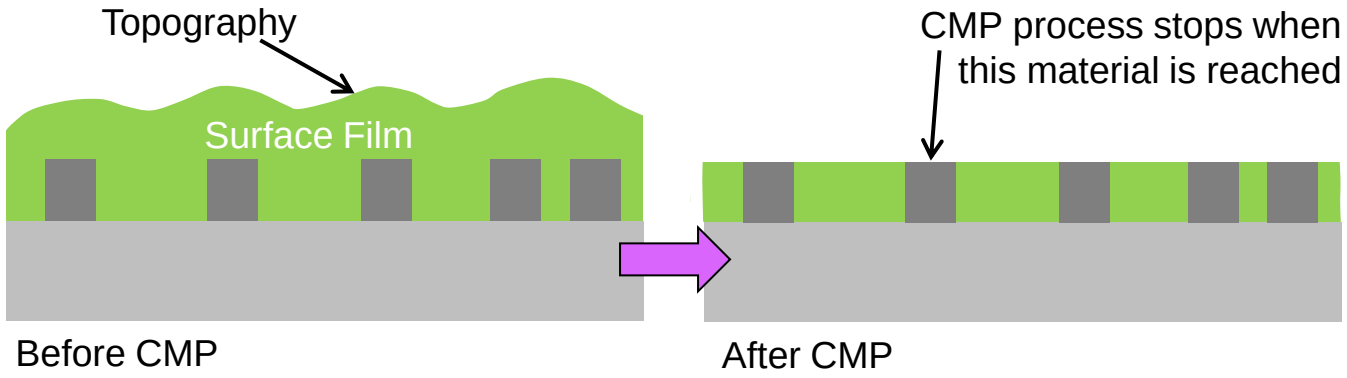


Chemical Mechanical Planarization (CMP)

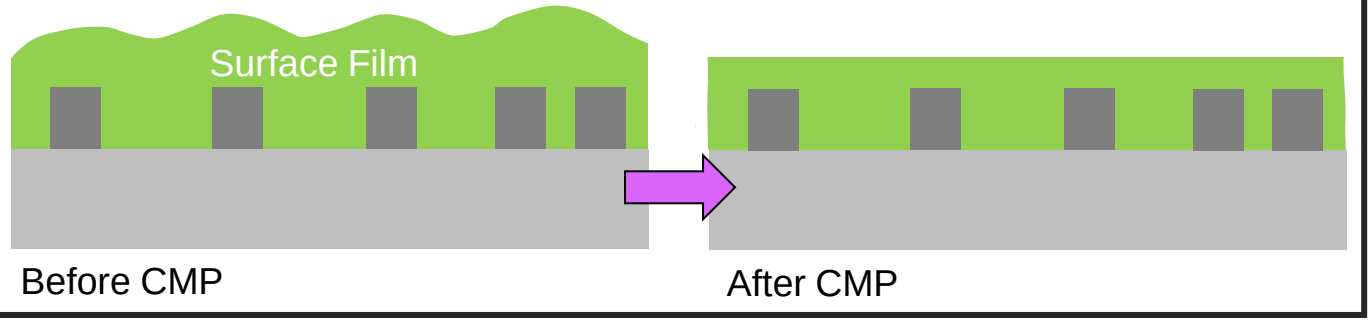
- CMP is used to reduce or eliminate topography on the wafer surface. A planar surface is necessary for photo to print patterns at very small feature sizes.
- CMP is also used to remove excess surface films after they have been deposited.
- CMP uses a polishing pad, and a chemical slurry made of fine abrasive particles suspended in a dilute chemical solution to perform the polishing process.
- Like wet etch and dry etch, CMP can selectively polish some films while leaving others untouched.



CMP "**Stop on Film**" process: on-tool sensors allows this process to detect the different hardness or optical properties of materials



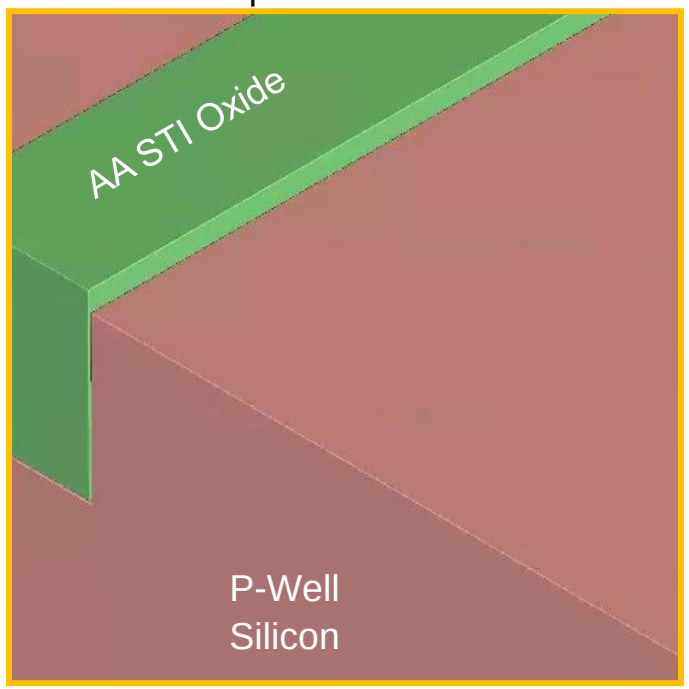
CMP "**Stop in Film**" process: this is a timed process

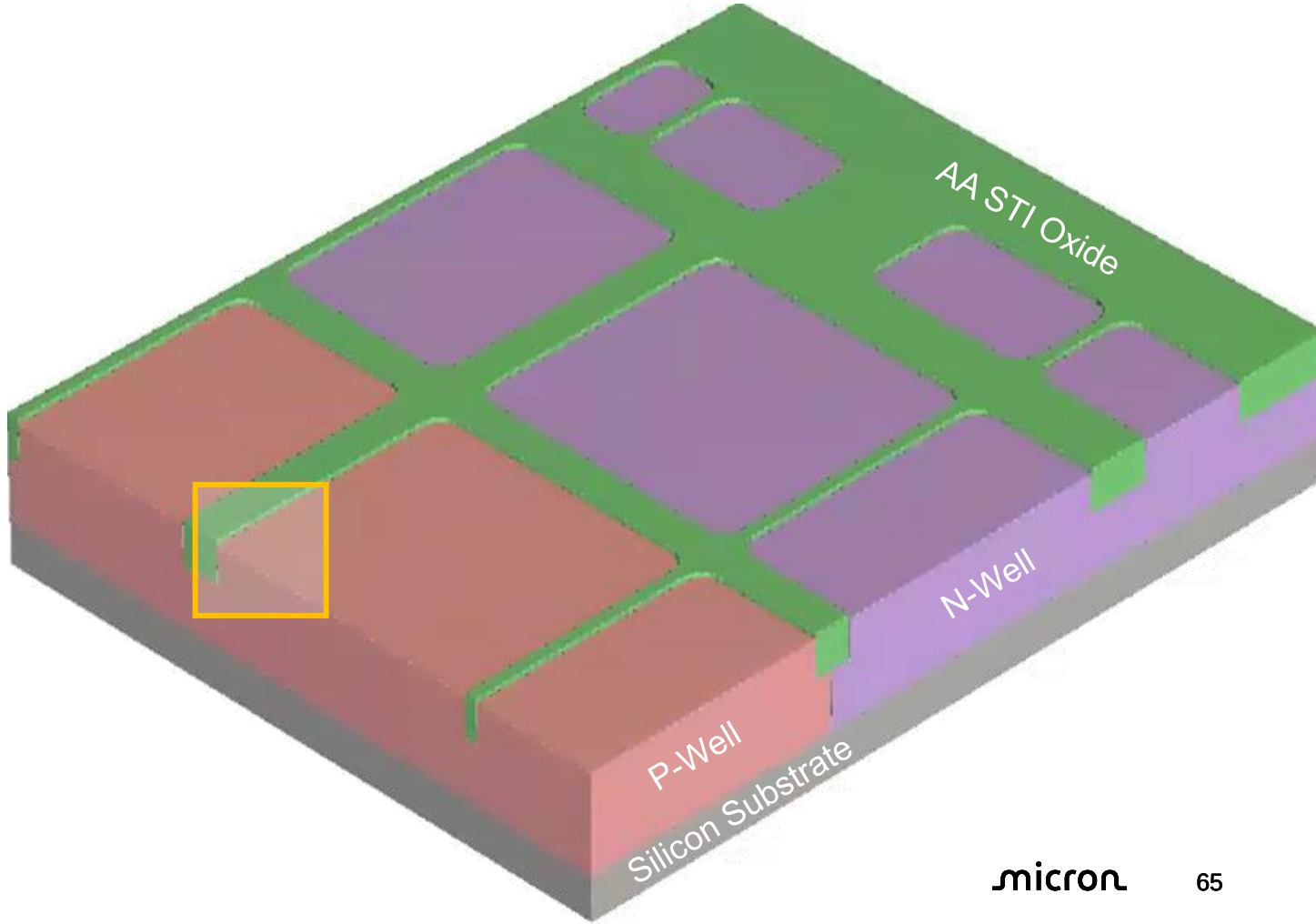


AA STI NITRIDE WET ETCH [WET PROCESS]

- The nitride film is no longer needed, so in the Wet Process Area wet chemicals are used to completely remove the nitride with minimal impact to the exposed oxide or silicon layers.
- A second wet chemical process removes the original Pad Oxide, exposing bare silicon.

Detail Close-up

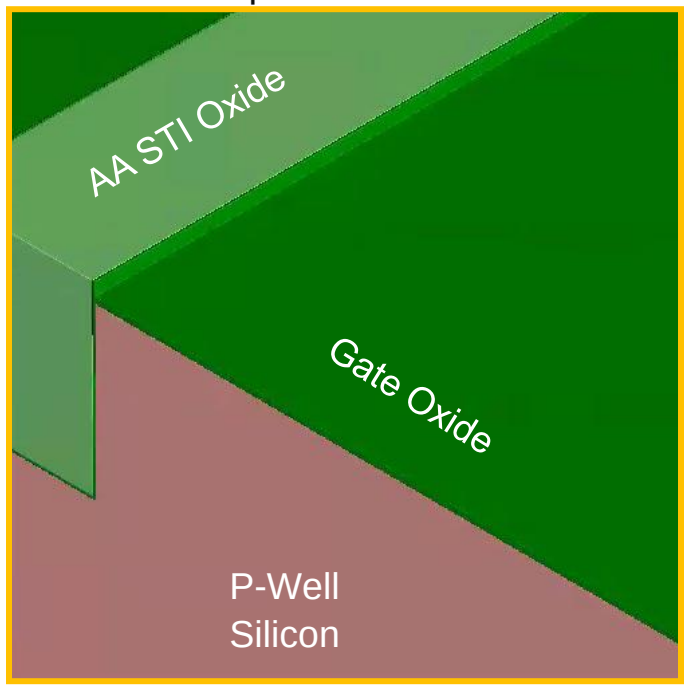


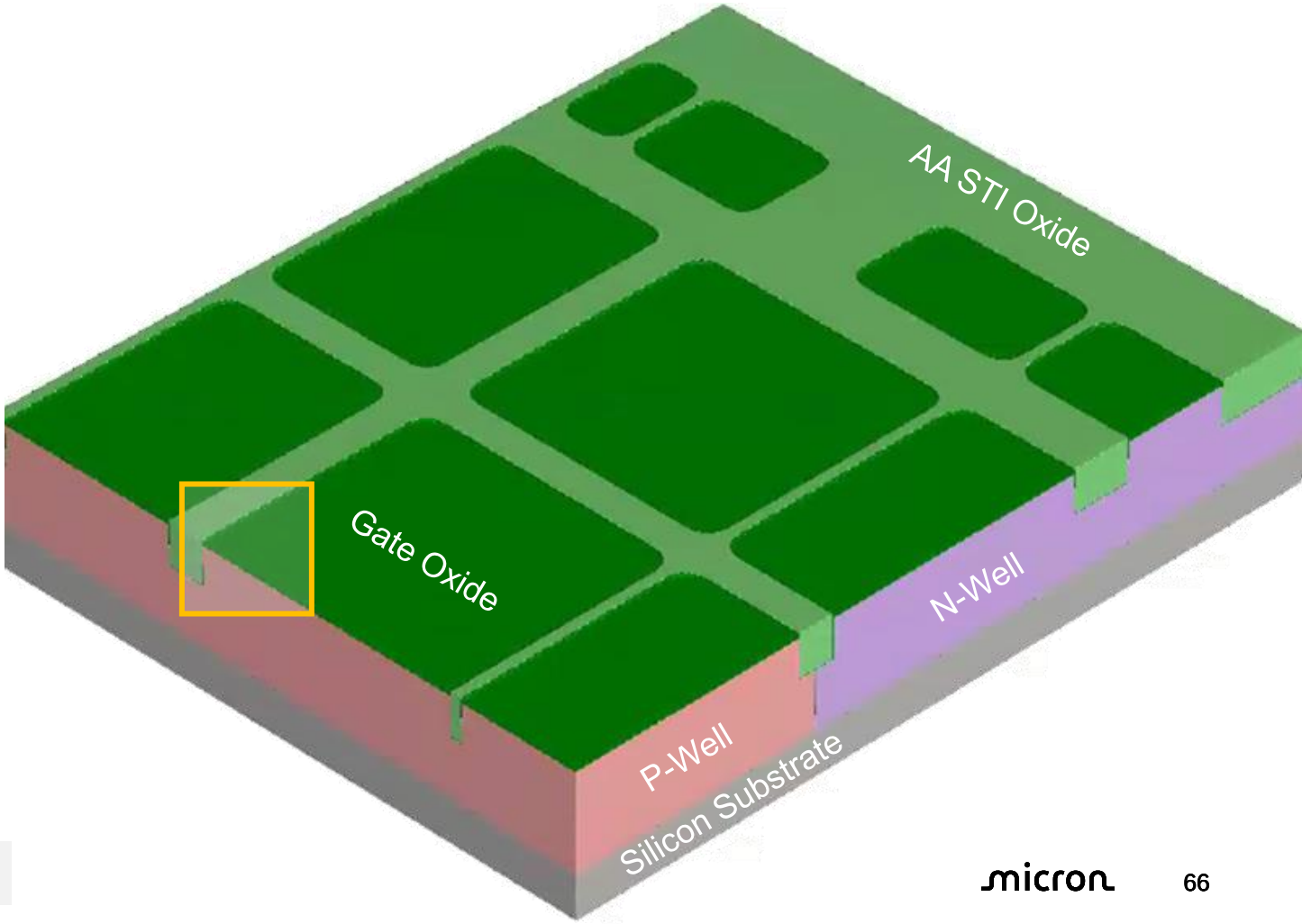


TG GATE OXIDE GROWTH [DIFFUSION]

- In the **Diffusion Area** a thin film of high-quality silicon dioxide is grown on the surface of the silicon wafer. This oxide will be an important part of the gates of the CMOS transistors: the gate oxide.

Detail Close-up



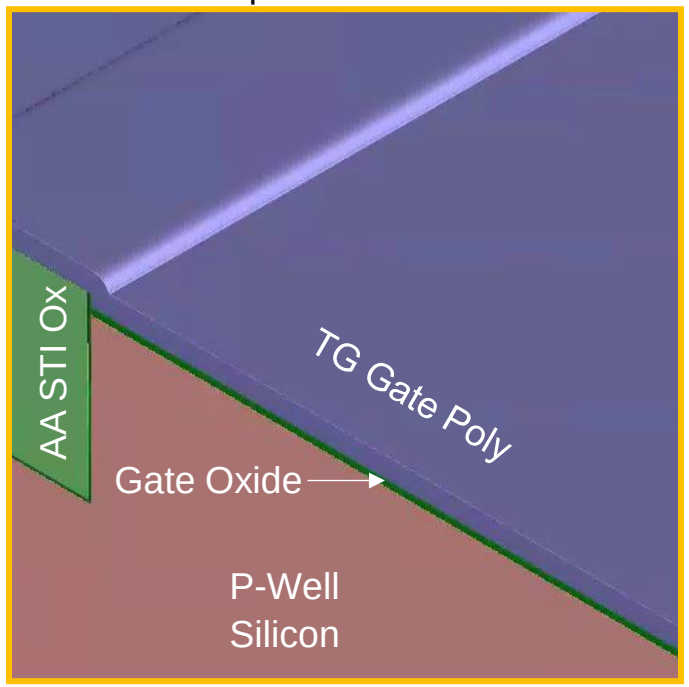


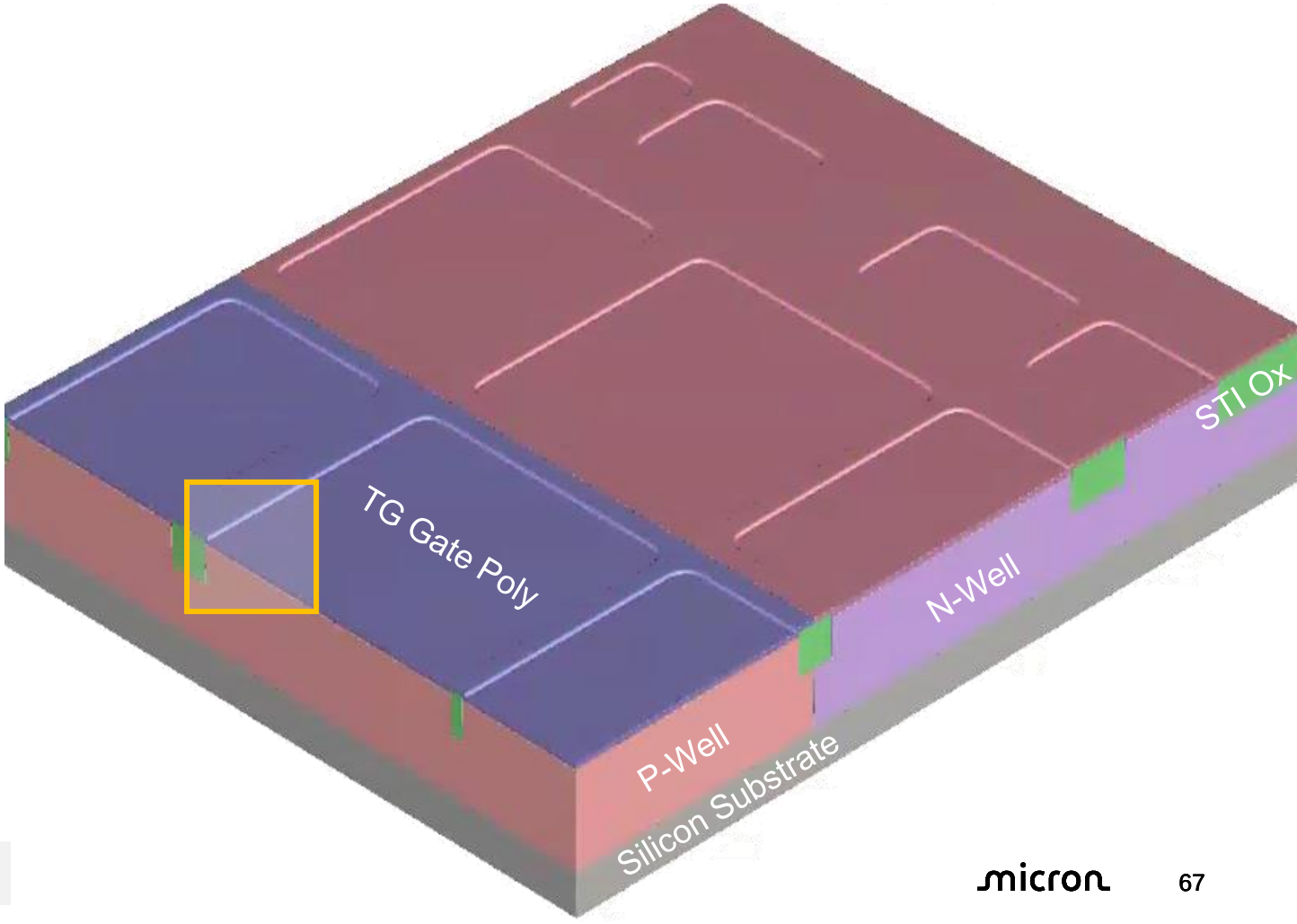
CMOS = Complimentary Metal Oxide Semiconductor Transistor

TG GATE POLYSILICON DEPOSITION [DIFFUSION]

- In the **Diffusion Area** a polycrystalline silicon film (known as “poly”) is deposited on top of the gate oxide. The poly will be the electrodes of the transistor gates.
- Note: The poly is doped N-type or P-type, shown as purple (N-type) or pink (P-type) in the diagram, as needed for optimal performance of the CMOS devices. The doping will be accomplished by a series of implants (not described in this document).

Detail Close-up





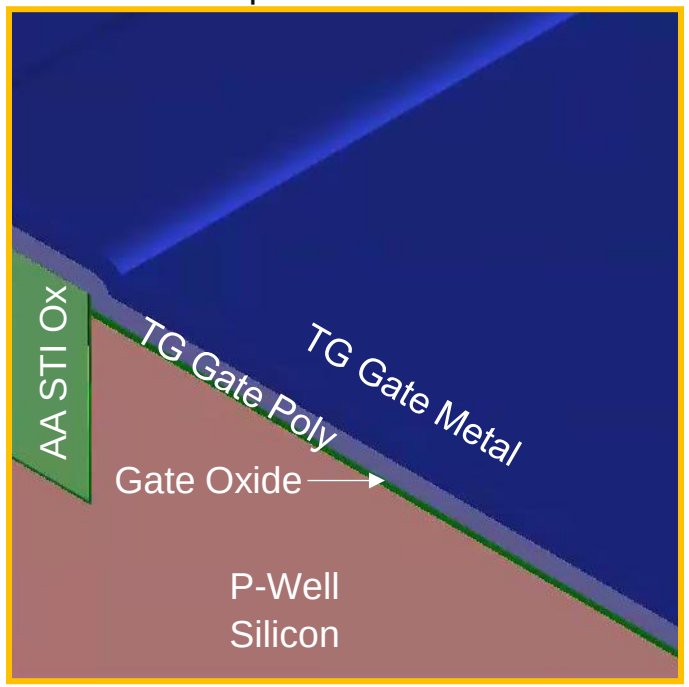
CMOS = Complimentary Metal Oxide Semiconductor Transistor

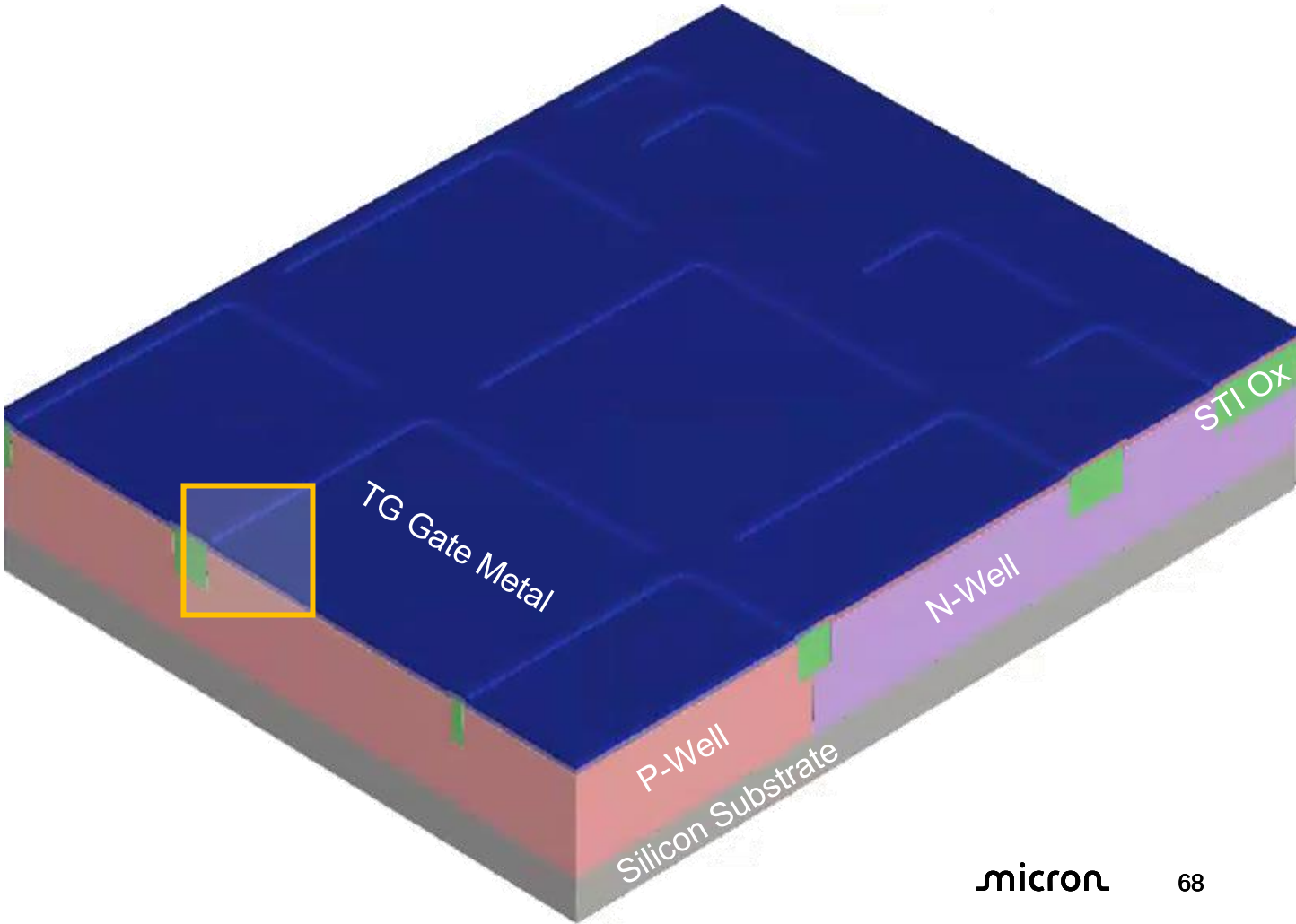
TG GATE METAL DEPOSIT [PHYSICAL VAPOR DEPOSITION (PVD)]

- In the **PVD Area** a metal film is deposited on top of the polysilicon film. This will form the conductive part of the transistor gates.

Note: Several different types of metals may be used for this step

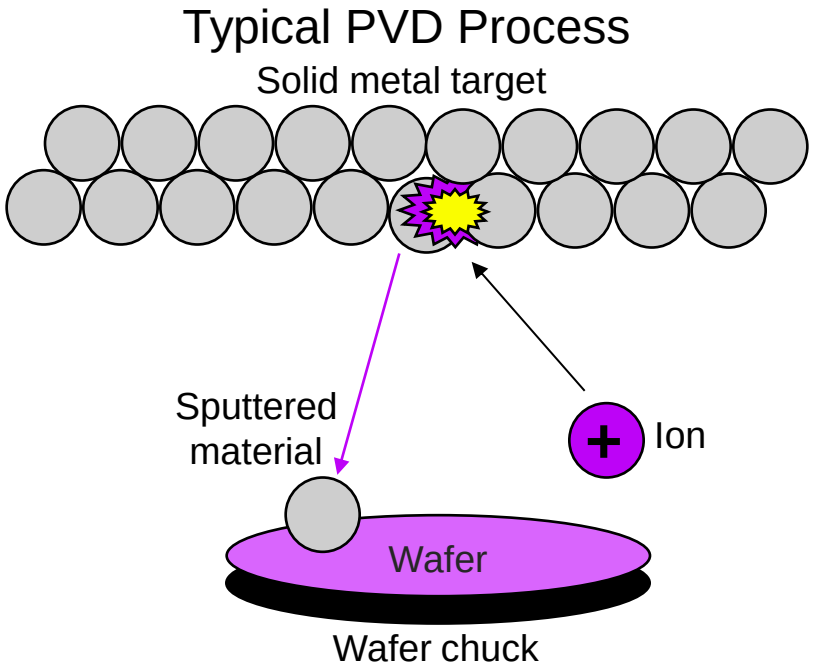
Detail Close-up

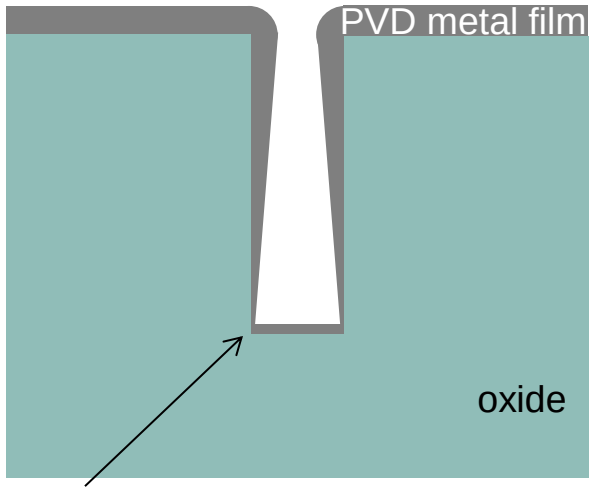




Physical Vapor Deposition (PVD)

- Many of the metal films in the process are deposited using Physical Vapor Deposition (PVD) technology (also known as “sputtering”).
- Ions bombard a metal target. The sputtered metal deposits on the wafer.
- The process involves little or no chemistry and takes place at low (or room) temperature.
- PVD deposits a wide variety of metal films quickly and at relatively low cost.
- PVD films do not deposit as conformally as CVD films, so they cannot be used to fill deep contacts or trenches.





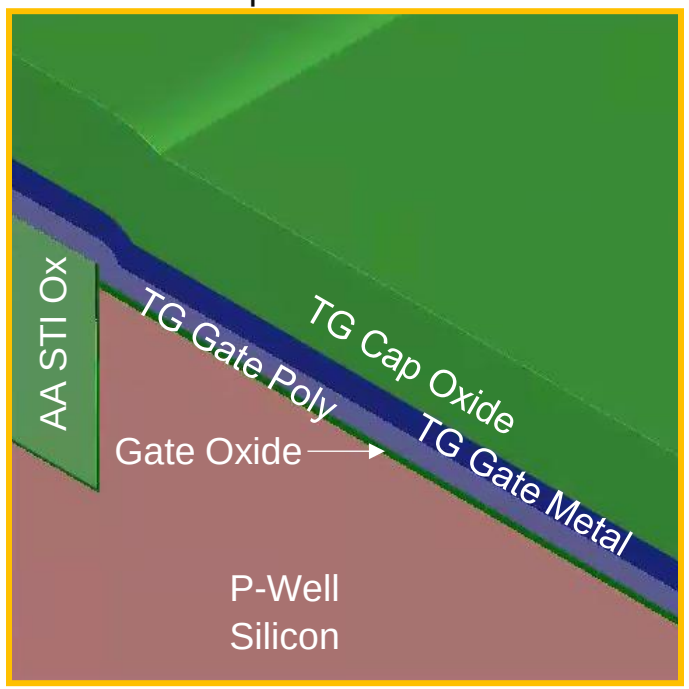
PVD Metal Thinning at the Bottom of a Deep Contact

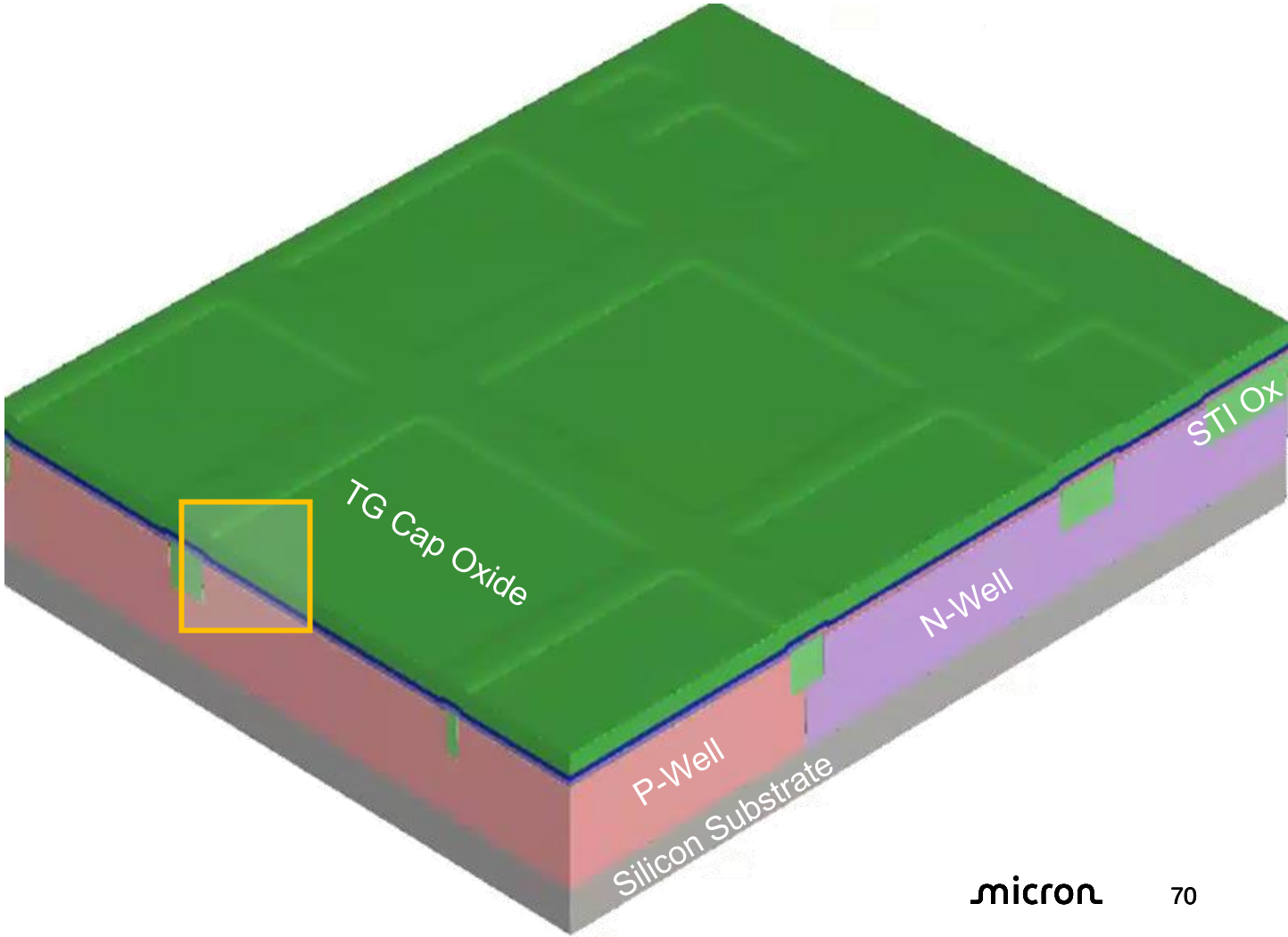
Compare with CVD

TG CAP OXIDE DEPOSIT [CVD]

- In the **CVD Area** a thick film of silicon dioxide is deposited to protect the gate metal layer from corrosion and damage. This film is called Cap Oxide in this case.
- Note: Some technologies use silicon nitride for this purpose.

Detail Close-up





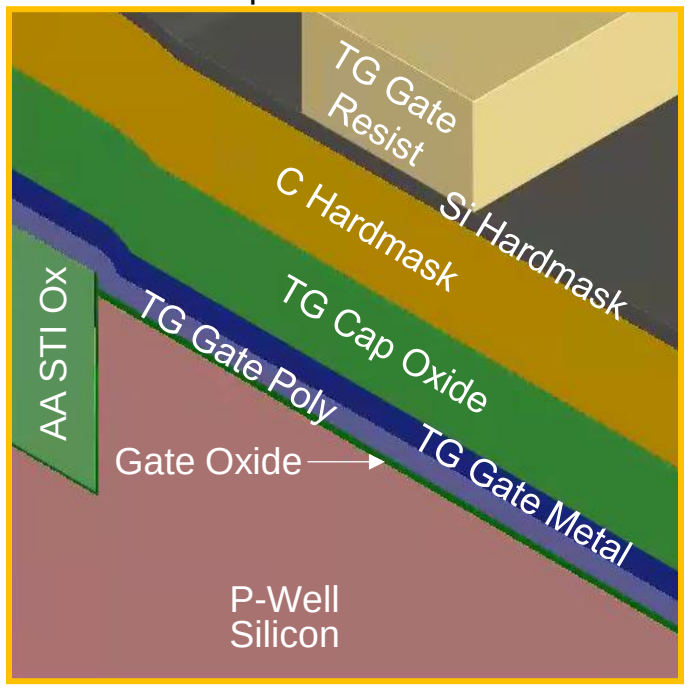
TG HARDMASK LAYERS DEPOSIT

- Deposit hardmask layers for patterning the transistor gates.

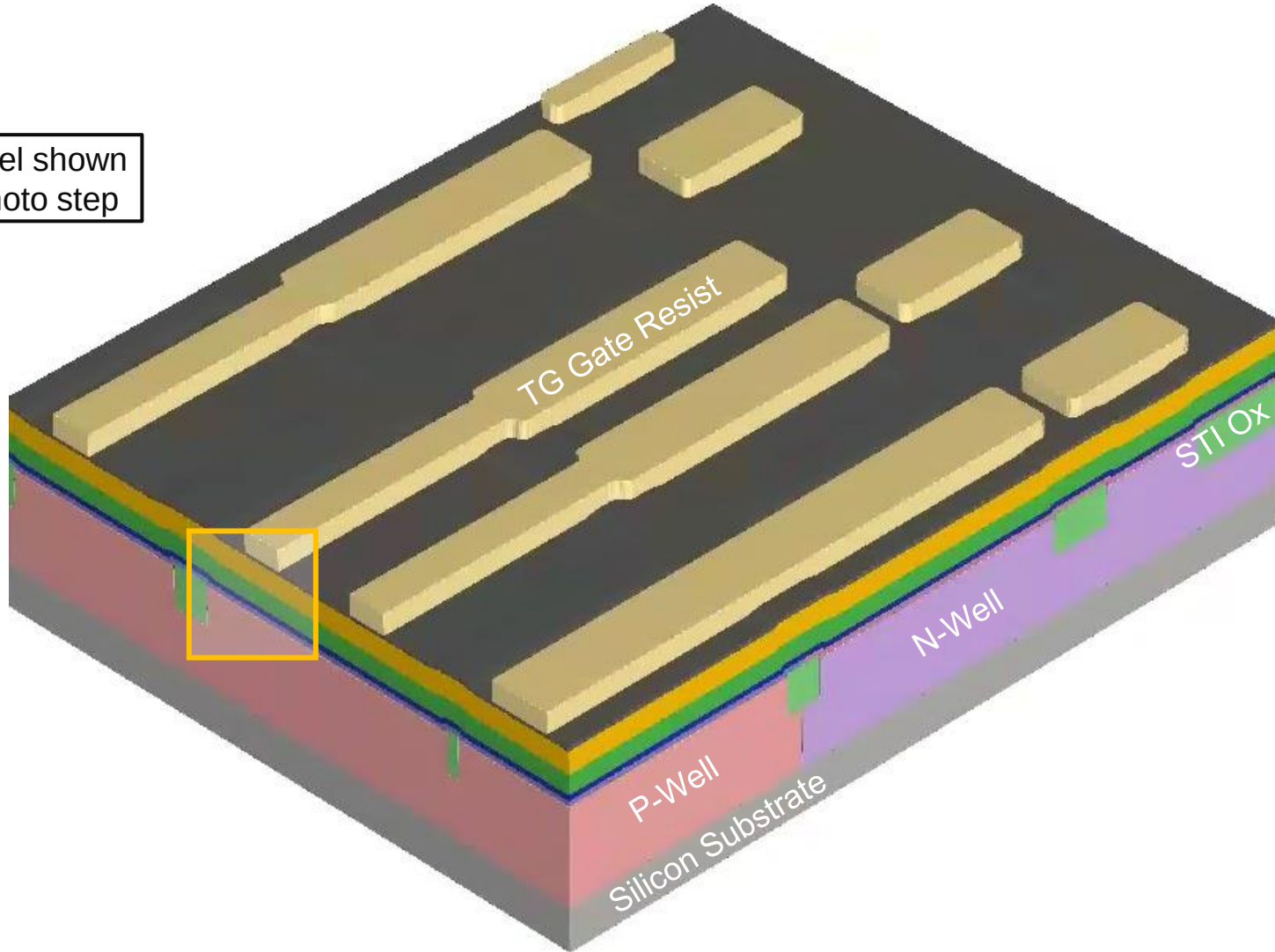
TG GATE PHOTO PATTERN

- The “TG” mask is used to define the pattern in photoresist for the gates of the CMOS devices. The pattern also electrically connects the transistor gates to each other.

Detail Close-up



3D model shown after photo step



TG = Transistor Gates

TG HARDMASK DRY ETCH

- A plasma process is used to transfer the TG photoresist pattern into the underlying hardmask layers.

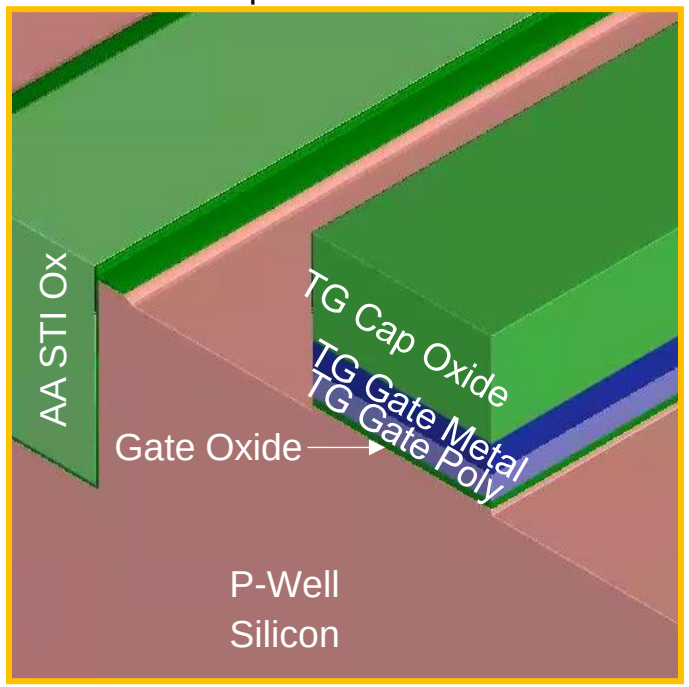
TG GATE DRY ETCH

- A second plasma process is used to etch away the unwanted gate stack layers, leaving behind the gates.

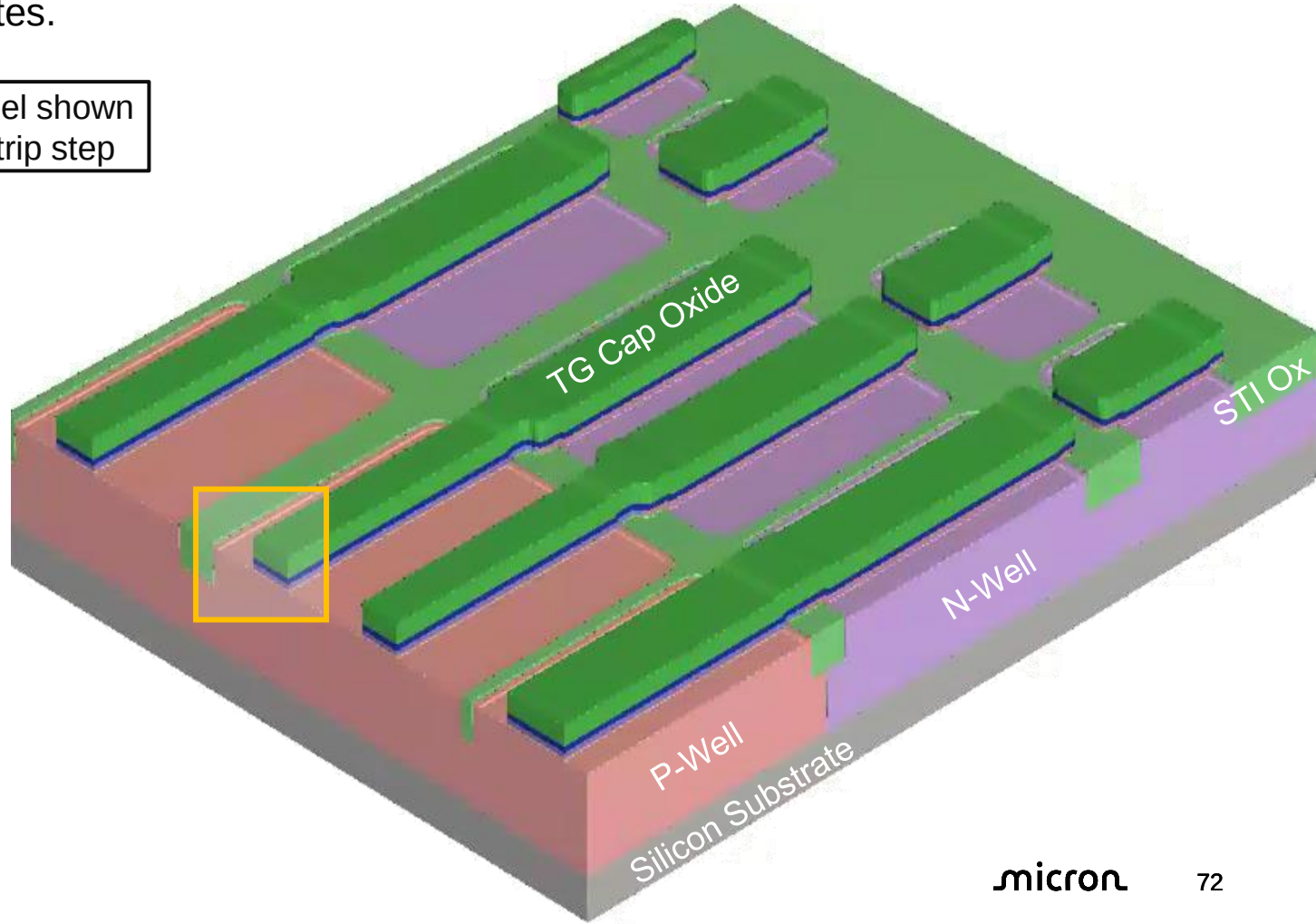
TG RESIST STRIP [WET PROCESS]

- Plasma and wet chemistry are used to remove the remaining carbon after the gate etch is complete.
- 3D model shows the structures after this step

Detail Close-up



3D model shown after strip step

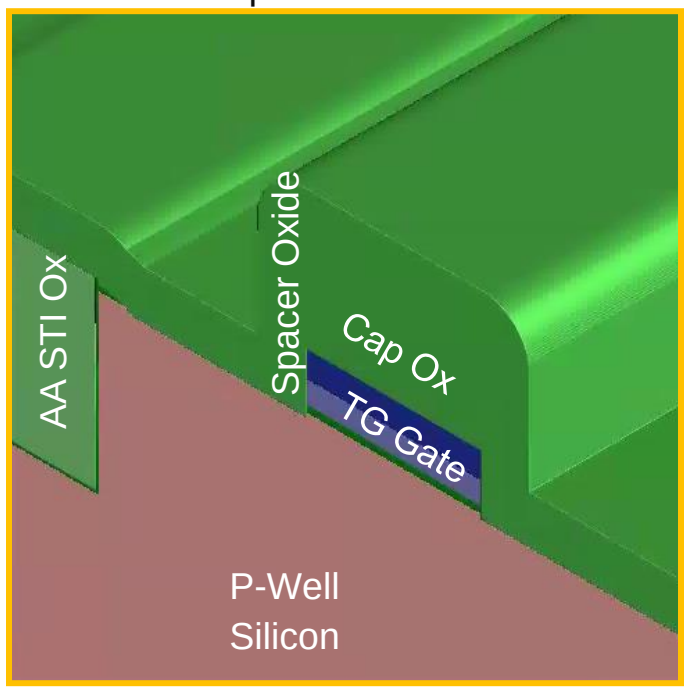


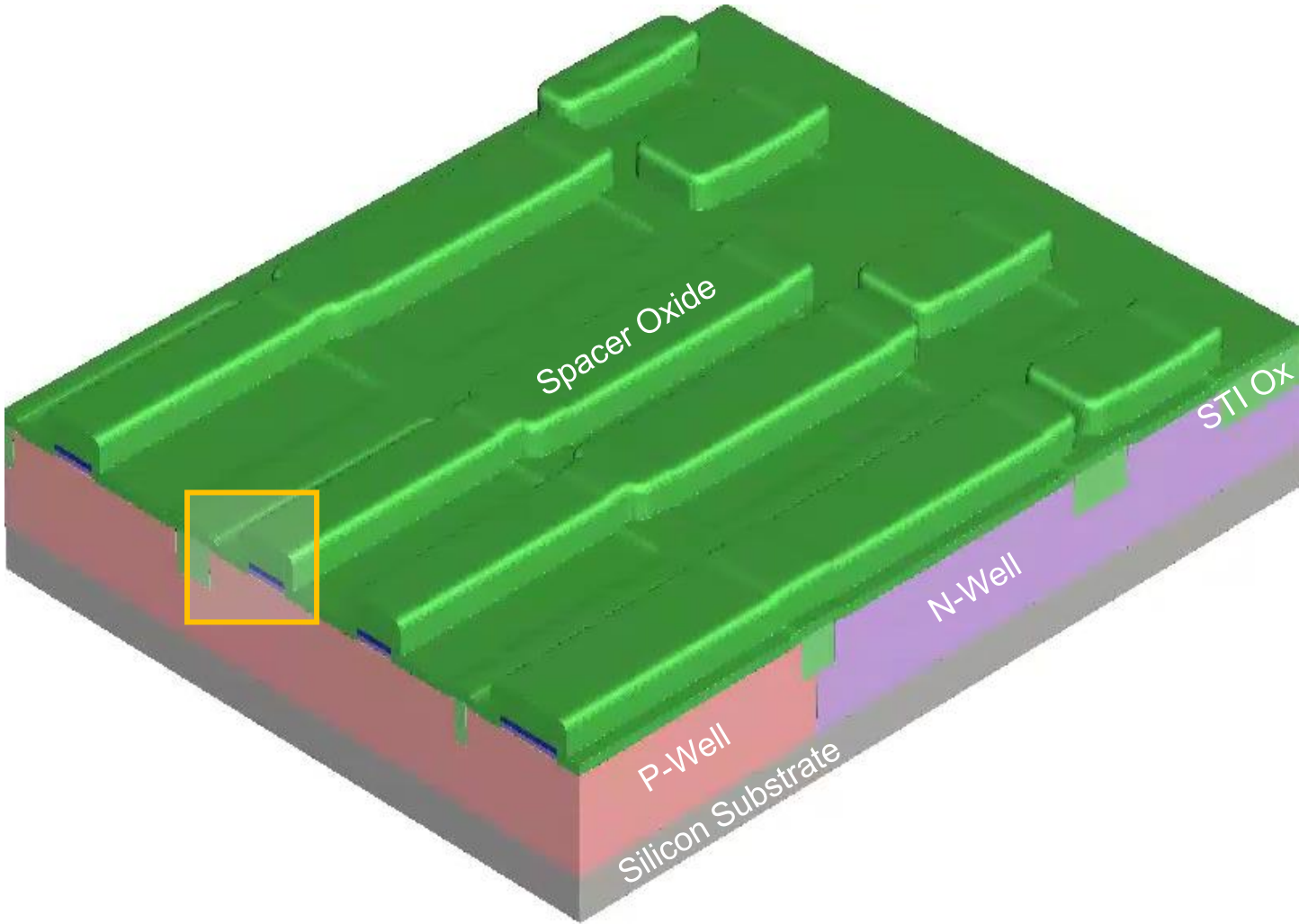
TG = Transistor Gates

TG SPACER OXIDE DEPOSIT [CVD]

- A thin film of silicon dioxide is deposited to form a spacer on the sidewalls of the gate. The spacer will protect the gate metal from corrosion and is used to ensure the source/drain implants will be correctly aligned to the gate.

Detail Close-up



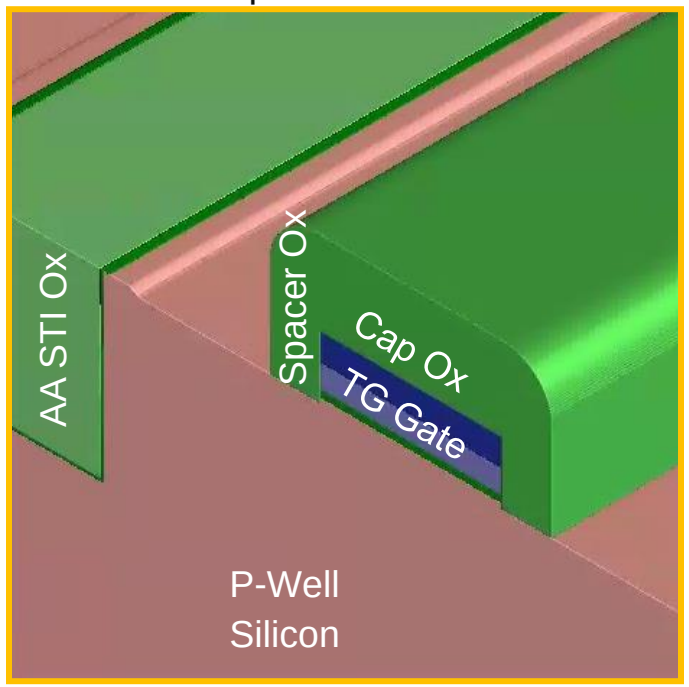


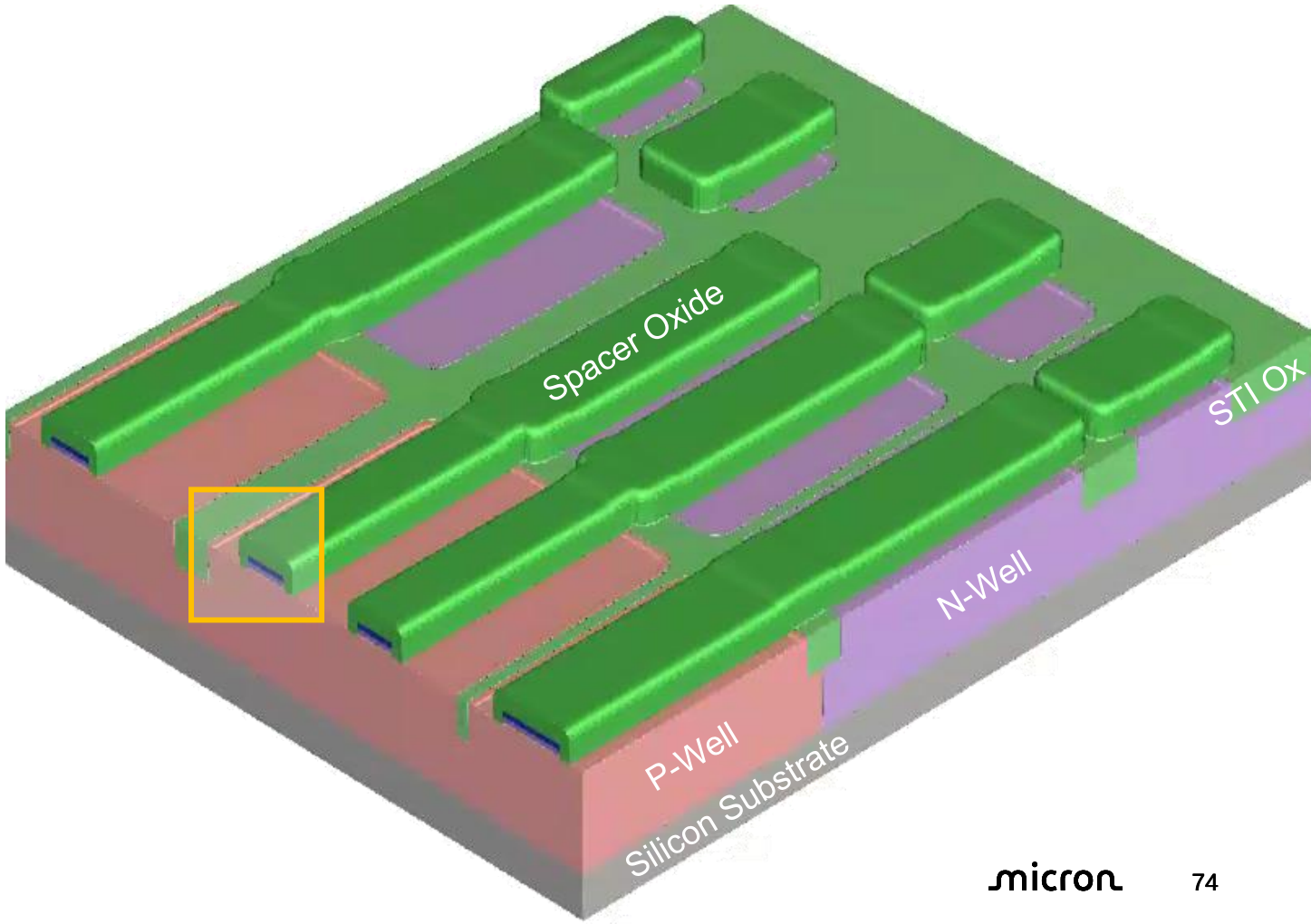
TG = Transistor Gates

TG SPACER OXIDE DRY ETCH [DRY ETCH]

- A specially-designed plasma process is used to etch the spacer oxide from the horizontal surfaces while the oxide remains intact on the sidewalls of the gates.

Detail Close-up





TG = Transistor Gates

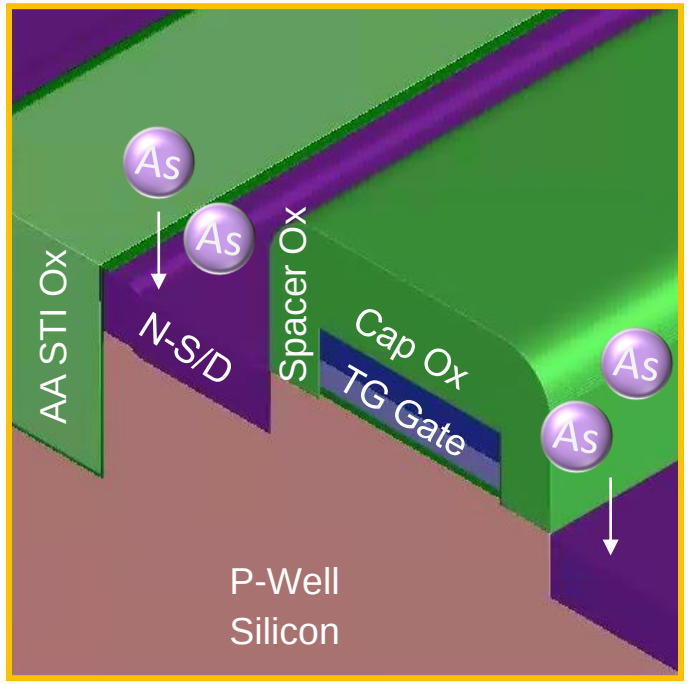
NA N-SOURCE/DRAIN PHOTO PATTERN

- The “NA” mask opens up the NMOS transistors to receive the N source/drain implant. A thick resist is used to block the implant in the areas that should not receive the implant.

NA N-SOURCE/DRAIN IMPLANT

- An ion implanter shoots a high dose of arsenic ions into the silicon near the surface to form the sources and drains for the NMOS transistors

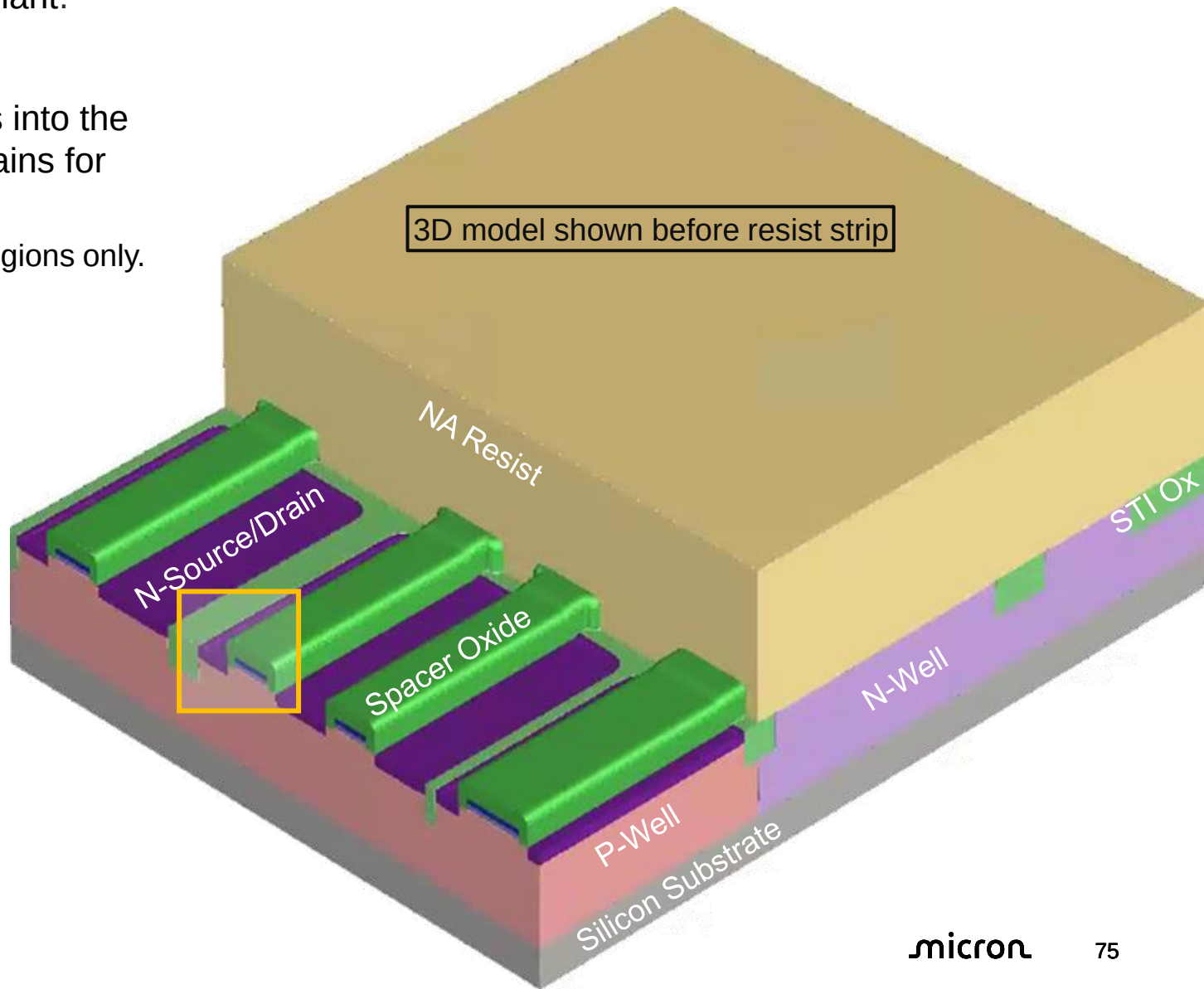
Note: The gate and spacers confine the implant to the S/D regions only. This is known as a “self-aligned” implant.



NMOS = N-Channel Metal Oxide Semiconductor Transistor

NA RESIST STRIP [WET PROCESS]

- Plasma and wet chemistry are used to remove the photoresist after the implant is complete



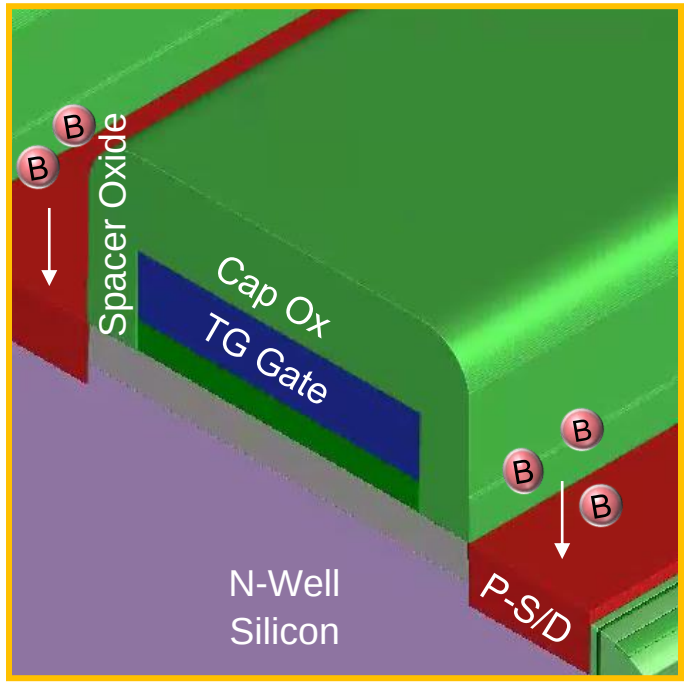
PA P-SOURCE/DRAIN PHOTO PATTERN

- The “PA” mask opens up the PMOS transistors to receive the P source/drain implant. A thick resist is used to block the implant in the areas that should not receive the implant.

PA P-SOURCE/DRAIN IMPLANT

- An ion implanter shoots a high dose of boron ions into the silicon near the surface to form the sources and drains for the PMOS transistors.

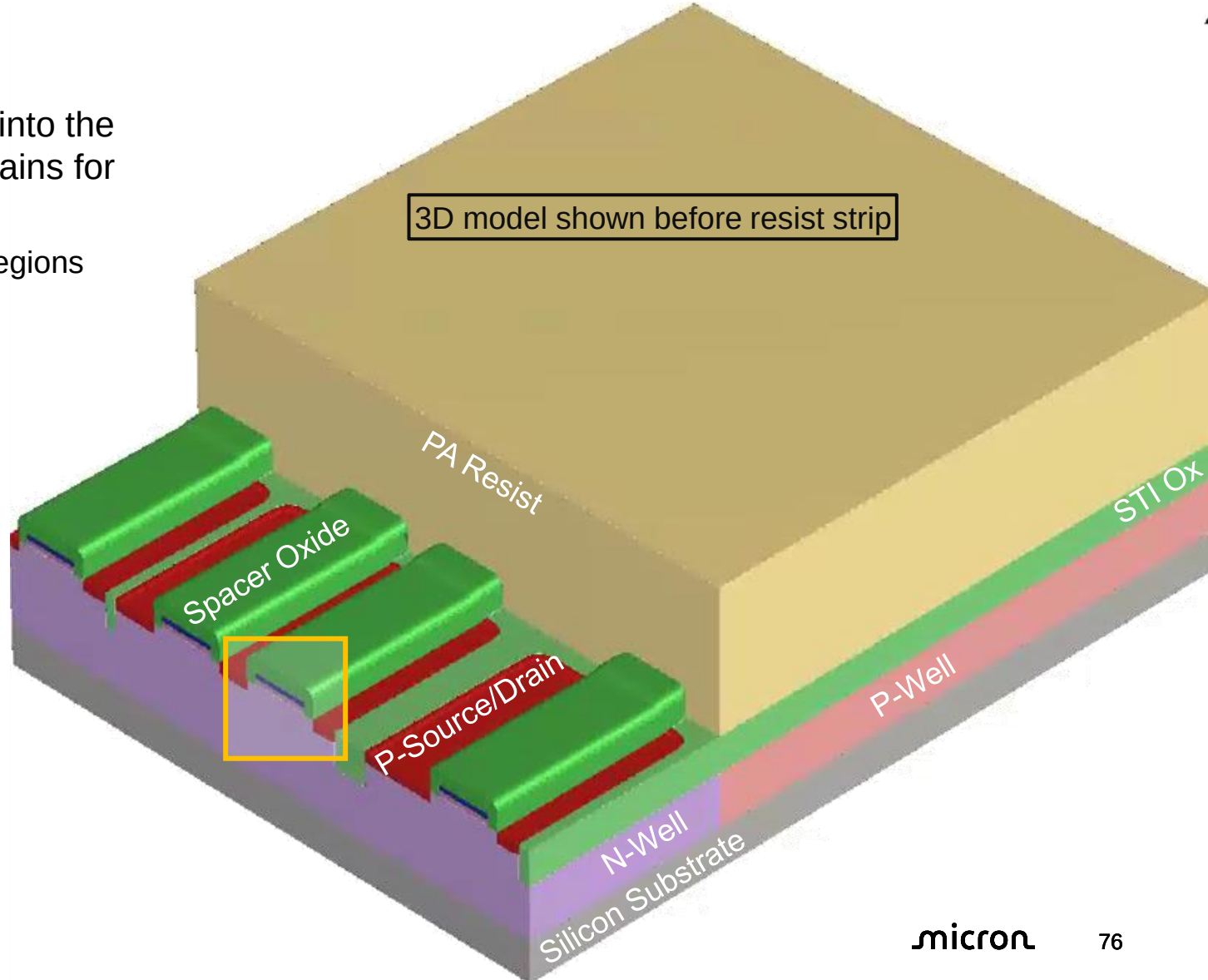
Note: The gate and spacers confine the implant to the S/D regions only. This is known as a “self-aligned” implant.



PMOS = P-Channel Metal Oxide Semiconductor Transistor

PA RESIST STRIP [WET PROCESS]

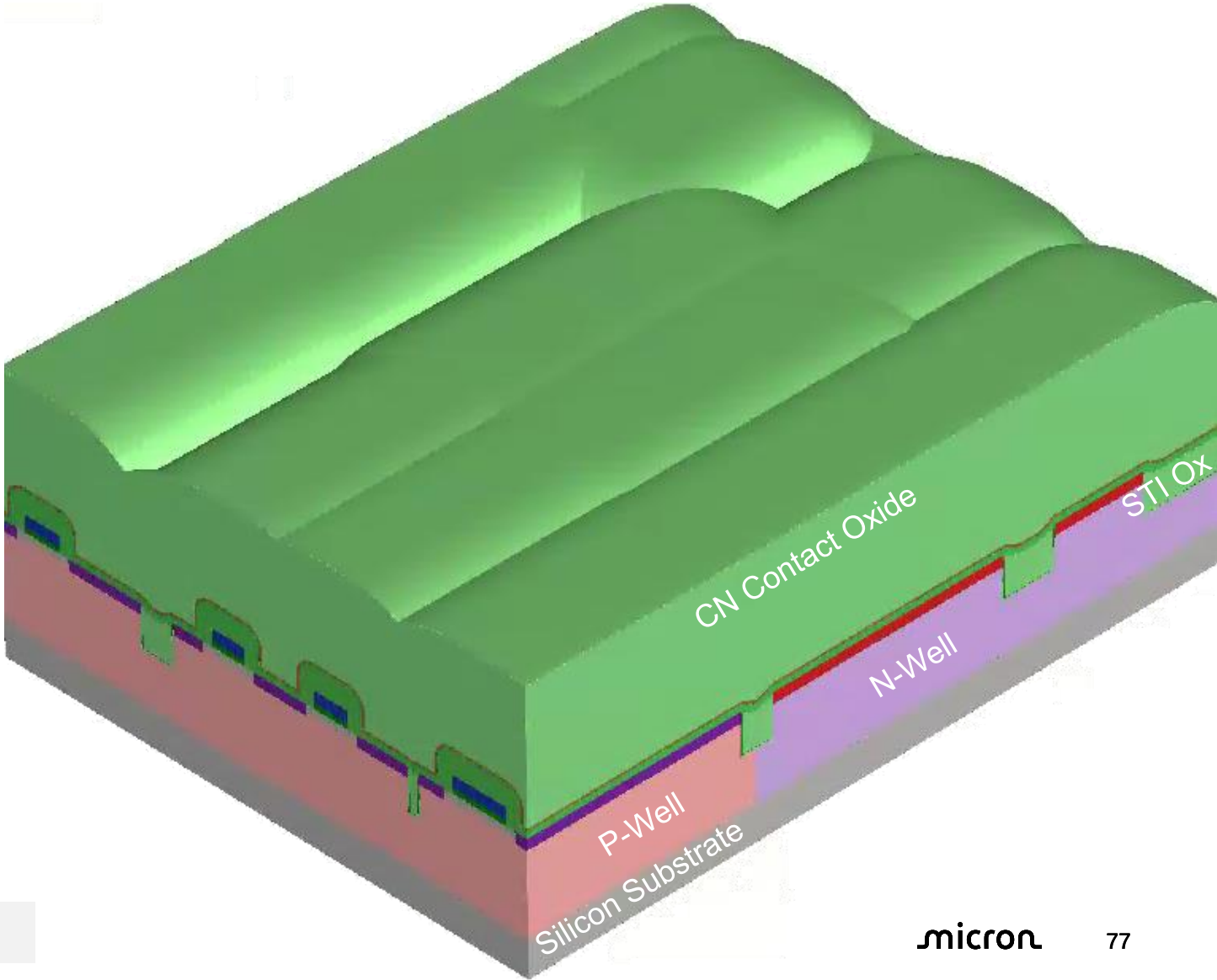
- Plasma and wet chemistry are used to remove the photoresist after the implant is complete.



CN CONTACT OXIDE DEPOSIT [CVD]

- A thick film of silicon dioxide is deposited to protect the CMOS transistors.

Q) What do you think is the next Traveler step?

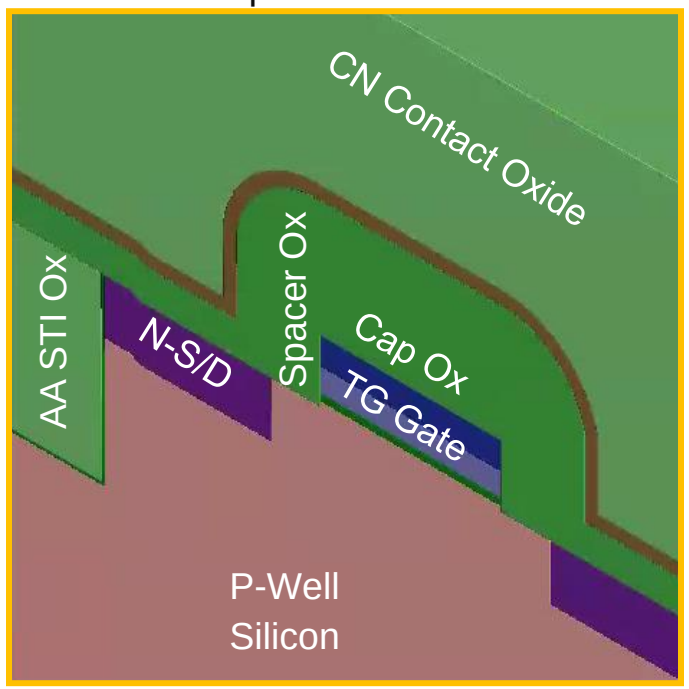


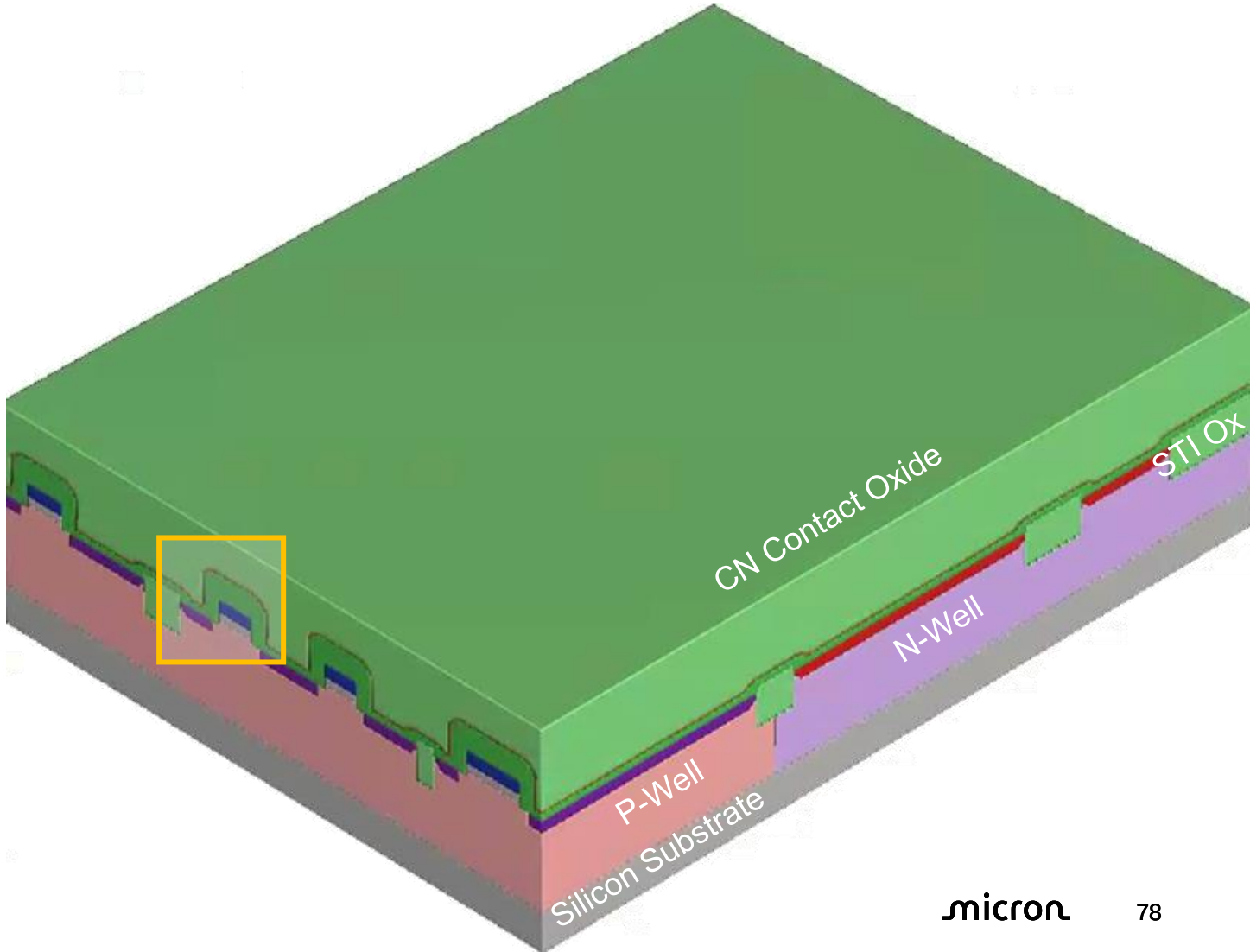
CMOS = Complimentary Metal Oxide Semiconductor Transistor

CN CONTACT OXIDE CMP [CMP]

- A polishing process is used to planarize the wafer surface to improve photo patterning of contacts. In this case a CMP “Stop in Film” timed process is used.

Detail Close-up





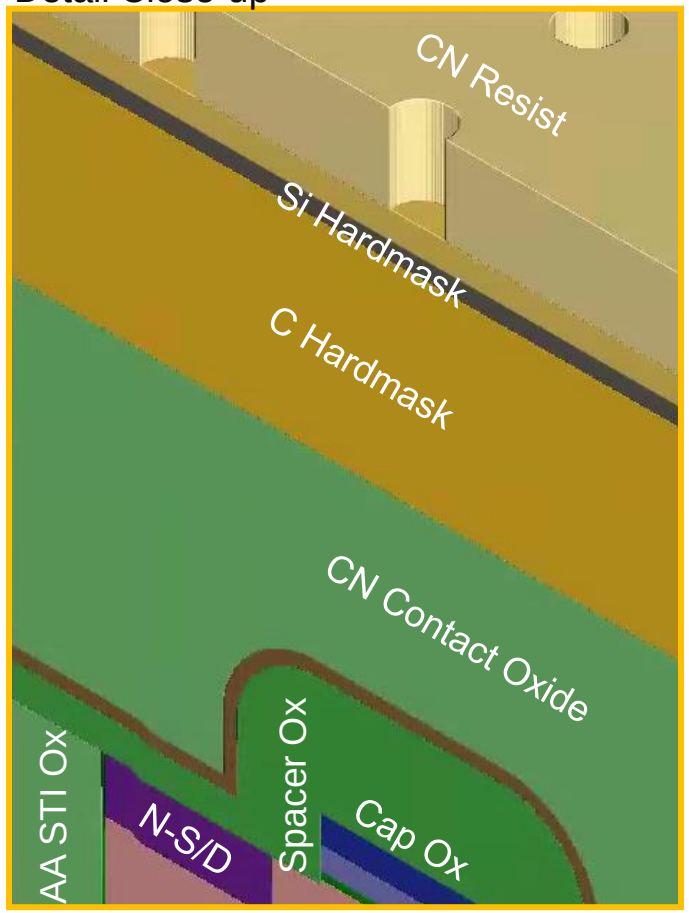
CN HARDMASK LAYERS DEPOSIT

- Deposit hardmask layers for patterning the contacts.

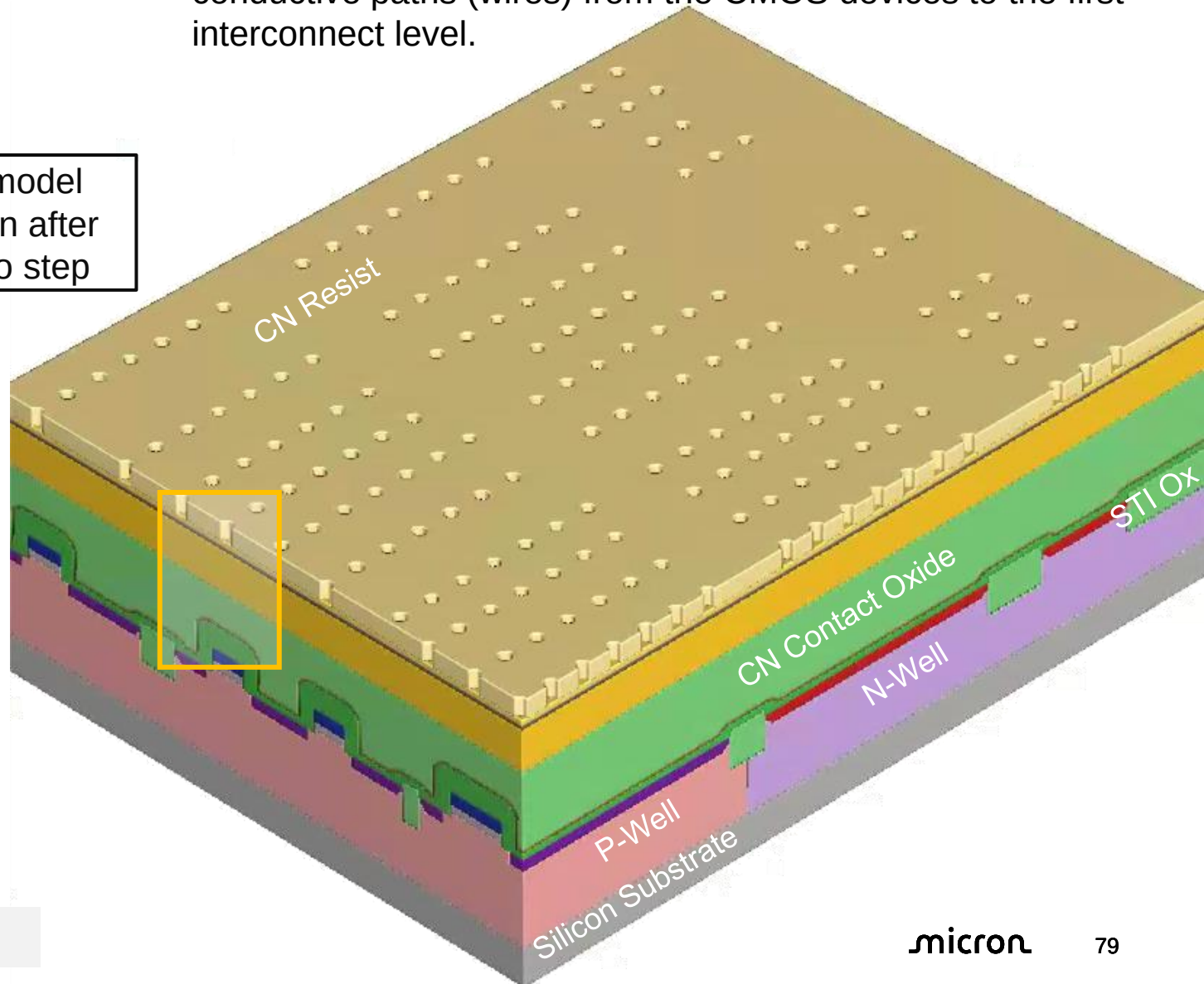
CN CONTACT PHOTO PATTERN

- The “CN” mask is used to define the pattern in photoresist for the contacts. The contacts will provide vertical conductive paths (wires) from the CMOS devices to the first interconnect level.

Detail Close-up



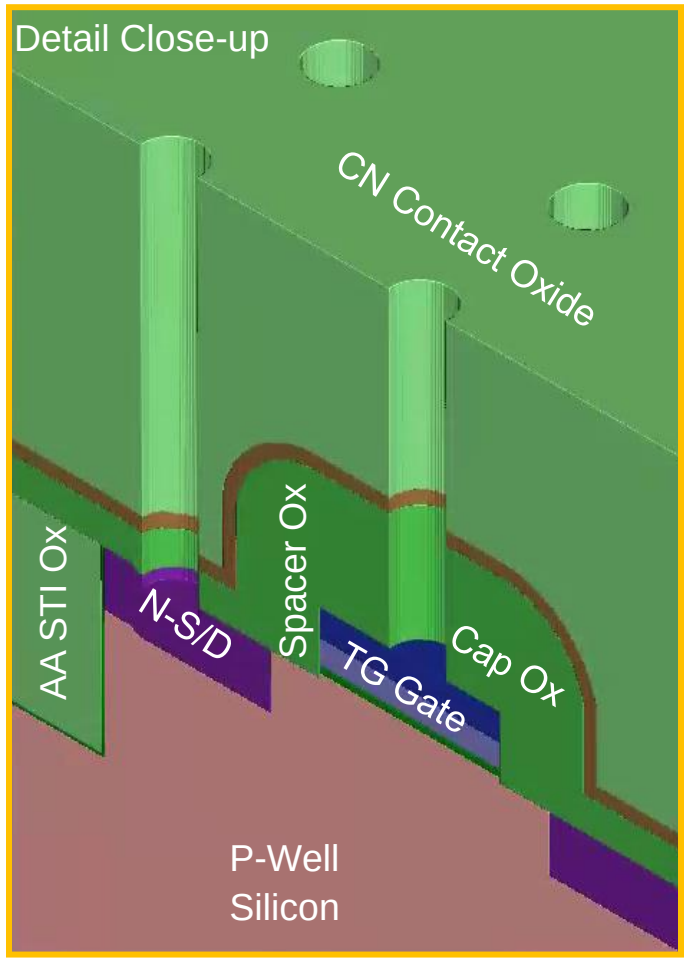
3D model shown after photo step



CMOS = Complimentary Metal Oxide Semiconductor Transistor

CN CONTACT DRY ETCH

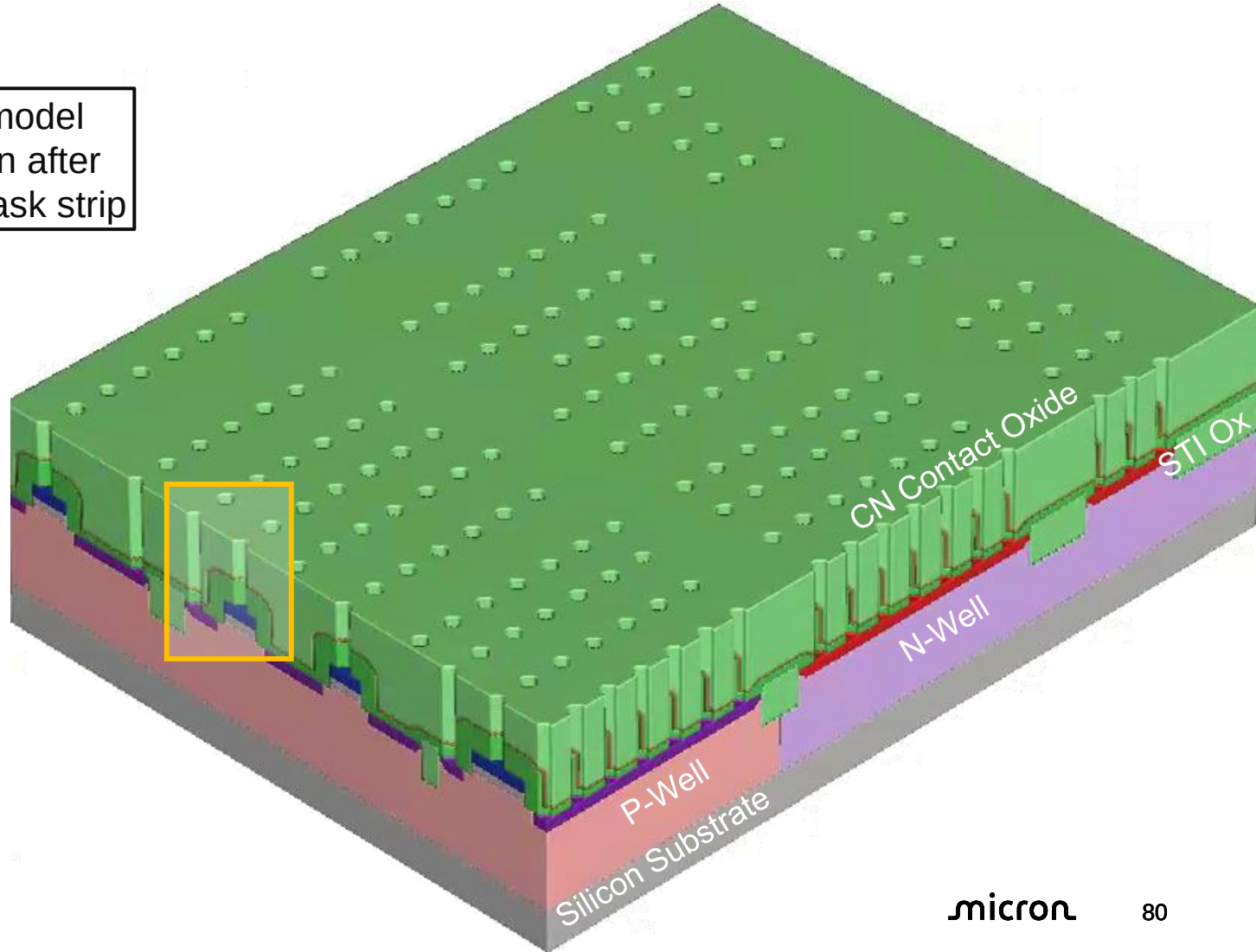
- A plasma process is used to etch holes in the hardmask layers, and down through the oxide films. The etch has selectivity to stop on the sources and drains (silicon), and gates (metal).



CN RESIST STRIP [WET PROCESS]

- Plasma and wet chemistry are used to remove the remaining carbon after the contact etch is complete.

3D model shown after hardmask strip

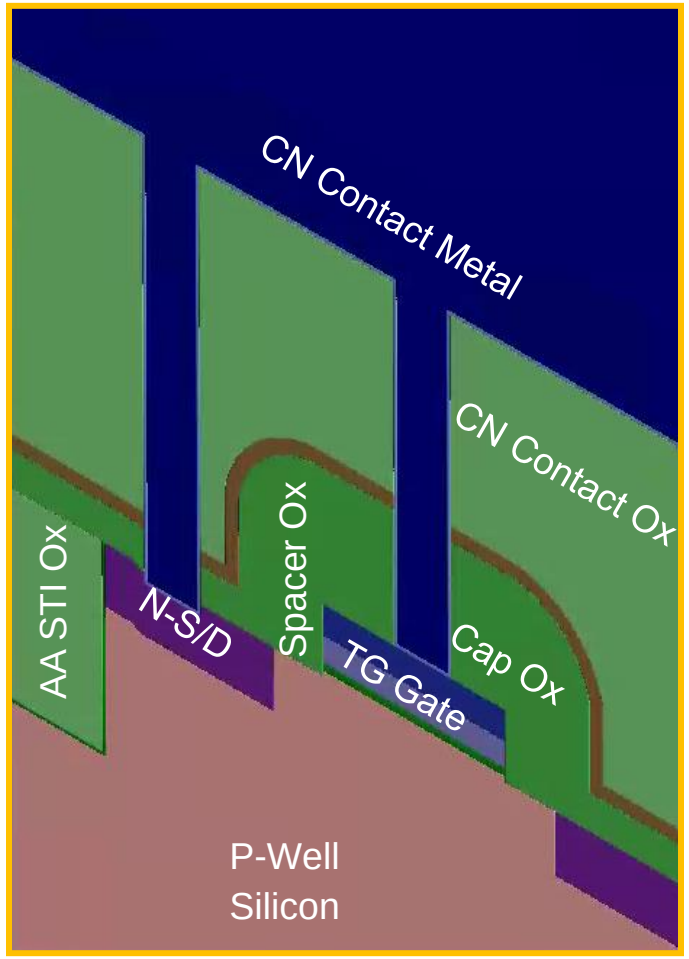


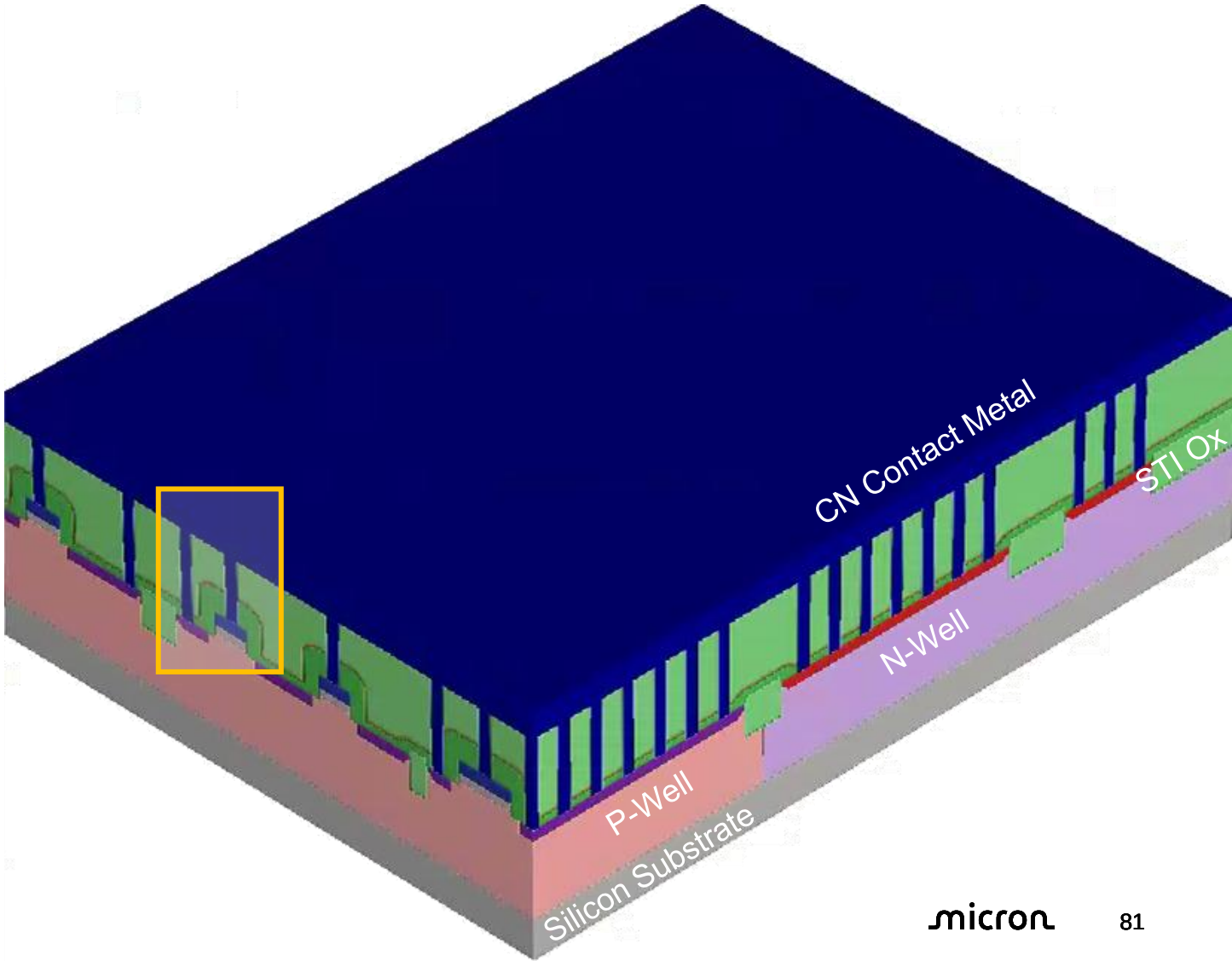
CN CONTACT METAL DEPOSIT [CVD]

- A conductive metal layer is deposited to fill the contact holes. CVD tungsten (W) is chosen to completely fill the holes without creating voids.

Q) What do you think is the next Traveler step?

Detail Close-up



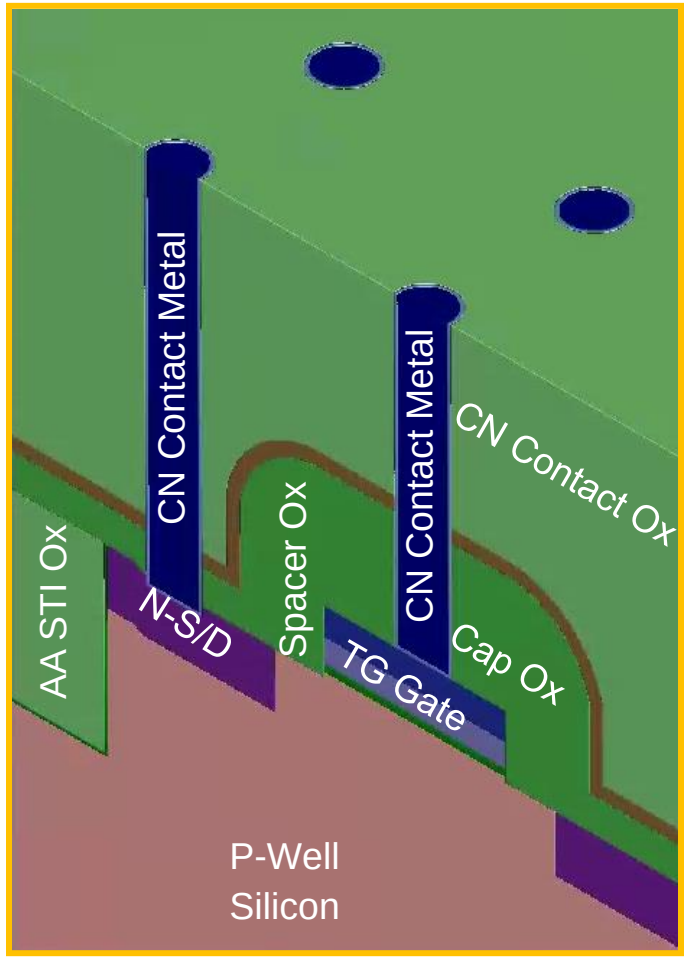


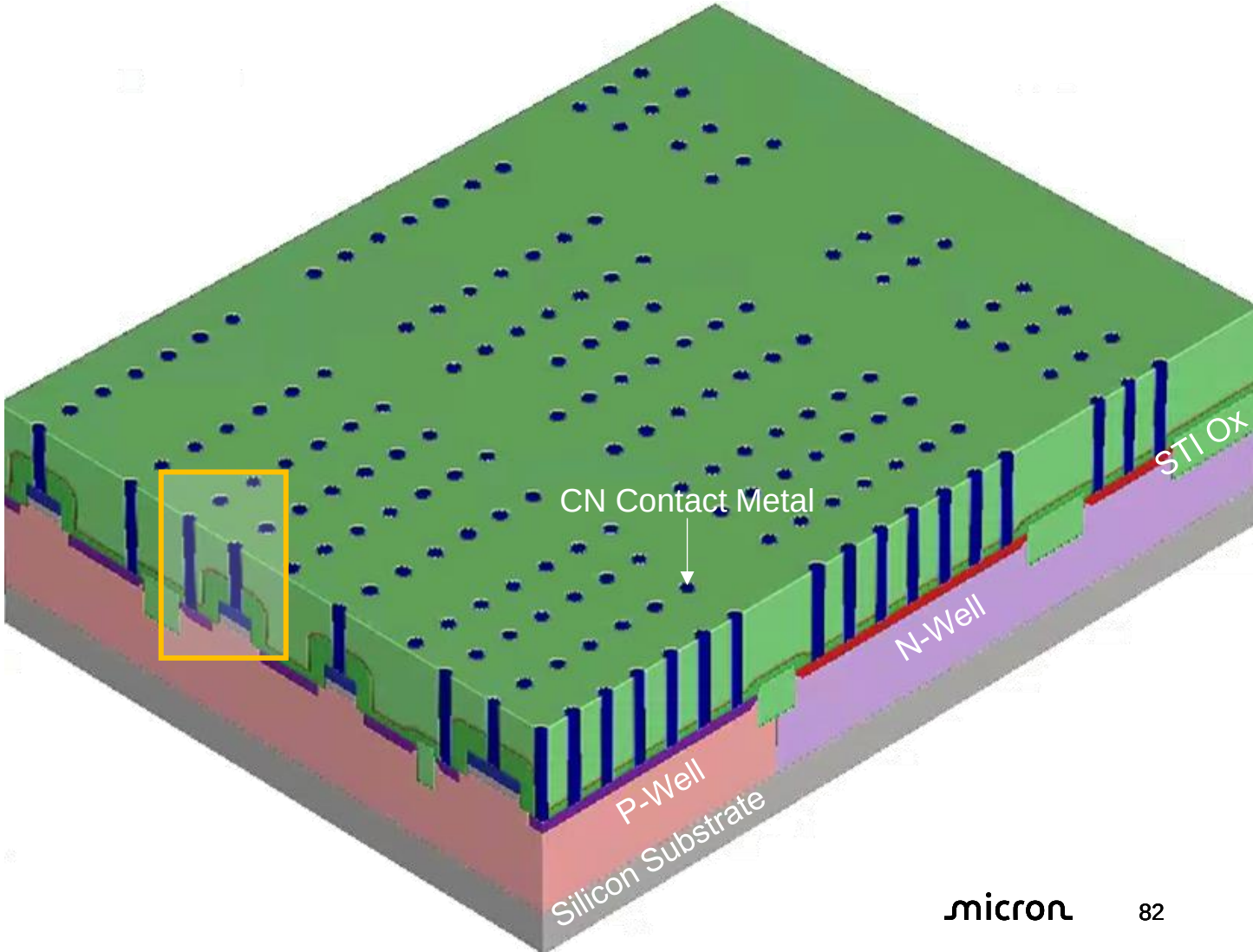
CN CONTACT METAL CMP [CMP]

- A polishing process is used to remove all the metal on the surface (known as “overburden”), leaving only the contacts filled with metal.

Q) What do you think is the next Traveler step?

Detail Close-up



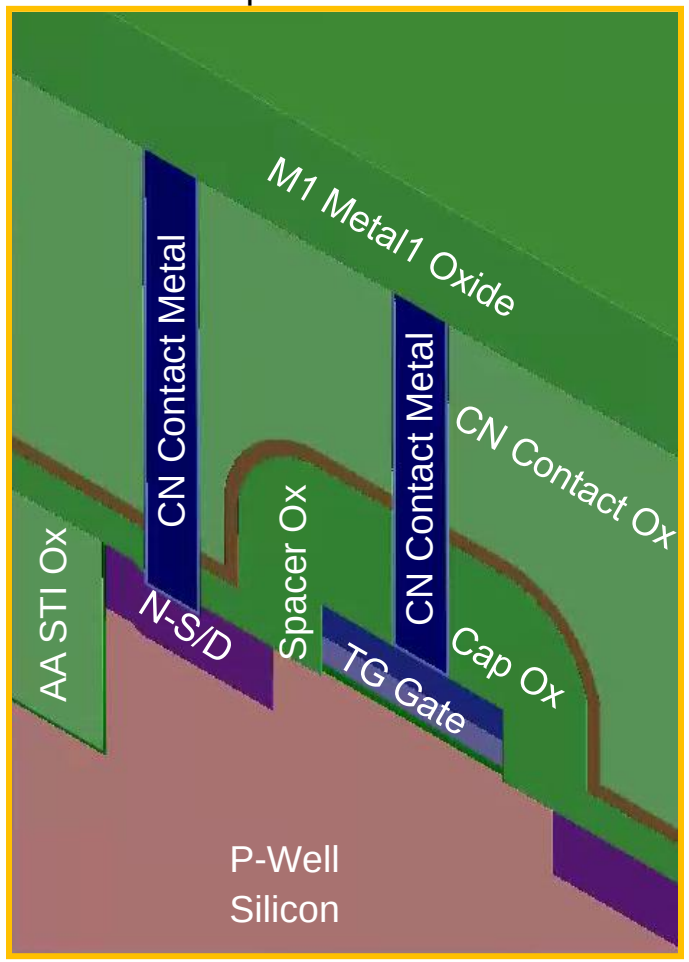


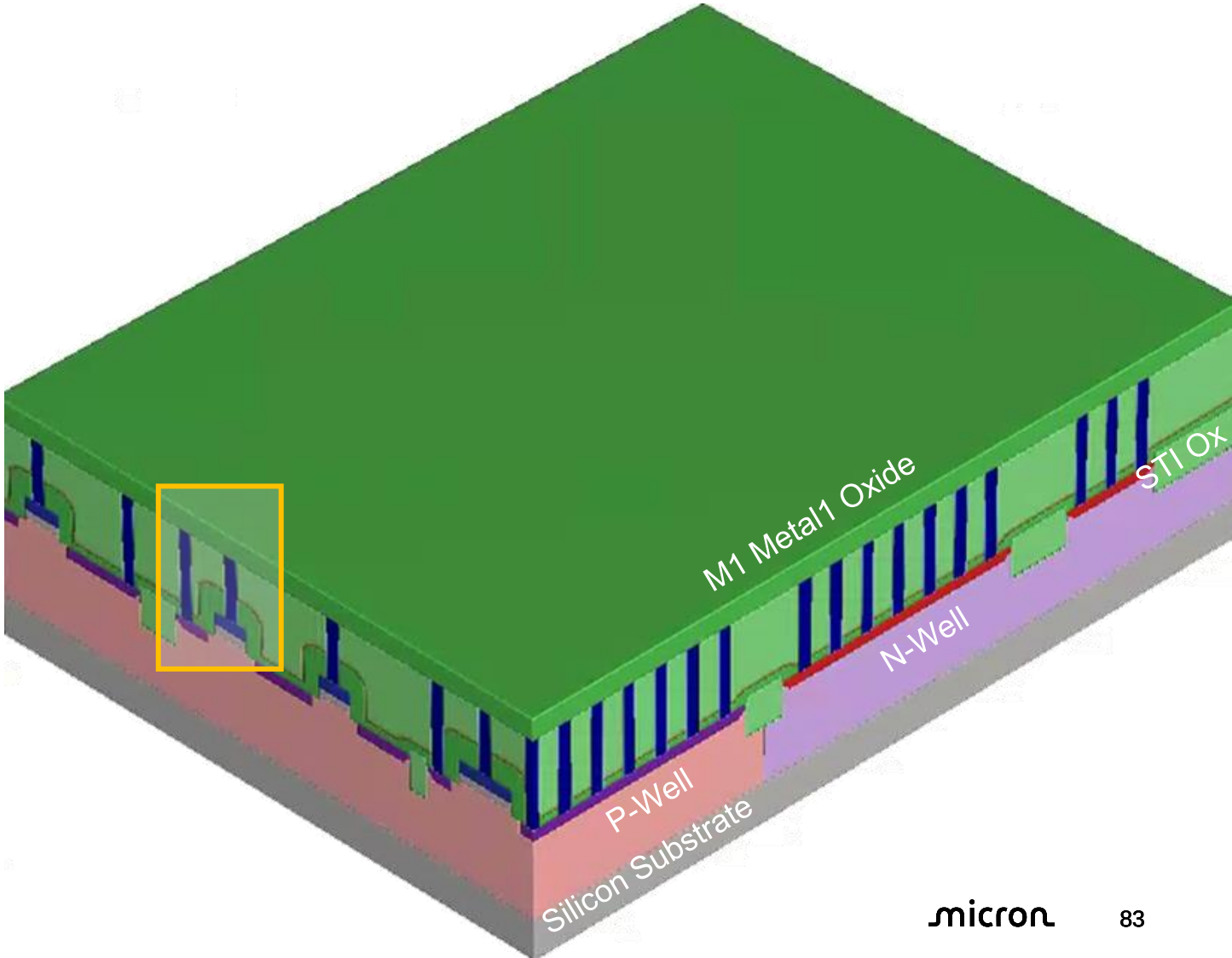
M1 METAL1 OXIDE DEPOSIT [CVD]

- A thick film of silicon dioxide is deposited to serve as the foundation for the formation of the first metal interconnect layer.

Note: Most chips will have multiple levels of metal interconnects. In this example, we will only show one level.

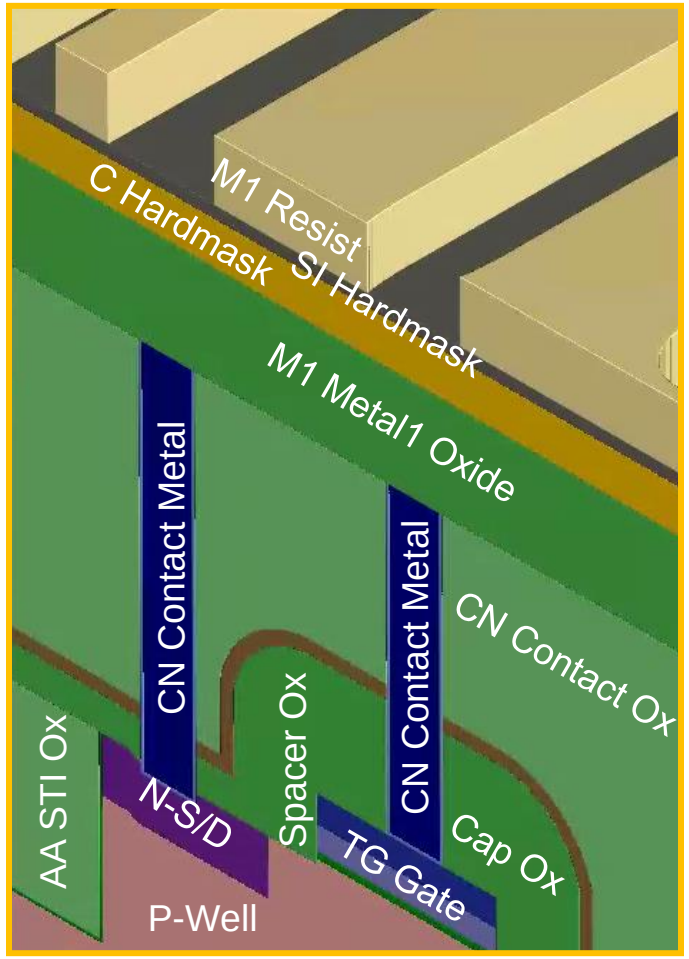
Detail Close-up





M1 HARDMASK LAYERS DEPOSIT

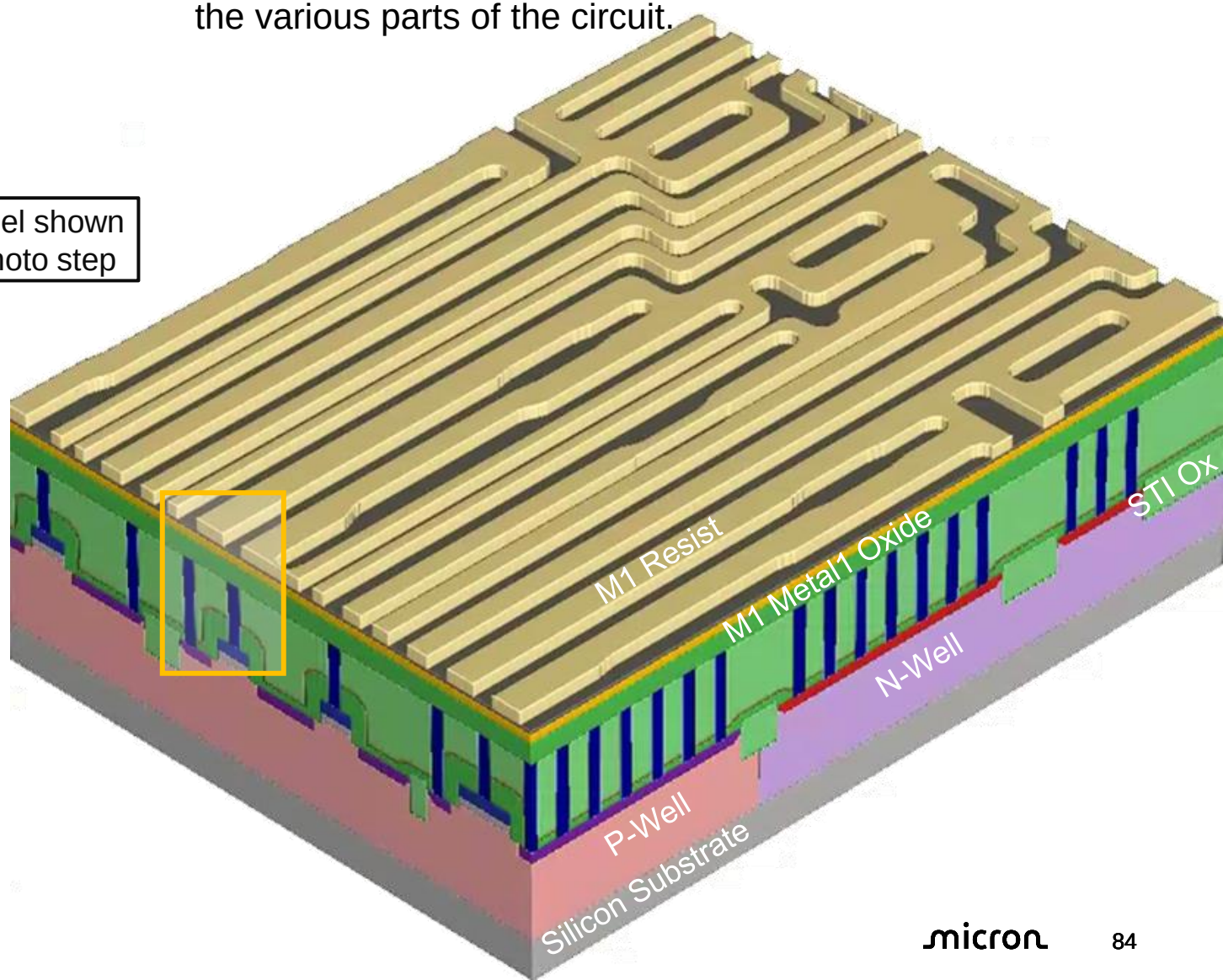
- Deposit hardmask layers for patterning the metal interconnects.



M1 METAL1 PHOTO PATTERN

- The “M1” mask is used to define the pattern in photoresist for the first level of metal interconnects. The interconnects will provide horizontal conductive paths (wires) connecting the various parts of the circuit.

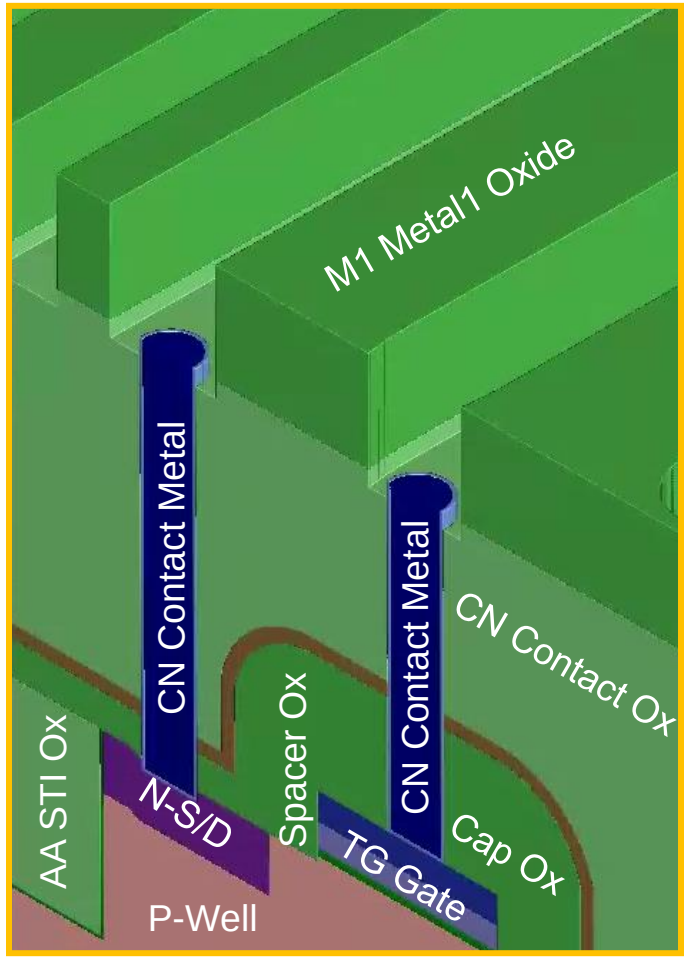
3D model shown after photo step



M1 METAL1 DRY ETCH

- A plasma process is used to etch trenches in the M1 oxide layer. The etch must be deep enough to expose the top of the CN metal contacts.

Detail Close-up

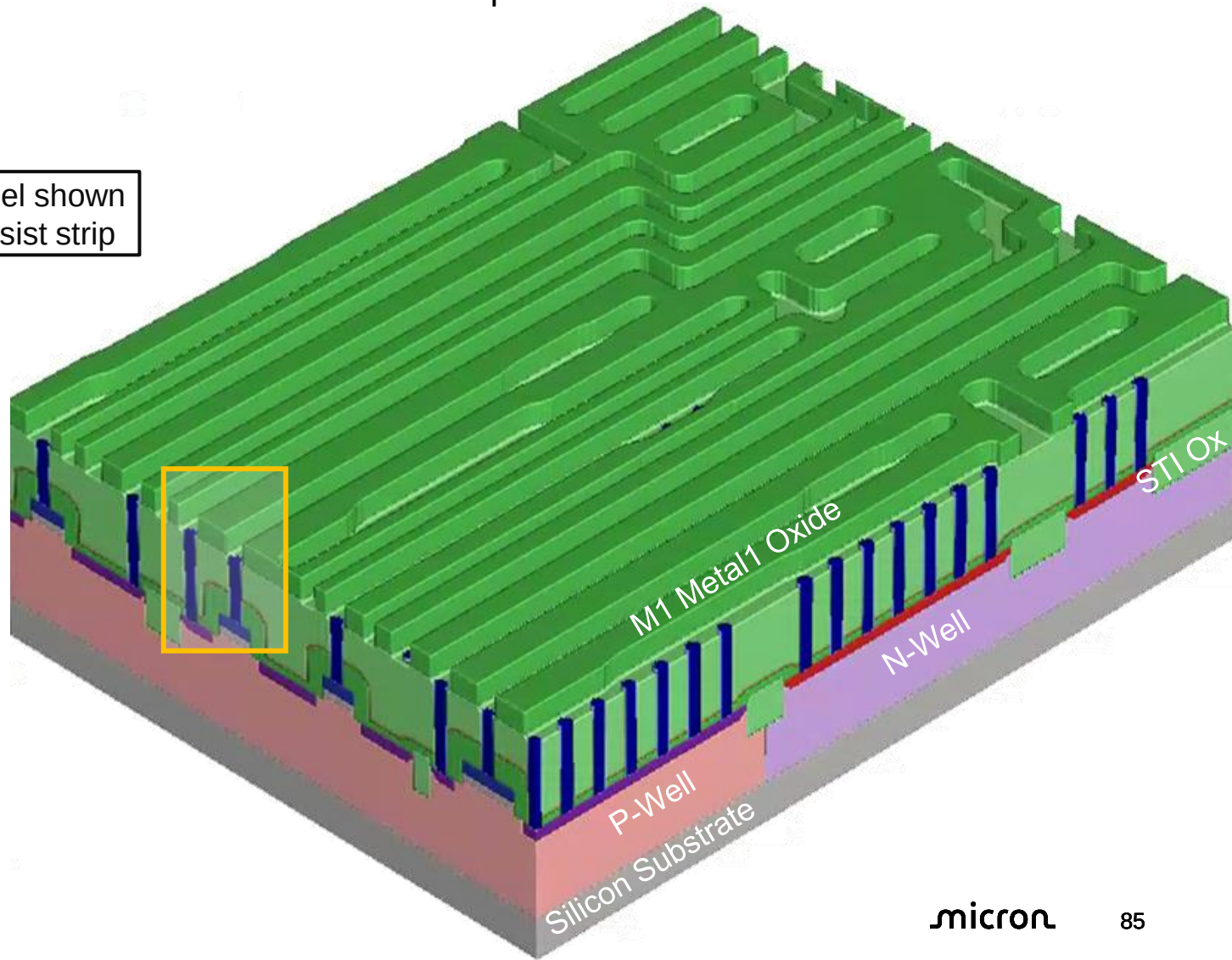


M1 RESIST STRIP [WET PROCESS]

- Plasma and wet chemistry are used to remove the remaining carbon after the trench etch is complete.

Q) What do you think is the next Traveler step?

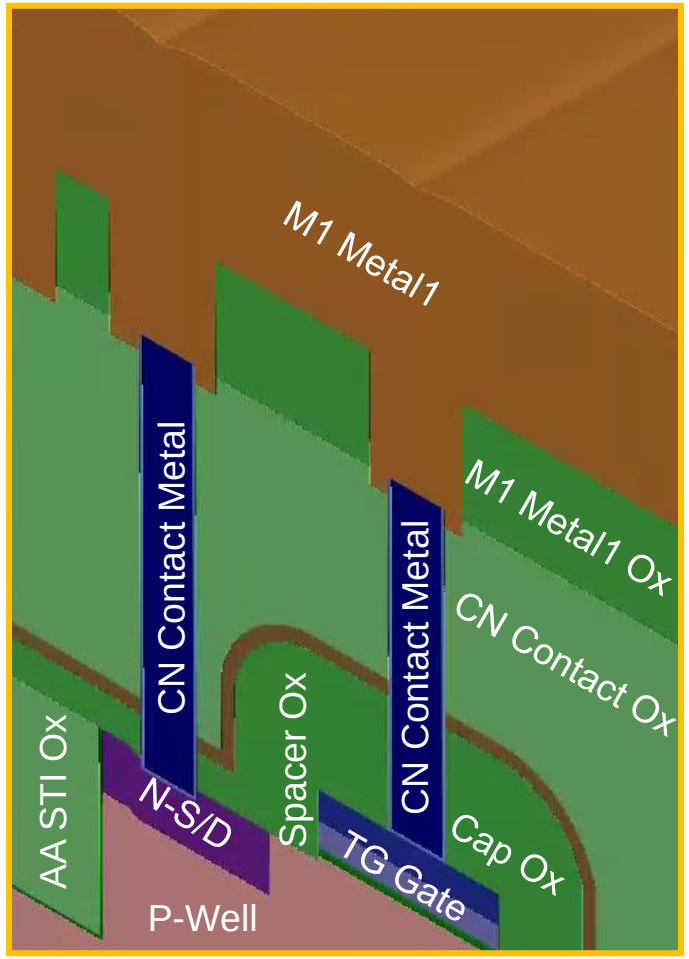
3D model shown after resist strip

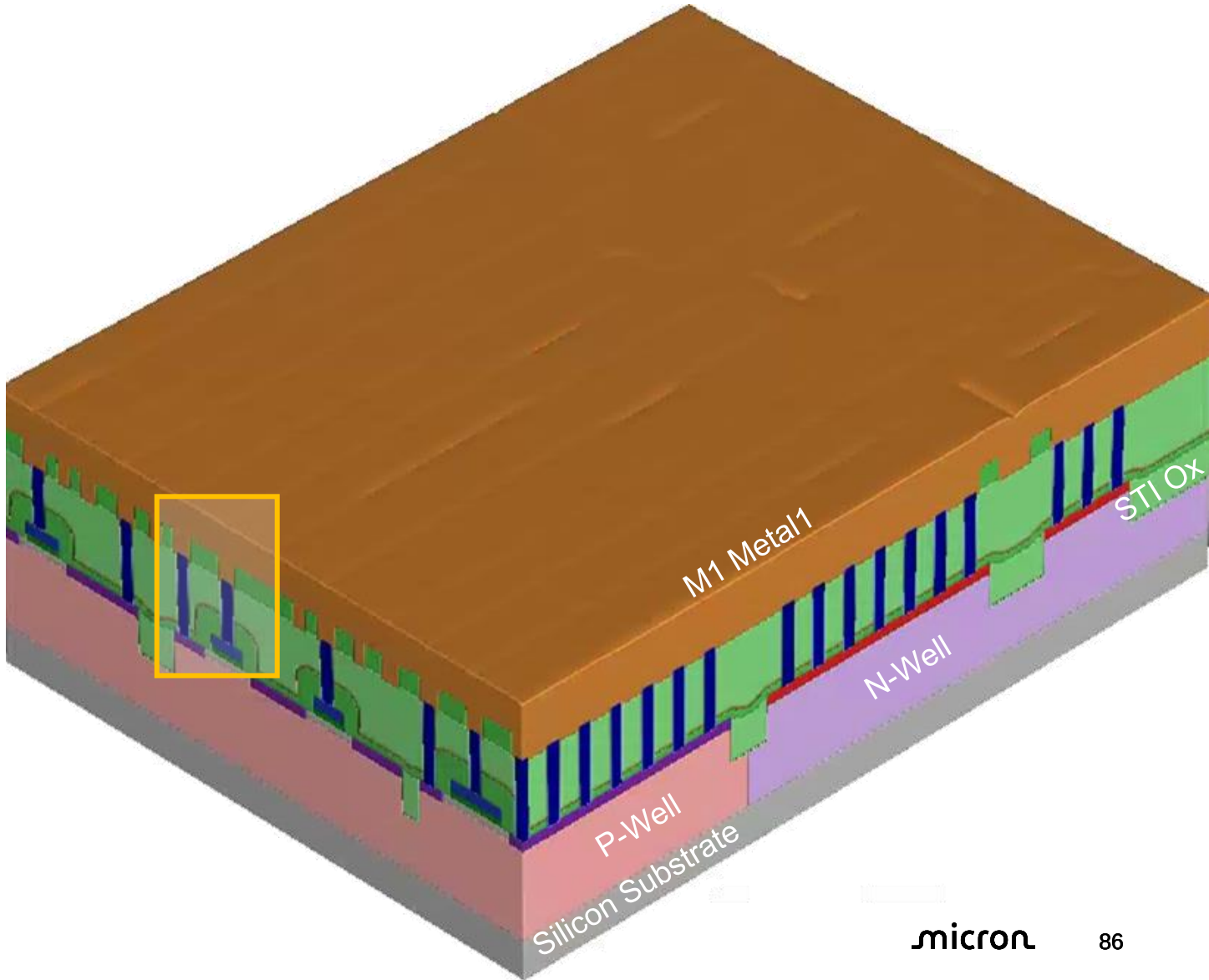


M1 METAL1 METAL DEPOSIT [WET PROCESS]

- A conductive metal layer is deposited to fill the trenches. Copper (Cu) is chosen for low resistivity. A special wet chemical process known as “electroplating” is used to deposit the copper.

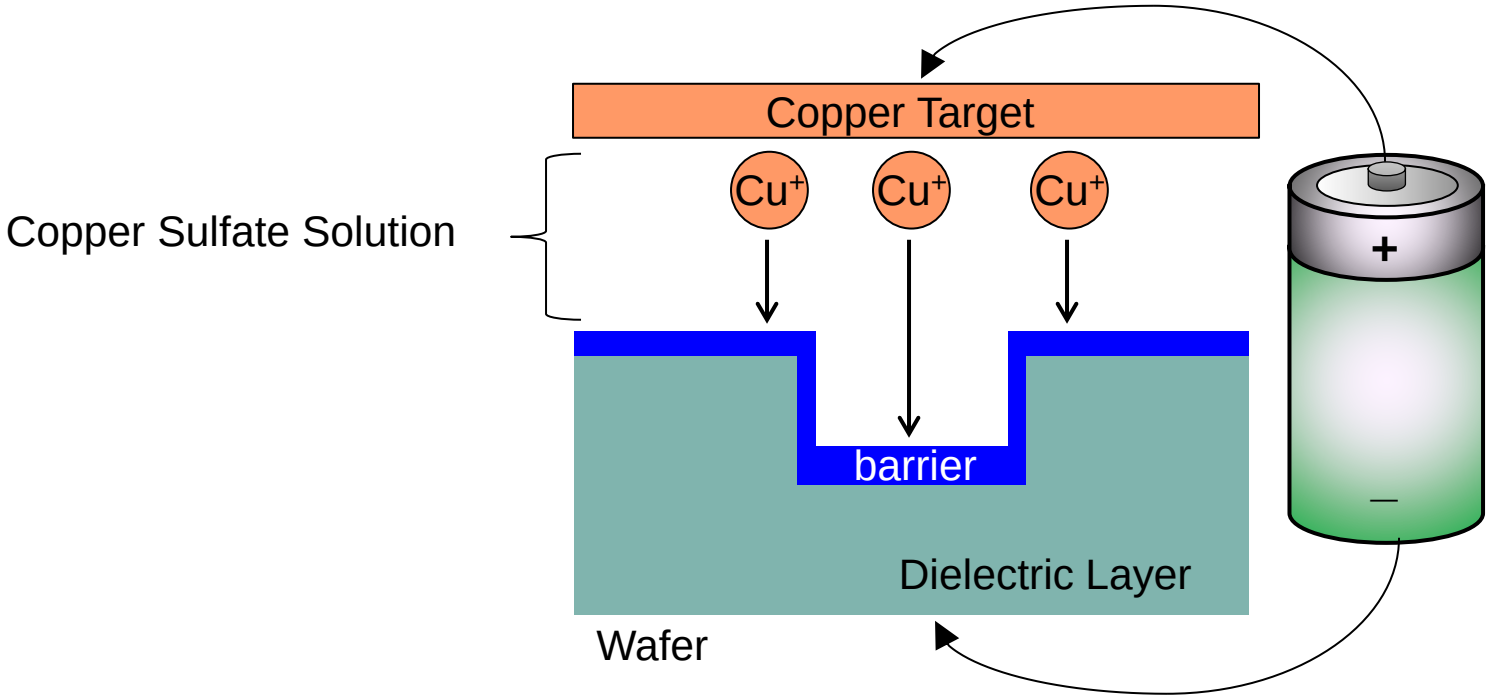
Detail Close-up





Wet Process – Electroplating

- Copper is uniquely deposited via electroplating.
- The wafer is immersed in a solution of copper sulfate. An electric current is forced through the solution, and copper ions are transported from a target to the wafer.
- Electroplating effectively fills deep trenches and is more cost effective than PVD for thick copper layers.

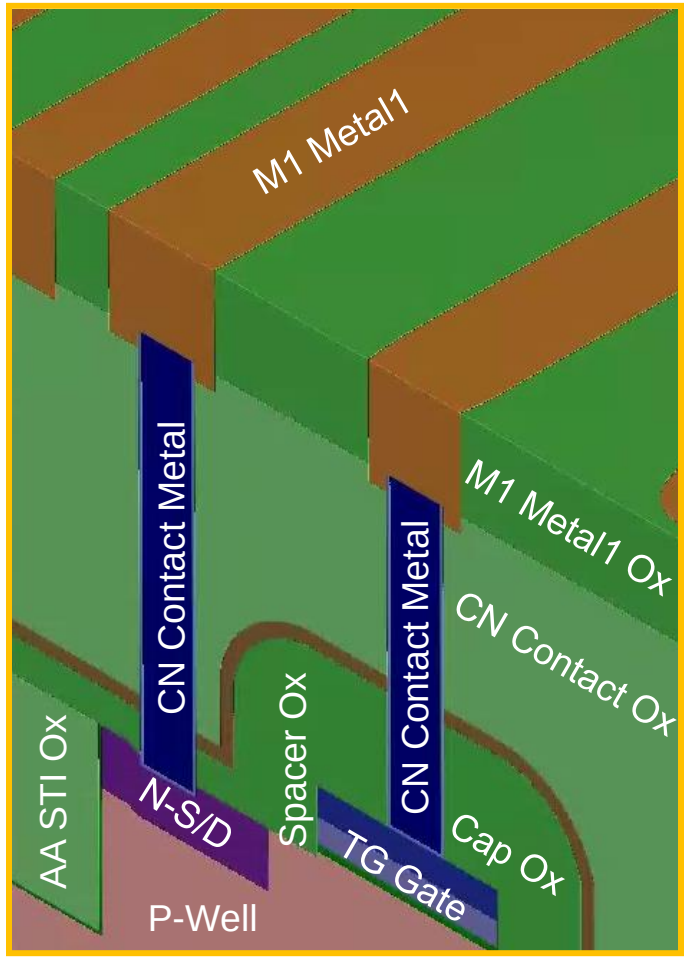


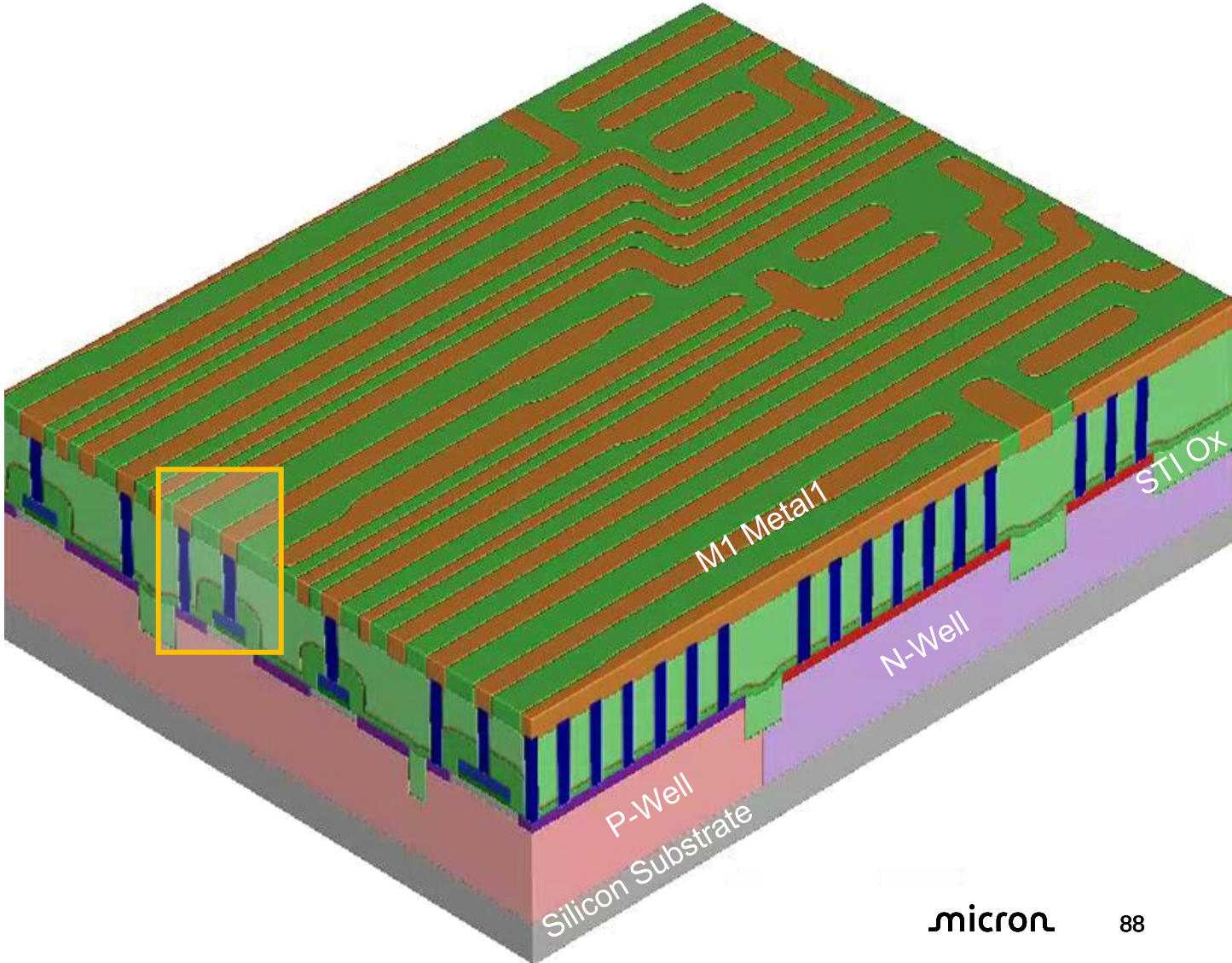
M1 METAL1 CMP [CMP]

- A polishing process is used to remove the overburden metal on the surface, leaving the trenches filled with copper.

Note: The process of forming metal interconnects by filling trenches with metal and then using CMP to remove the surface metal is known as “damascene”. (Due to resembling the ancient metal handicrafts made in Damascus, Syria)

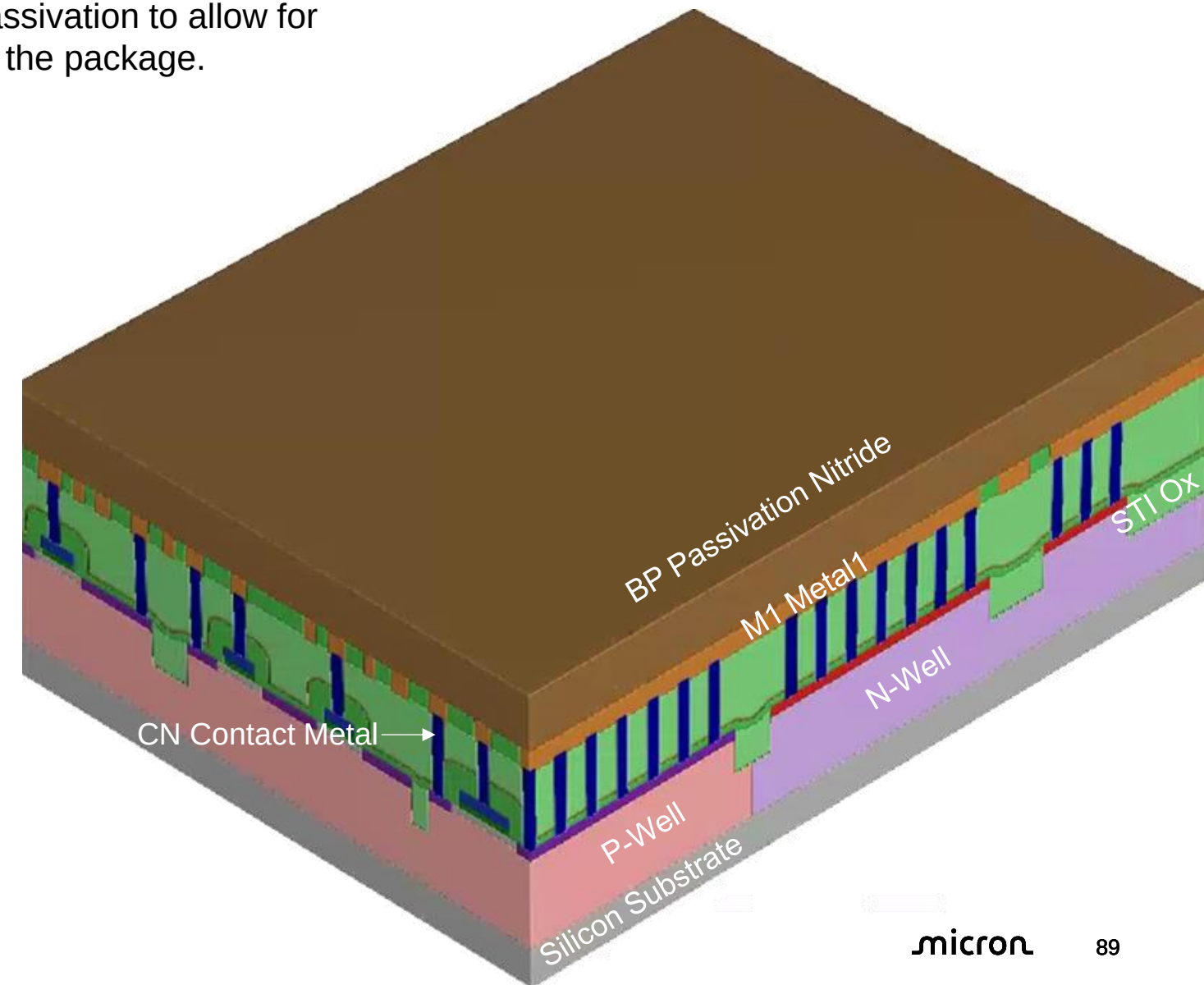
Detail Close-up





BP PASSIVATION DEPOSIT [CVD]

- A thick film of silicon nitride, known as “passivation”, is deposited to protect the fragile circuits and devices from moisture, contamination, and damage.
- Large holes (not shown) will be etched into the passivation to allow for electrical testing and to connect the die circuits to the package.



Key Terminology Glossary

micron

Glossary

Term or acronym	Definition/description
Anneal	The anneal process exposes the wafer to high temperatures for a specific amount of time. These high temperatures enable the diffusion and activation of dopants. Anneal can also be used to relieve stress, densify films and repair implant damage, among other applications.
Array	The die has a memory array and a periphery. The memory array is where the data (1s and 0s) is stored.
CDs	Critical Dimensions. Refers to the size of a feature printed in a resist or etched into the substrate. Usually measured at the smallest or most critical structures within the die, and at various points across the wafer.
CMP	Chemical Mechanical Planarization (or Polishing). One of the ten fab areas. CMP has the purpose of removing material and planarizing the wafer surface. CMP uses a polishing pad and a chemical slurry to perform the polishing process.
CVD	Chemical Vapor Deposition. One of the ten fab areas. The CVD process is used to deposit films on the wafer. Gases are introduced into a chamber where plasma is usually used. The reaction generates a film that deposits on the wafer. CVD films can be very conformal making it a process of choice when a conformal film is needed in high aspect ratio contacts or trenches.
Cleanroom	A controlled environment used for semiconductor manufacturing where high levels of cleanliness are required to prevent particles and contamination on the product and processes. Cleanrooms have HEPA (high efficiency particulate air) filtration to remove particles from the air. Micron cleanrooms are one hundred times cleaner than a hospital operating room.
CMOS	Complementary Metal Oxide Semiconductor (MOSFET) transistors. CMOS are low-power electronic transistor devices used in digital applications. Complementary refers to the use of symmetrical pairs of p-type and n-type MOSFET transistors for logic functions.
Deposition	Also abbreviated as dep or depo. Refers to the process of depositing a film of a material on the wafer. Some fab areas that deposit films on wafer are CVD, PVD and Diffusion. Films deposited can be insulators (like silicon dioxide or silicon nitride), conductors (like tungsten or titanium) and also semiconductors.
Die	A memory die is a semiconductor memory chip in its state before it is packaged. At Micron, memory die are fabricated on a silicon substrate. Hundreds of memory die are built on the wafer, and after fabrication is completed, each memory die gets cut apart through the die singulation process. Individual memory die are very delicate, so they next go through the Packaging process.

Glossary

Term or acronym	Definition/description
Diffusion	One of the ten fab areas. In the Diffusion area there are vertical furnaces where a batch of up to 125 wafers can be loaded at a time in a boat. Gases are introduced through injectors. Different process take place in the diffusion area like oxidation, film depositions, and heat treatments.
Dopant	See doping
Doping	Doping is the process of intentionally adding specific impurities to a semiconductor material like silicon with the goal of changing the electrical properties of the material. The impurities added are called dopants. Examples of dopants used in the semiconductor industry are boron, phosphorous and arsenic.
Dry Etch	One of the ten fab areas. The purpose of Dry Etch is to etch or remove films using plasma (ionized gases). Wafers usually go first to the Photolithography area where a photoresist is patterned. The pattern is then used in the Dry Etch area. The regions of the wafer protected with photoresist do not get etched, while the regions of the wafer without photoresist get exposed to the Dry Etch plasma and the exposed film is etched away. Dry Etch can provide anisotropic etches.
Electroplating	Electroplating technology is used to deposit some films on wafer. This is the case of copper deposition, where the wafer is immersed in a solution of copper sulfate and an electric current is forced through the solution. Copper ions are transported from a target to the wafer.
EUV	Extreme Ultraviolet Lithography. EUV is a type of photolithography technology that uses extreme ultraviolet light at 13.5nm wavelengths to manufacture wafers.
Fab	Abbreviation for Fabrication facility. It refers to the cleanroom facility and all the equipment for memory semiconductors fabrication.
Fabrication	The process of building circuits on a silicon wafer in a cleanroom environment where all aspects of production (temperature, power, chemistries, moisture, contamination, etc.) are tightly controlled.
Implant	One of the ten fab areas. See Ion Implantation.
Ion Implantation	The process of introducing dopants into the silicon via a high-energy beam of ions directed at the wafer surface. The purpose of the dopants is to modify the electrical properties of the silicon wafer.
Manufacturing	See Fabrication

Glossary

Term or acronym	Definition/description
Mask	A masks is used as part of the photolithography process. A mask is a plate that has a pattern. Parts of the plate are opaque, and parts of the plate are transparent. The transparent regions of the mask allow ultraviolet light to pass through so the pattern can be transferred onto a photosensitive film on the wafer. Micron owns a Mask Technology Center in Boise, Idaho that fabricates the masks used at Micron.
Metrology	One of the ten fab areas. The Metrology area takes measurements that evaluate the results of prior traveler steps. Micron has different metrology tools that can measure film thicknesses, critical dimensions like the diameter of a hole or the distance between two lines, film resistivity, surface planarity, film composition, stress, etc.
Nitride	Abbreviation for Silicon Nitride or Si_3N_4. Nitride is an insulator used in many steps of the memory manufacturing process.
Oxidation	Refers to the process of introducing oxygen into a chamber which reacts with an exposed film and form an oxide of that film. A very common oxidation process at Micron is exposing the silicon wafer to oxygen, forming a high-quality silicon dioxide (SiO_2) film.
Pad Oxide	A film of silicon dioxide grown on the surface of the wafer to protect the silicon substrate from surface damage during implants and to keep the surface clean and free from defects
Periphery	A memory die is a memory chip in its state before it is packaged. The die has a memory array and a periphery. The periphery is the region of the die that has the many circuits that allow to operate on the memory array. Some of the periphery circuits are pumps, regulators, IO (Input/Output), ESD (electrostatic discharge circuits), etc.
Photo	See Photolithography
Photolithography	One of the ten fab areas. Photolithography is the process of defining a temporary pattern on a photosensitive film called photoresist. In the Photolithography process ultraviolet light of a specific wavelength is projected through a reticle or mask containing the pattern to project on the photoresist. After the light goes through the mask, a system of lenses shrinks the pattern and then the shrank pattern is printed on the photosensitive photoresist.
Photomask	See Mask
Photoresist	See Resist
PVD	Physical Vapor Deposition. One of the ten fab areas. See Sputtering.

Glossary

Term or acronym	Definition/description
Planarization	See CMP
RDA	Real-time Defect Analysis. One of the ten fab areas. RDA inspects wafers at critical points in the manufacturing process to identify and categorize defects. Defects can cause die failure. The information RDA gathers is used by the different fab areas to work on reducing defectivity.
Reticle	See Mask
Resist	Light sensitive film used to coat the wafer in the Photolithography area. In the Photolithography process ultraviolet light shines through a mask with a specific pattern (e.g., lines, spaces, etc.). The light then goes through a lens system that shrinks the image. The shrank image is exposed onto the light sensitive resist. After the resist is developed it is ready to be used by areas like Dry Etch or Implant where the wafer is etched or doped in the regions not protected by the resist, while the regions protected by resist don't get etched or doped.
Silicon Nitride	See Nitride
Smock	Garment used on top of street clothes to enter into a cleanroom. The purpose of the smock is to protect the wafers and fab processes from human contamination. Smocks are familiarly called bunny suits.
SON	Stop on Nitride. It refers to an etch or a film removal processes that is designed to stop upon reaching a silicon nitride film.
Sputtering	The process of bombarding a target with ions so dislodged pieces of the target get deposited on the wafer. This is the process used in the PVD tools.
Traveler	A sequential list of every step needed to make semiconductor memory at the wafer level. Each Traveler step is performed at one of the ten fab areas and has a Recipe associated with it. The recipe contains detailed instructions to process the wafer (e.g., specific temperatures, pressure, gases, speeds, time, etc.)
Wet Process	One of the ten fab areas. Wet Process uses chemical baths and de-ionized water to etch films and clean wafers to reduce defectivity. Wet process steps make up the largest percentage of traveler steps, as the wafer is cleaned after almost each active step of the traveler to ensure contamination is not carried over to the next step.

Document Updates

Document Updates

Date	Description
January 2025	• Added goals, objectives and target audience • Added Construction Analogy (slide 14) • Added schematics to Wafer Processing Areas slide (slide 15) • Added photo of diffusion vertical batch (slide 28) • Added slide on Reticles (slide 35) • Added slide on Hardmasks (slide 54) • Added slide showing before and after dry etch (slide 56) • Added several new images • Added acronym legends • Added glossary section (slides 90-94)

Educator Hub