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MOS Transistor (MOSFET) Device Physics

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Device Physics Module Sequence

1. **Semiconductor fundamentals & PN junction device physics**
   - Energy band diagram, fermi-level, density of states, doping, PN junction

2. **MOS Capacitor (MOSCAP)**
   - **MOS electrostatics, ideal CV, non-idealities, key parameter extractions**

3. **MOS Transistor (MOSFET)**
   - **Channel transport, long channel vs short channel, subthreshold slope, DIBL, GIDL**

Table of Contents

Device Physics: MOSFET – goal and objectives

Goal

- Provide a foundational understanding of MOSFET and its electrical characteristics

Objectives

- Illustrate the architecture and operations of MOSFET
- Interpret and draw band-diagram for different material systems and operating conditions
- Understand various non-idealities of MOSFET

Target Audience

- Interns, NCGs (new college grads) and new employees in some technical roles need to understand these concepts
- Examples of critical target audience roles at Micron that utilize these concepts
  - Device Engineer
  - Process Integration Engineer
  - Process Engineer
  - Design Engineer
  - Product Engineer
  - Reliability Engineer
  - Quality Engineer
  - Yield Enhancement Engineer
  - Probe Engineer
  - Characterization Engineer
  - Test Engineer
  - Verification Engineer
  - Signal Integrity Engineer

Pro tip

Everyone interviewing at Micron can use this presentation to prepare for the interview by learning foundational information about memory. Check out the candidate guides for Engineering, Technician and Business roles.

- Micron engineering candidate guide
- Micron technician candidate guide
- Micron business candidate guide

MOSFET IV Characteristics

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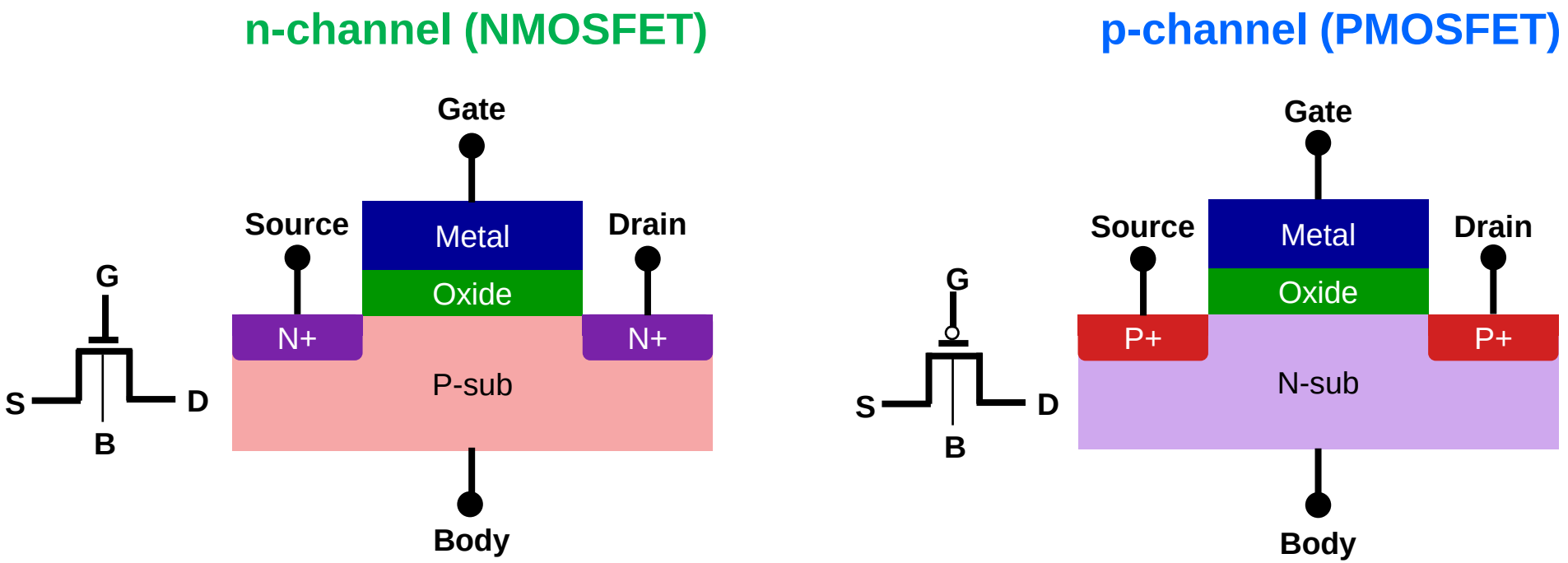
MOSFET

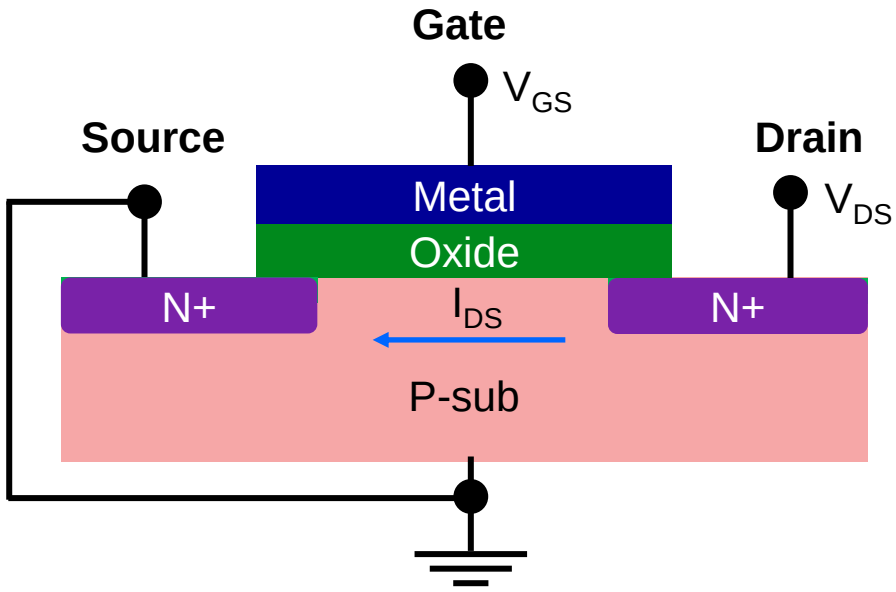
- **MOSFET** stands for **Metal Oxide Semiconductor Field Effect Transistor**
- MOSFET is a four-terminal device



- **CMOS** is **Complementary MOSFET** uses both NMOS and PMOS FETs for logic functions

MOSFET

- **Source** is **grounded** together with **bulk**
- Hence typically there are two potential of interest, V_{GS} and V_{DS}
- In terms of current, there is no I_{GS} as there is oxide in between metal and semiconductor, we are interested in I_{DS} that flows between source and drain

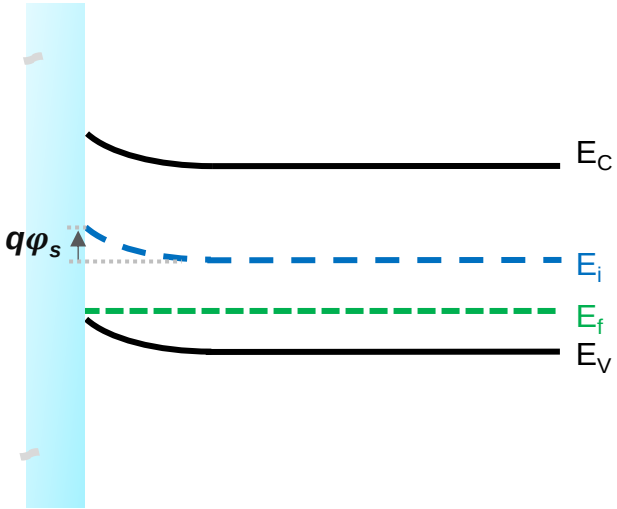


MOSFET Threshold Voltage, V_T

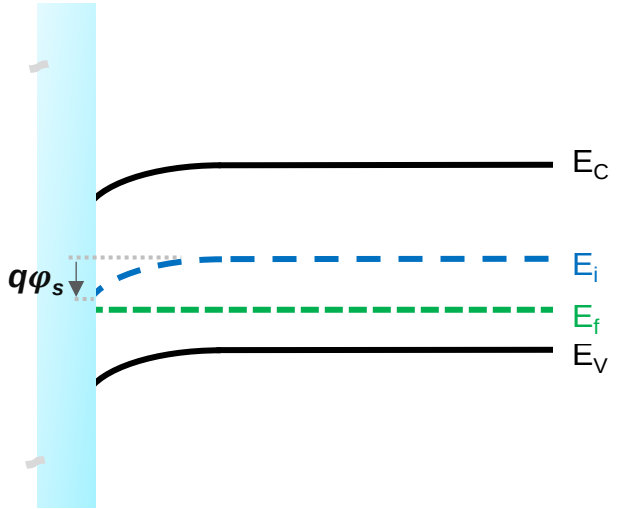
Refer to slide #14-20, MOSCAP - Part 2 document for detailed descriptions

Threshold = **Onset of strong inversion** (channel is inverted from p-type to n-type, electron concentration at surface equals holes concentration at bulk)

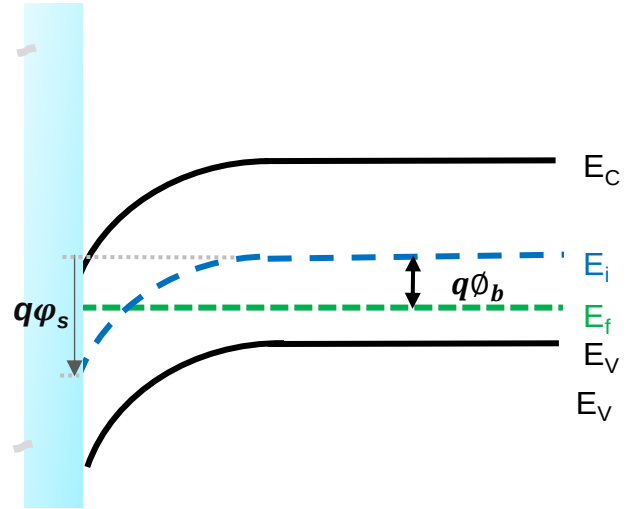
Convention: φ_s is positive when energy band bends down and negative when band bends up, recall $E = -e.V$



Accumulation



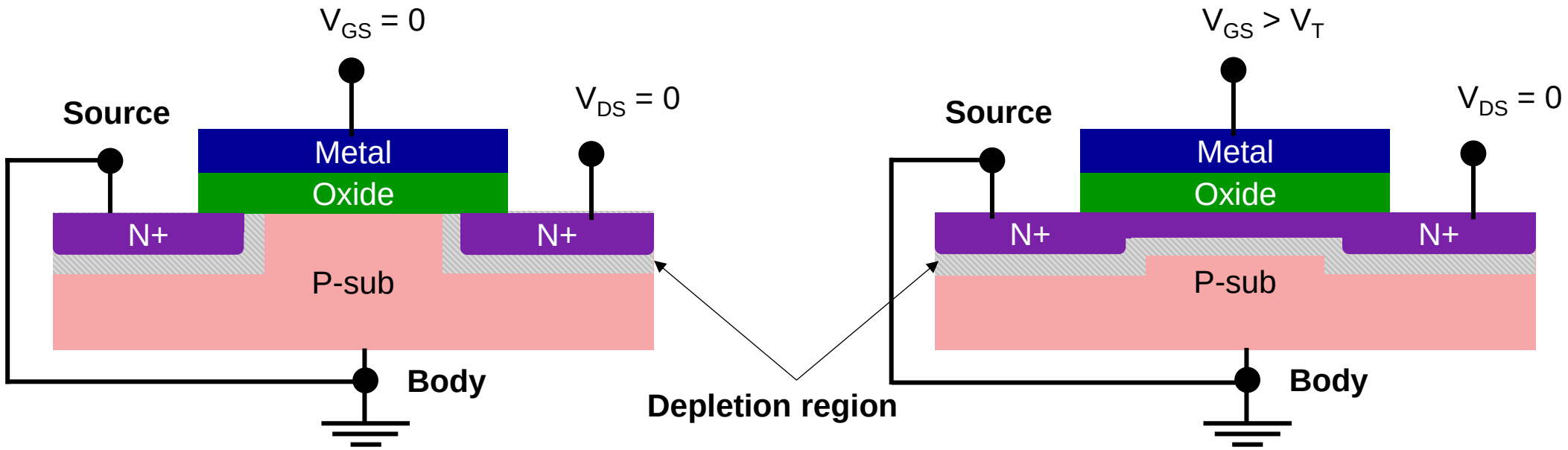
Depletion



Inversion (onset of strong inversion)

φ_s=2$\emptyset_b$

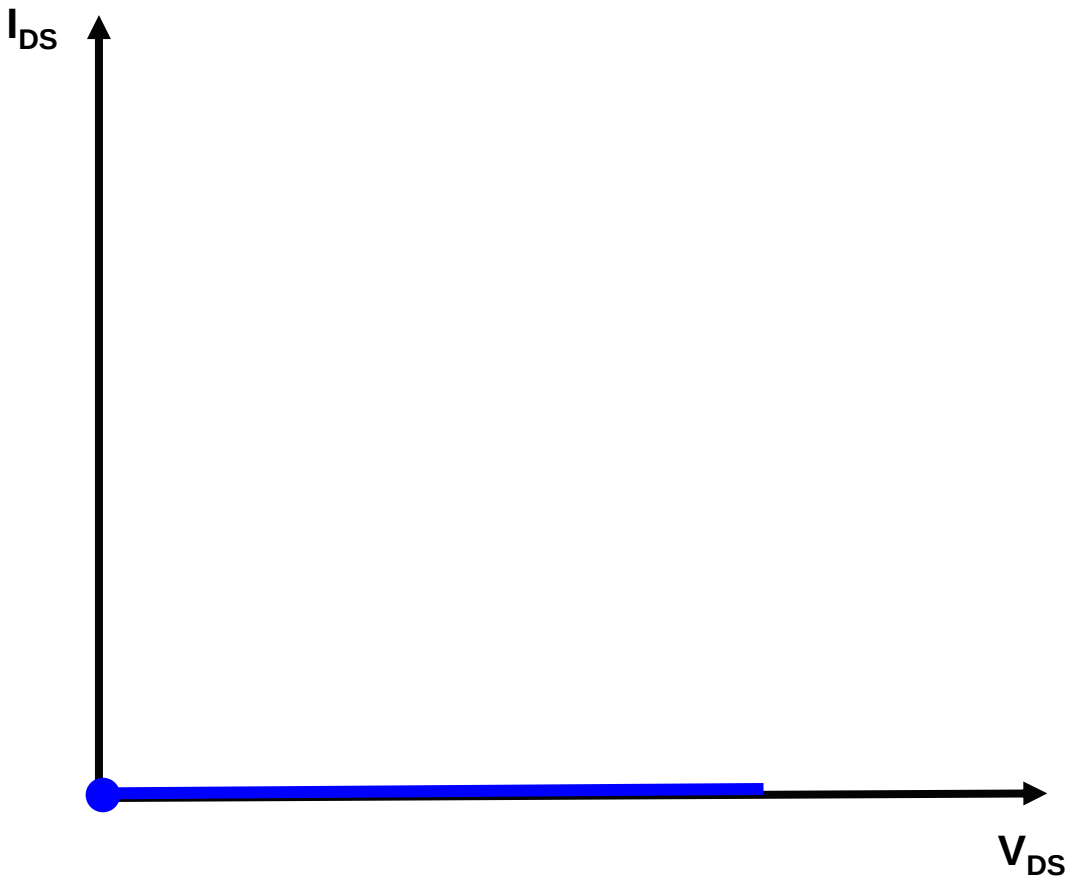
MOSFET IV Characteristics

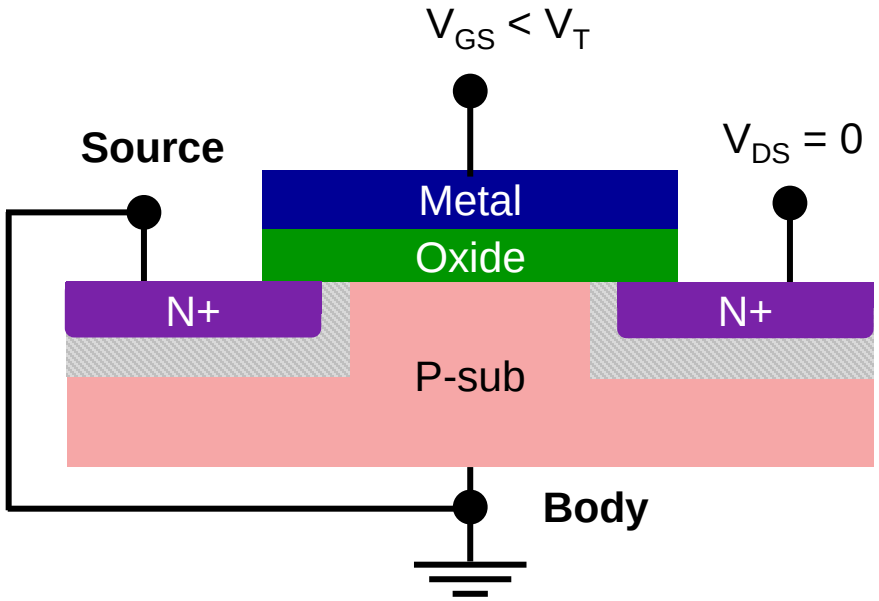


- Depletion regions at PN junctions blocks any current flow

- Channel is formed (inverted to n-type at surface)
- Regardless, there will be no current flow as potential drop along the channel is zero (V_{DS})

I_D-V_G Characteristics





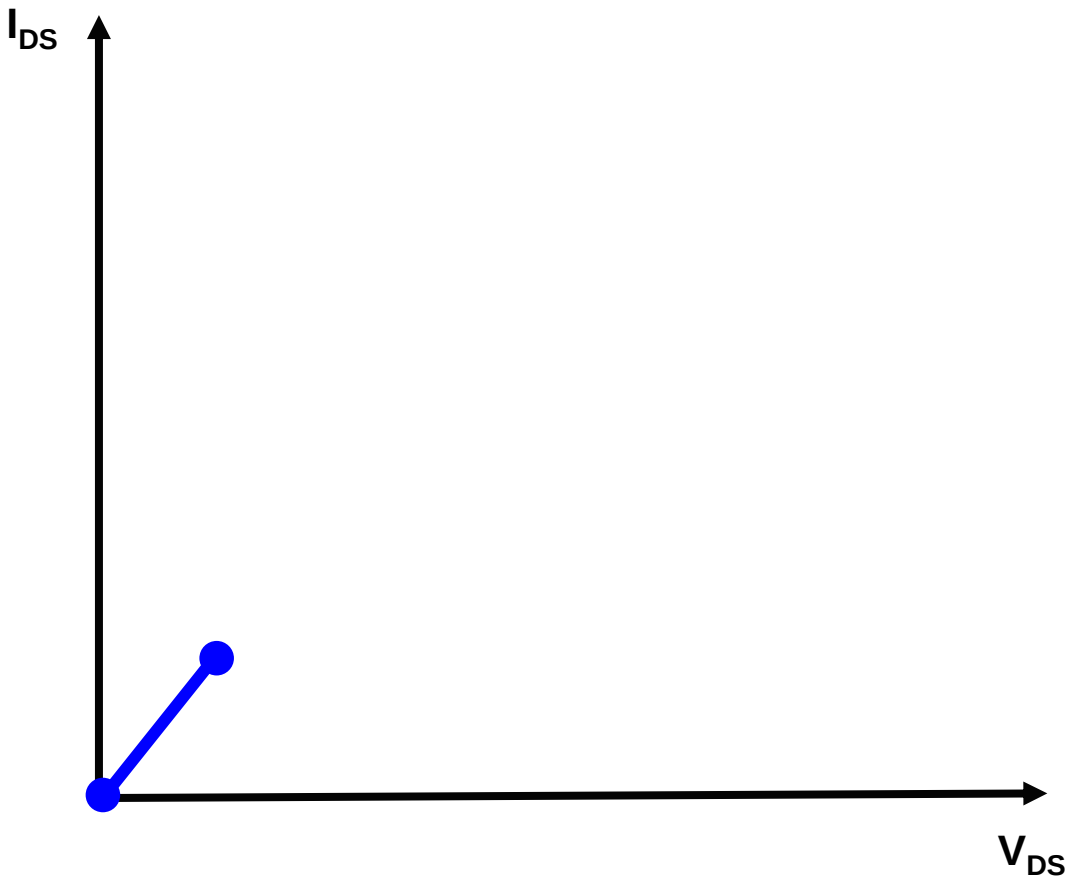
$V_{GS} < V_T$

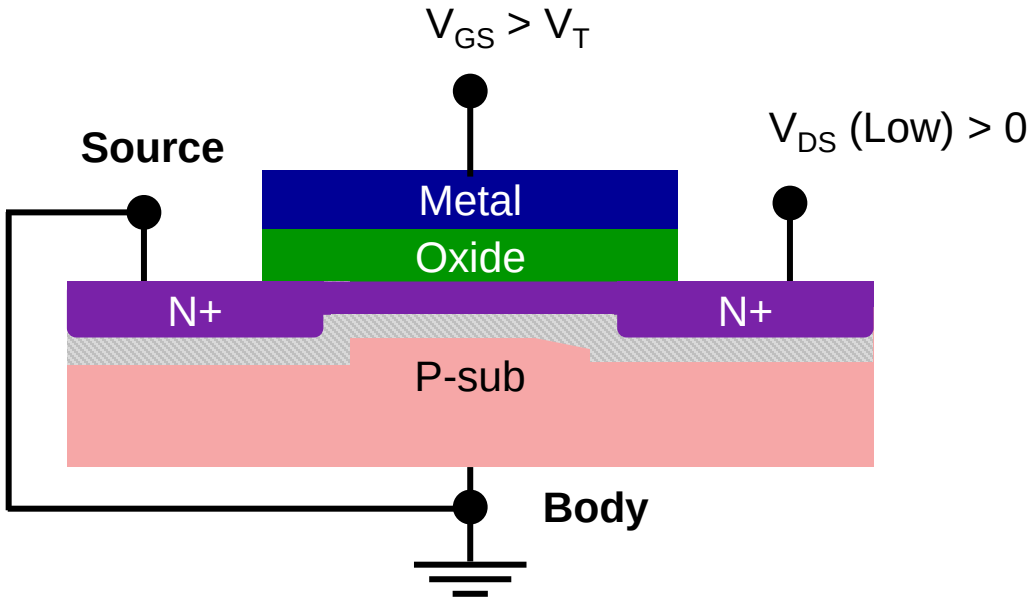
- No channel formation

$$Q_{Inv} = -C_{Ox}(V_G - V_T)$$

Gate Overdrive, inversion charge forms only when there is net gate overdrive

I_D-V_G Characteristics

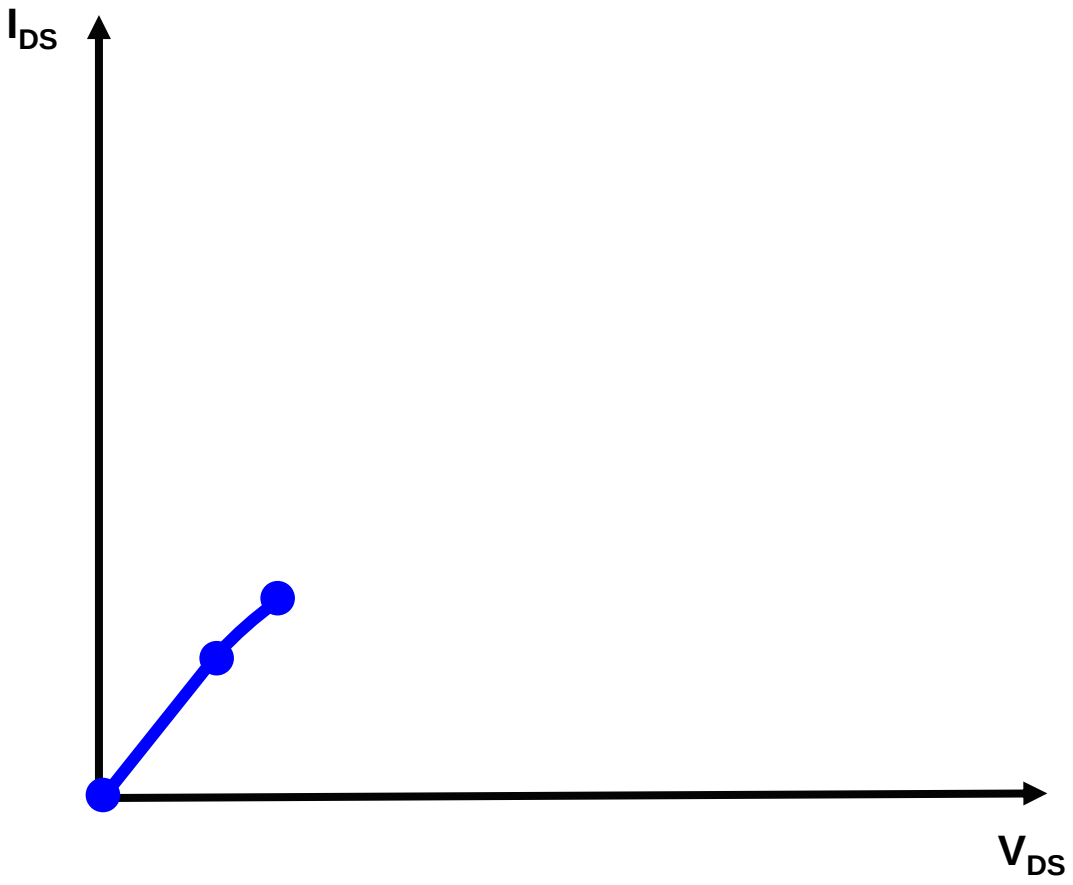


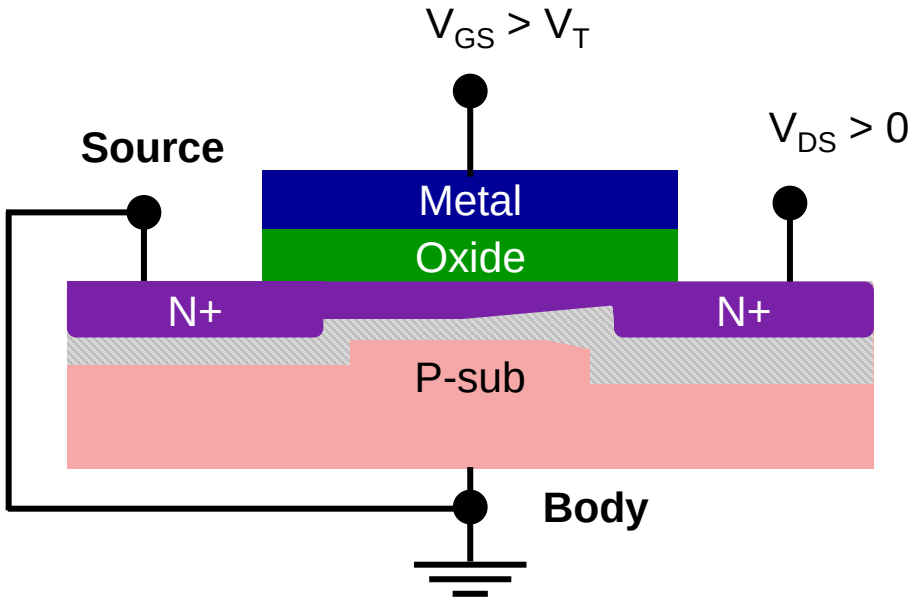


Low V_{DS}:

- Ohmic/Linear region (thin sheet of conductor)
- MOSFET acts as a resistor, follows Ohms law (V=IR)

I_D-V_G Characteristics





Moderate V_{DS}:

- Potential is increasing from S→D
- Drain side is increasingly reverse biased, depletion region width increases from S→D
- I_{DS} will increase but not at the same rate as before

$$Q_M = Q_{Inv} \downarrow + Q_{Dep} \uparrow \qquad I_{DS} = \frac{V_{DS} \uparrow}{R_{ch} \uparrow}$$

I_D-V_G Characteristics

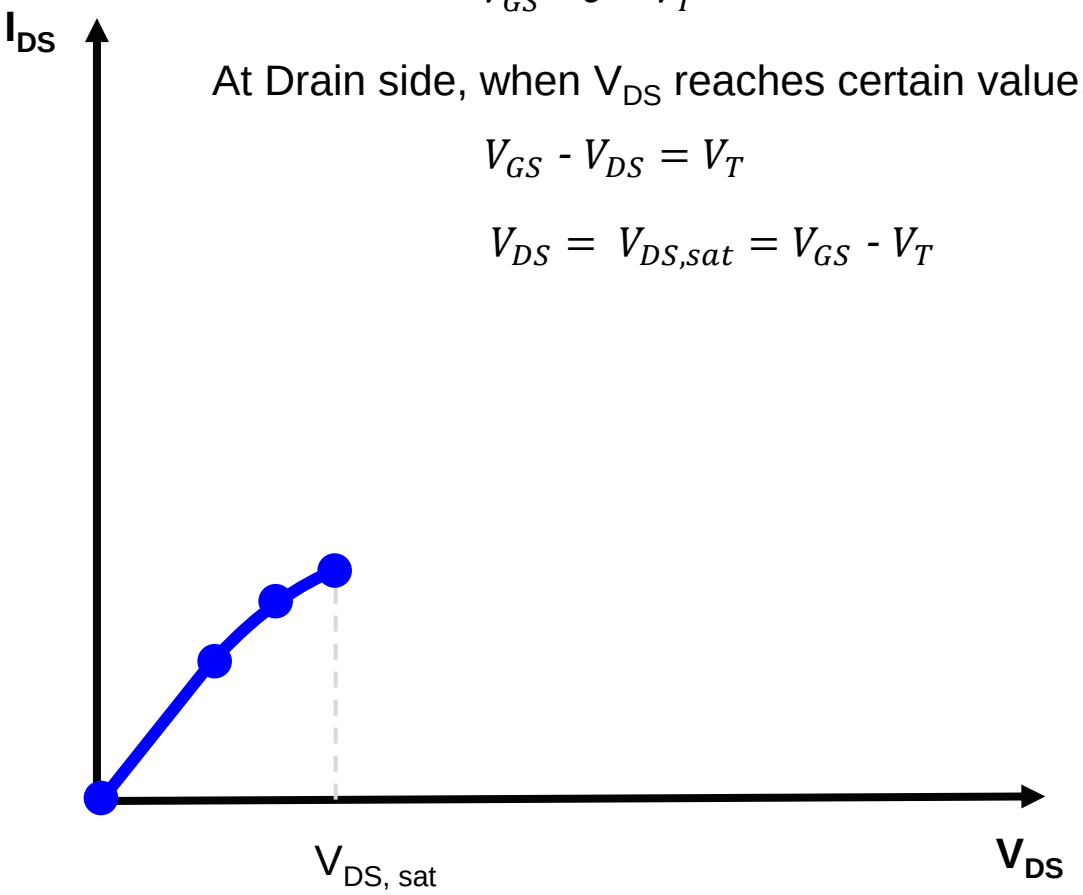
At source side

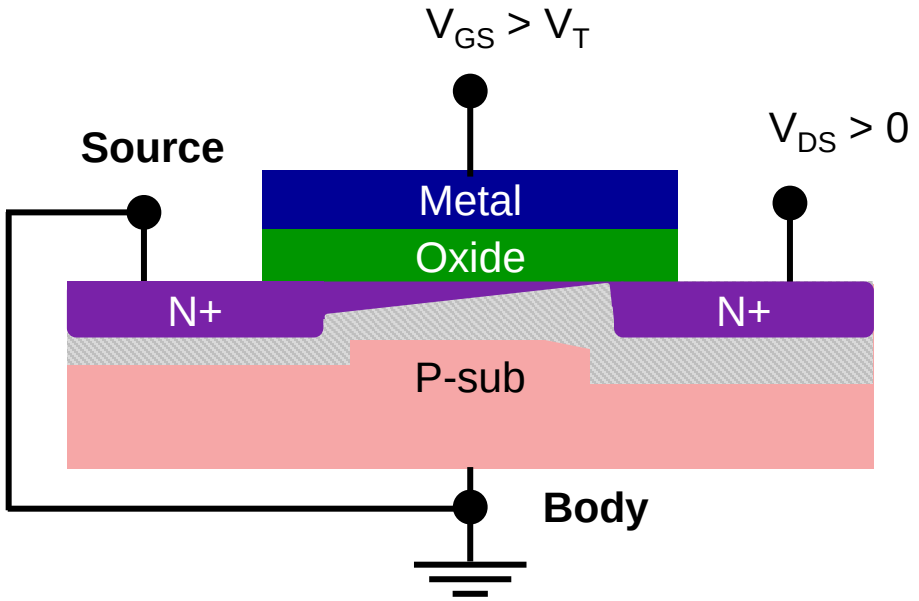
$$V_{GS} - 0 > V_T$$

At Drain side, when V_{DS} reaches certain value, $V_{DS,sat}$

$$V_{GS} - V_{DS} = V_T$$

$$V_{DS} = V_{DS,sat} = V_{GS} - V_T$$



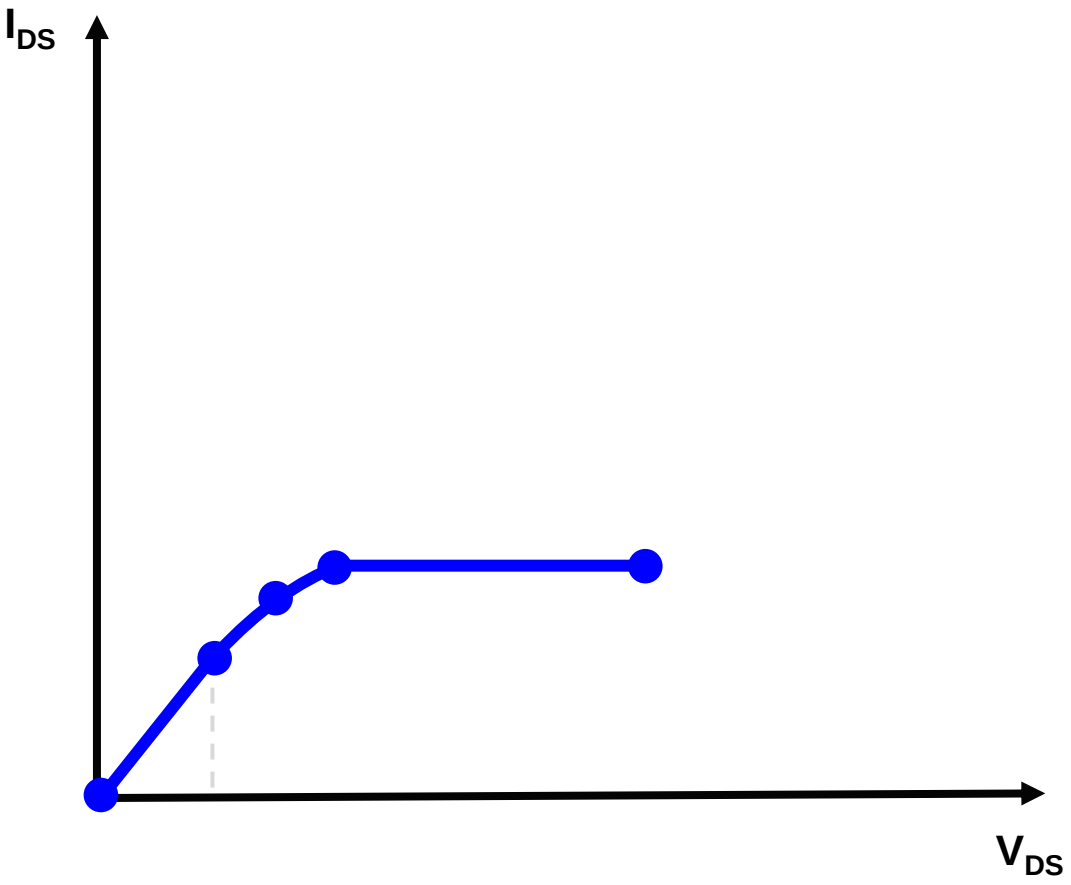


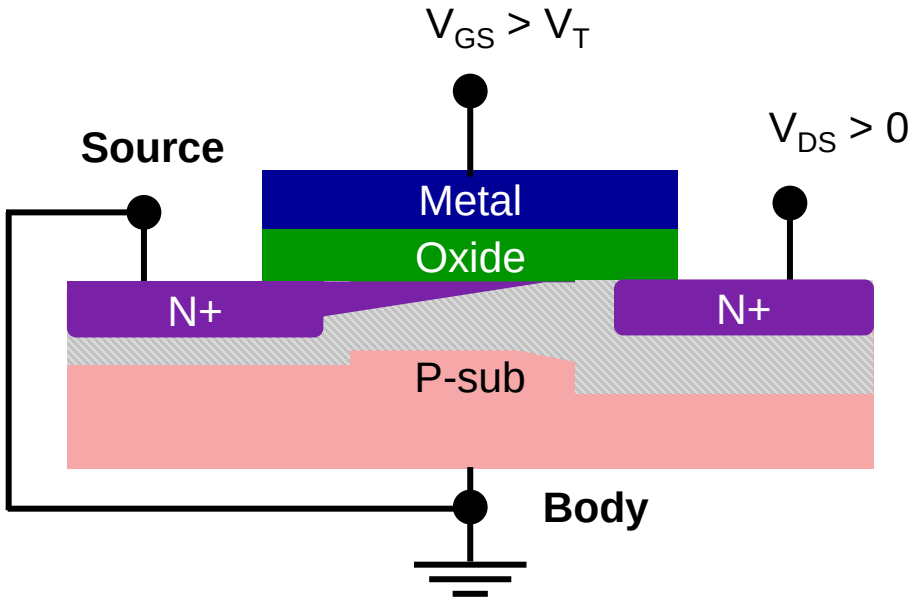
High V_{DS} (Pinch-off point):

- When $V_{DS} = V_{GS} - V_T$, channel is pinched off, no channel formation at drain edge, channel current saturates beyond this point

$$|Q_M| = Q_{Inv} \downarrow + Q_{Dep} \uparrow$$

I_D-V_G Characteristics





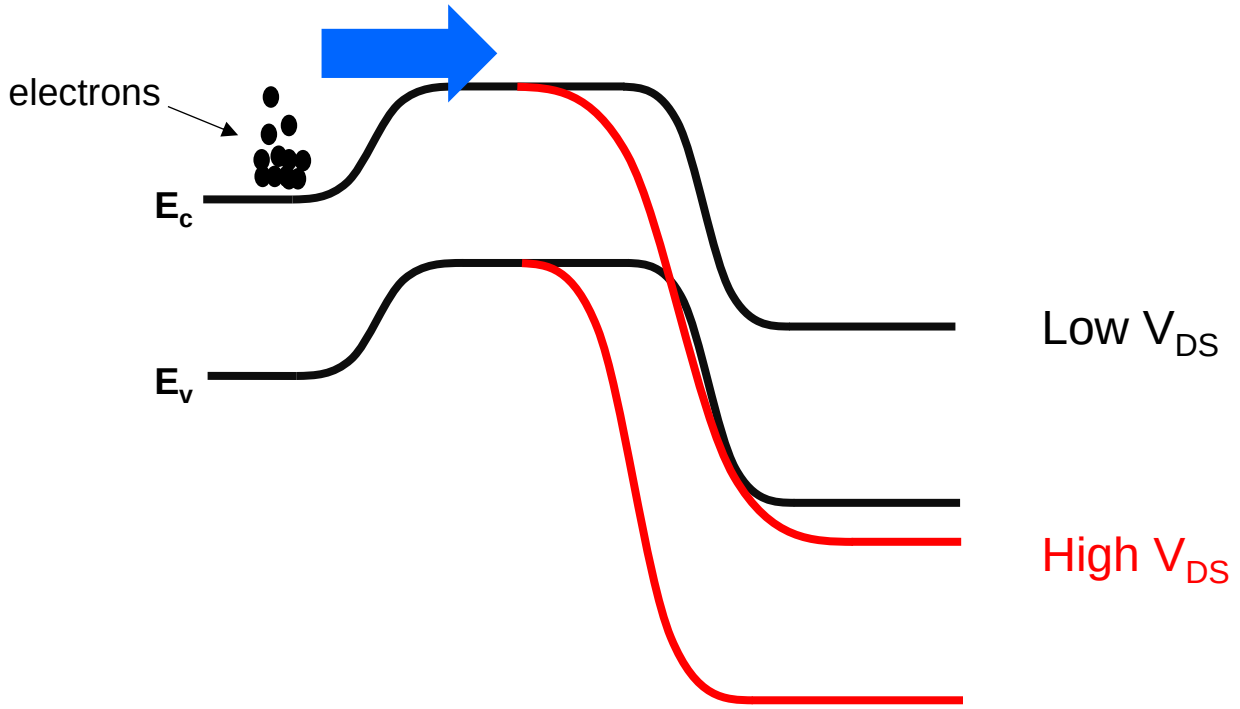
Very high V_{DS} :

- When $V_{DS} > V_{GS}$ - V_T, channel formation further reduces, channel current does not increase further, reaches saturation

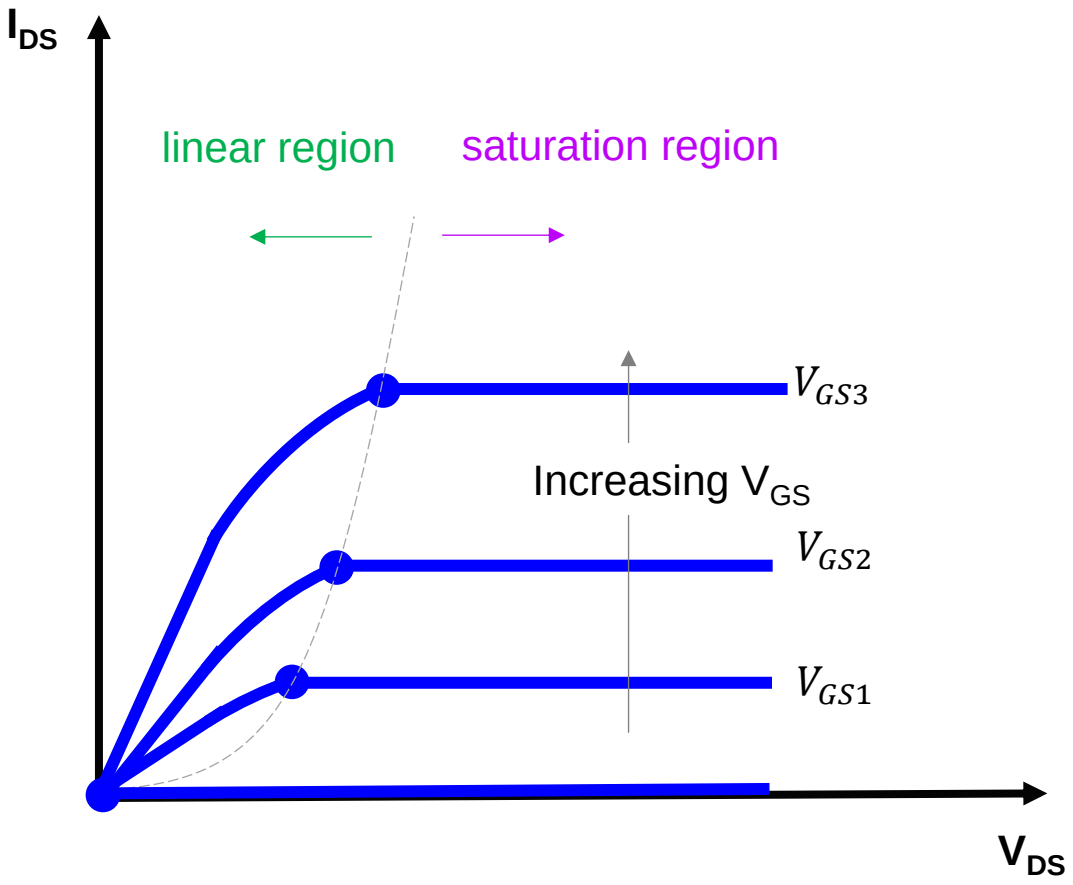
$$|Q_M| = Q_{Inv} \downarrow + Q_{Dep} \uparrow$$

Why channel current saturates?

- Current is controlled by the rate of electron emission from the source into the channel
- Electrons are swept by large electric field at pinch off/depletion region
- Current becomes independent of drain voltage in the saturation region



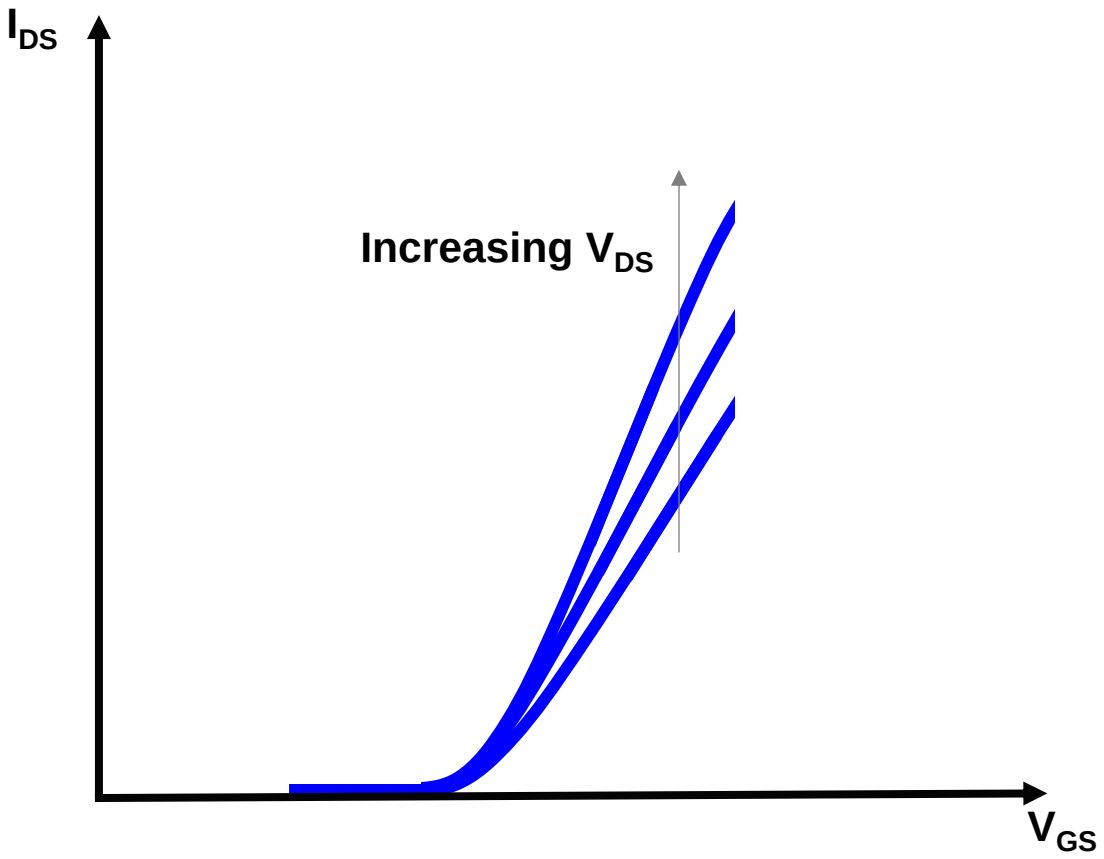
I_D-V_G Characteristics



Linear (triode) region $V_{DS} < V_{GS} - V_T$

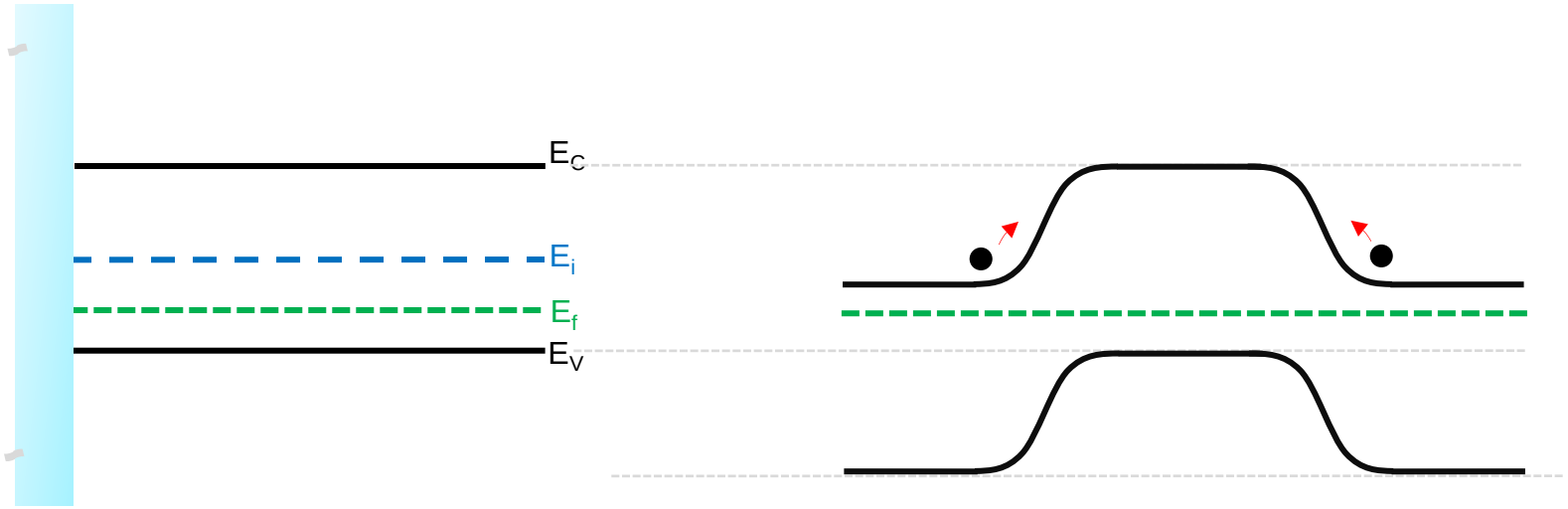
Saturation region $V_{DS} > V_{GS} - V_T$

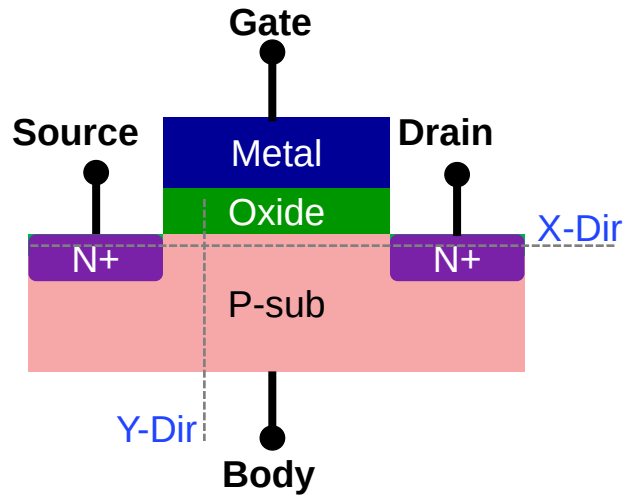
I_D-V_G Characteristics



Flat Band

V_{GS} = 0V, V_{DS} = 0V





Y-Dir

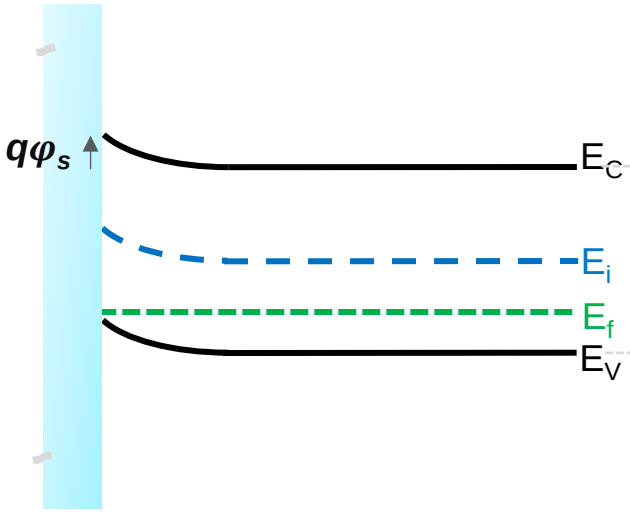
X-Dir

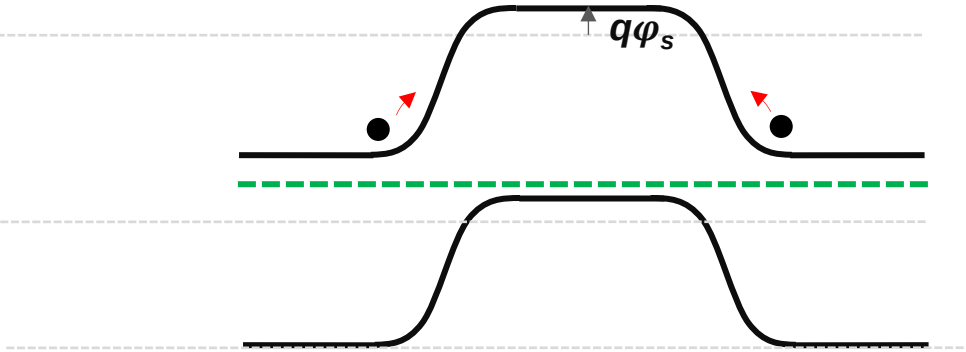
$\varphi_s = 0$

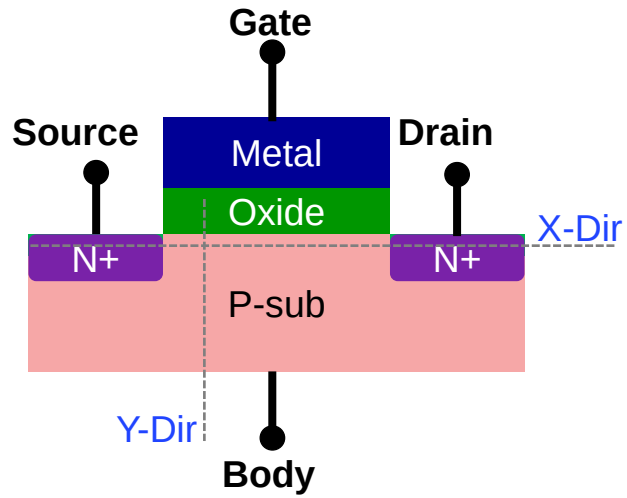
Large barrier for electrons to diffuse

Accumulation

$V_{GS} < 0V, V_{DS} = 0V$







Y-Dir

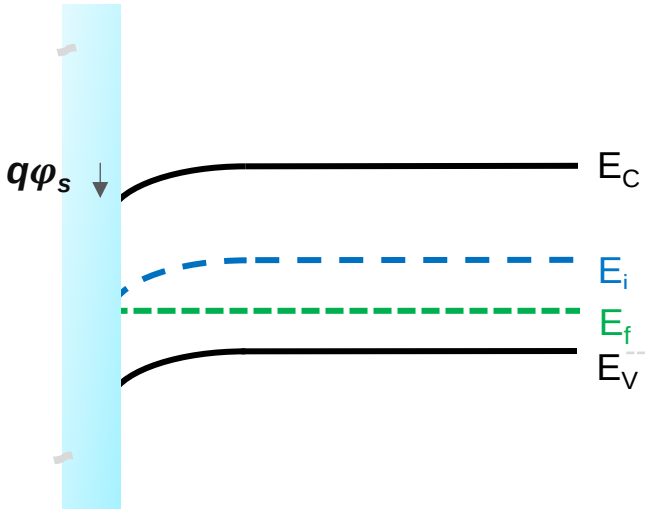
X-Dir

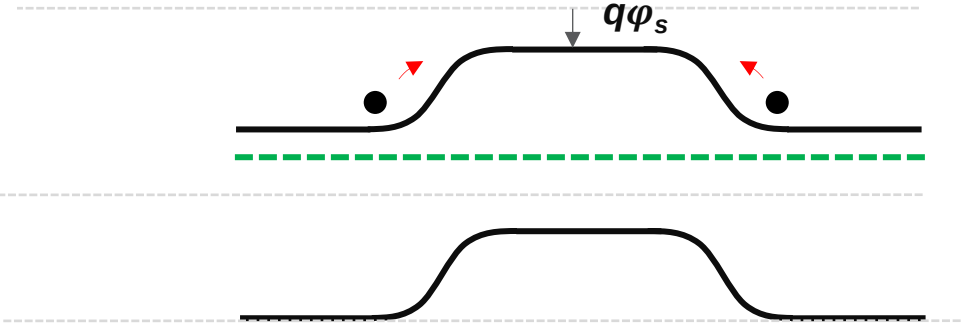
$\varphi_s < 0$

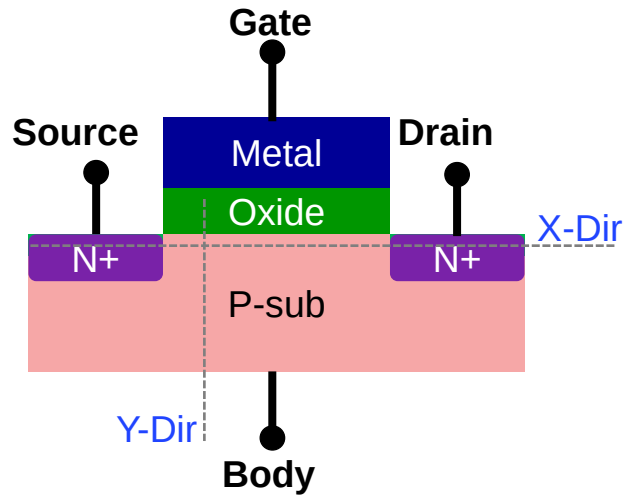
Large barrier for electrons to diffuse

Depletion

$V_{GS} > 0V, V_{DS} = 0V$







Y-Dir

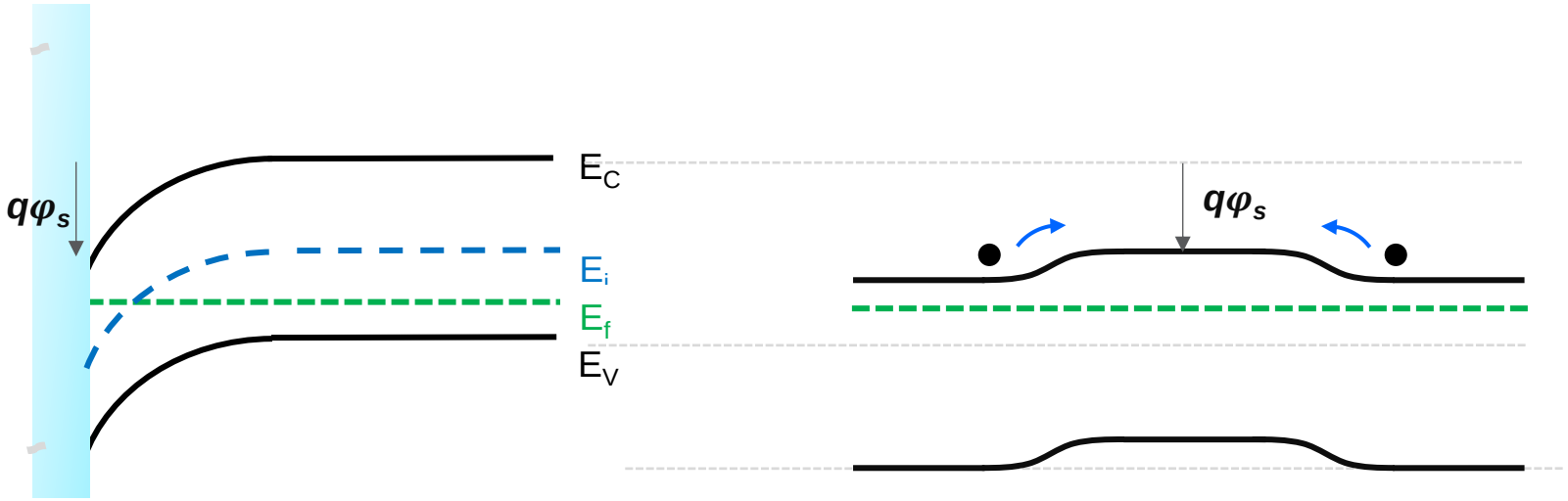
X-Dir

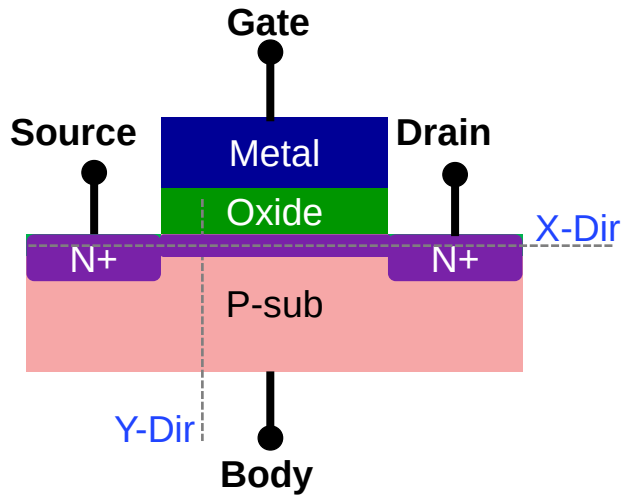
$\varphi_s > 0$

Large barrier for electrons to diffuse

Inversion

$V_{GS} > V_T$, $V_{DS} = 0V$





Inversion (onset of strong inversion)

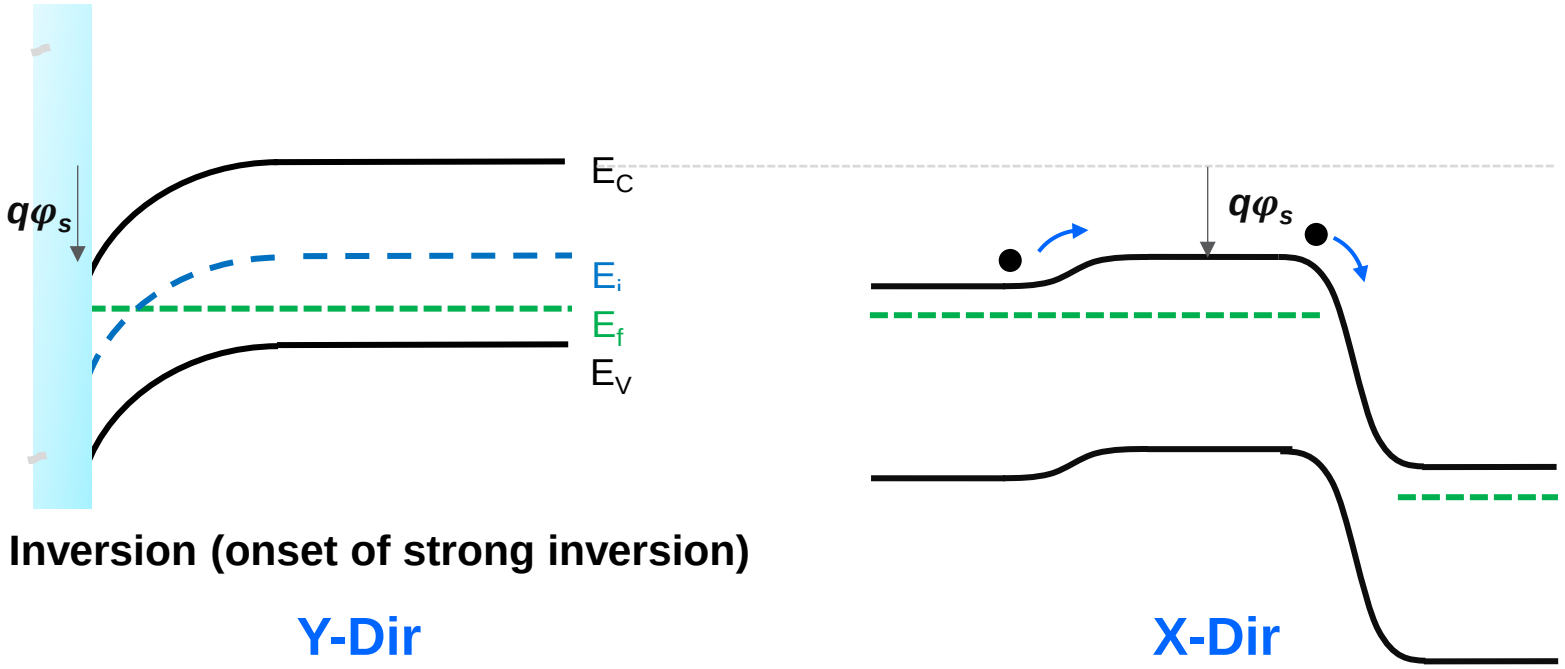
Y-Dir **X-Dir**

$\varphi_s = 2\emptyset_b$

Barrier is reduced, no net current as potential drop along the channel is zero

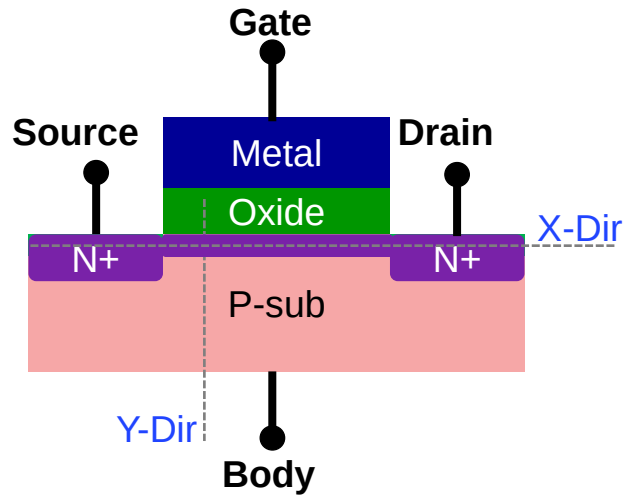
Inversion + V_{DS} ↑

$V_{GS} > V_T$, $V_{DS} = 0V$



Inversion (onset of strong inversion)

Y-Dir **X-Dir**

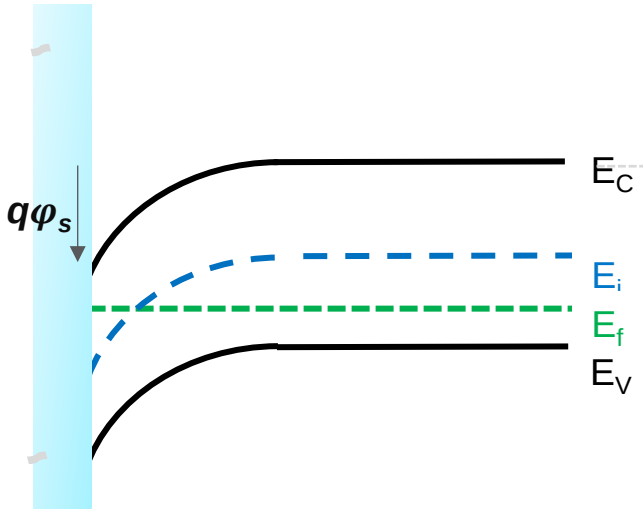


$\varphi_s = 2\emptyset_b$

Thermionic injection at source (diffusion) over potential barrier and then drift towards at the drain edge

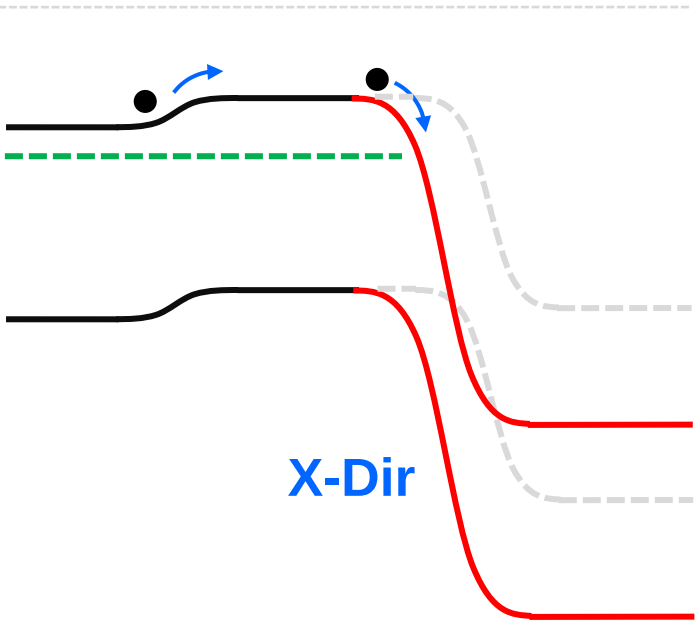
Pinch Off

$V_{GS} > V_T$, $V_{DS} = V_{GS} - V_T$

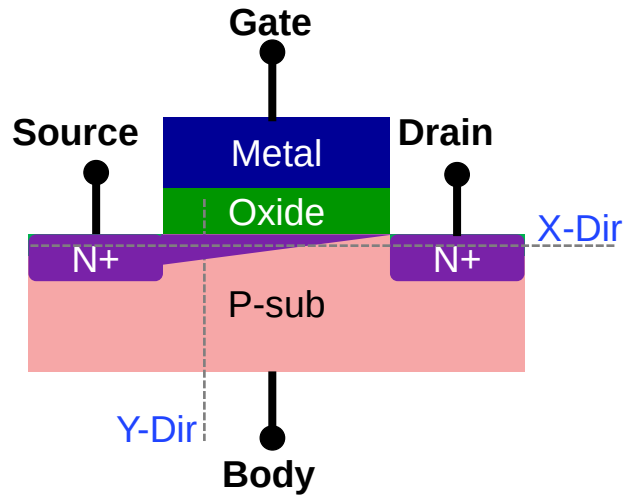


Inversion (onset of strong inversion)

Y-Dir



X-Dir

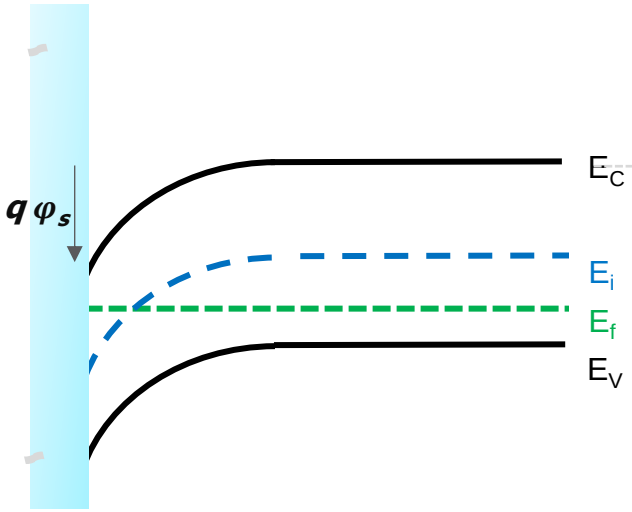


$\varphi_s = 2\emptyset_b$

Channel is pinched off, large electric field at drain side swept the electrons to drain

Saturation

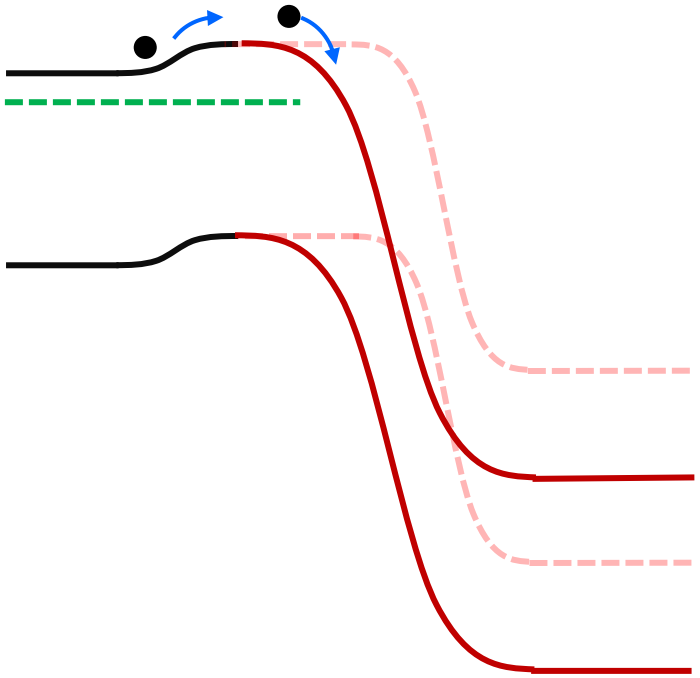
$V_{GS} > V_T, V_{DS} > V_{GS} - V_T$

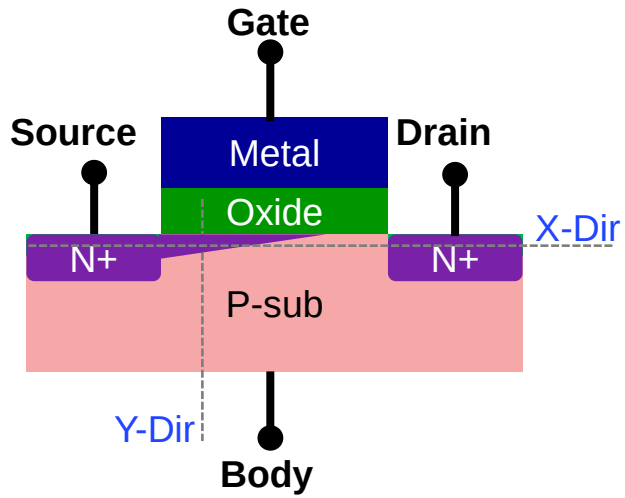


Inversion (onset of strong inversion)

Y-Dir

$$\varphi_s = 2\emptyset_b$$





Channel formation further reduces, channel current does not increase further, reaches saturation

MOSFET
Non-Ideal Effects

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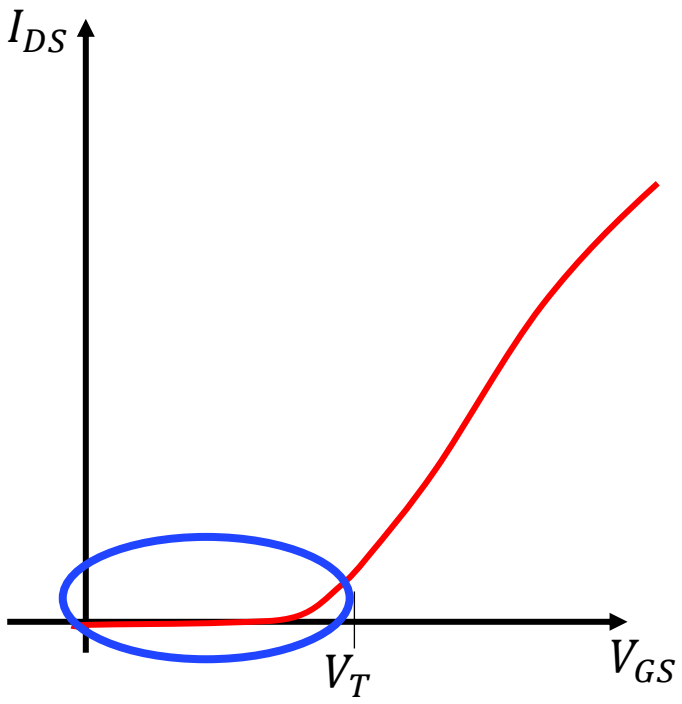
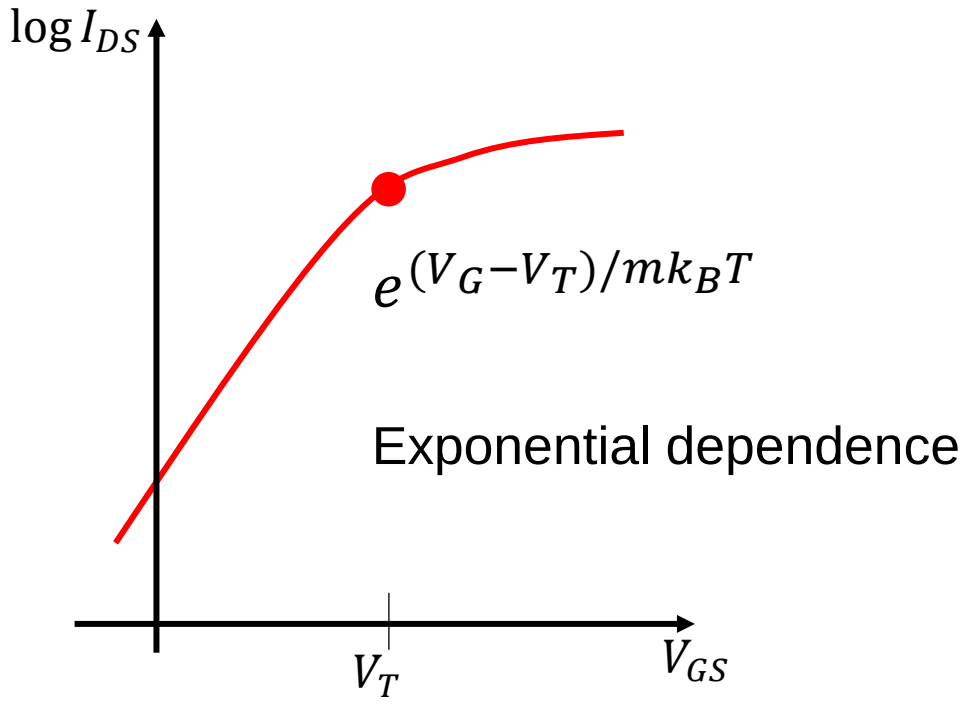
MOSFET Non-Ideal Effects

1. Subthreshold Leakage
2. Drain Induced Barrier Lowering (DIBL)
3. Gate Induced Drain Leakage (GIDL)

I_D-V_G Characteristics

Linear vs Log Scale

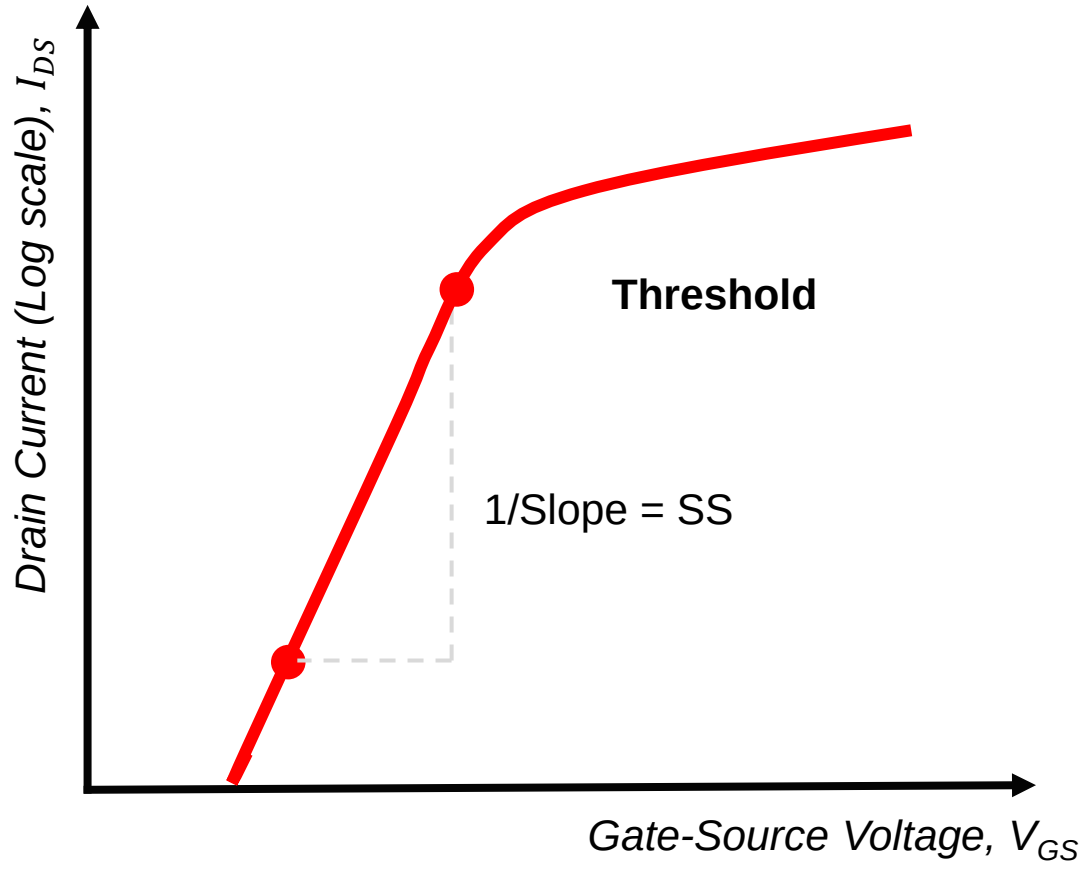




- It appears the subthreshold region is linear in log scale [i.e: ln e^x = x]
- This implies, subthreshold conduction (leakage) before V_T (threshold) is exponential in real nature

Subthreshold Conduction

Subthreshold Slope/Swing (SS)

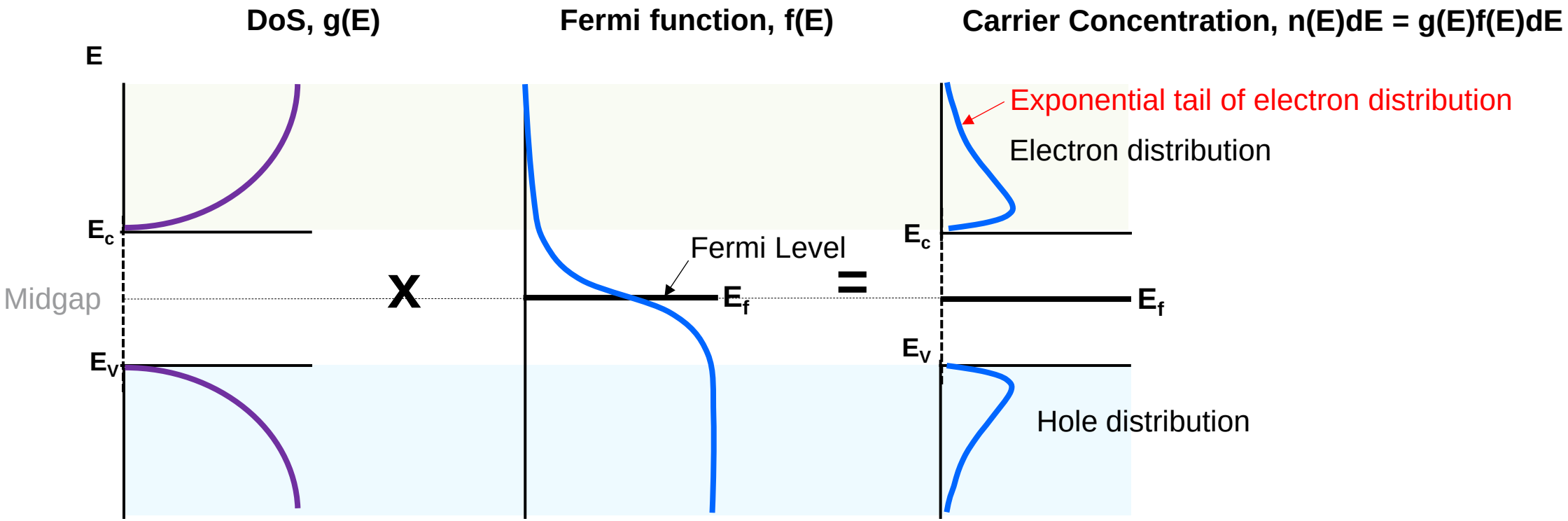


- SS: The gate voltage required to increase or reduce I_{DS} by one decade
- SS is given by the inverse of the slope of $\log I_{DS}$ vs V_{GS}

$$SS = \left[\frac{d\log I_{DS}}{dV_{GS}}\right]^{-1} [\text{unit: mv/dec}]$$

- Note that SS > 60mV/dec at room temperature (Why? Answer in next two slides

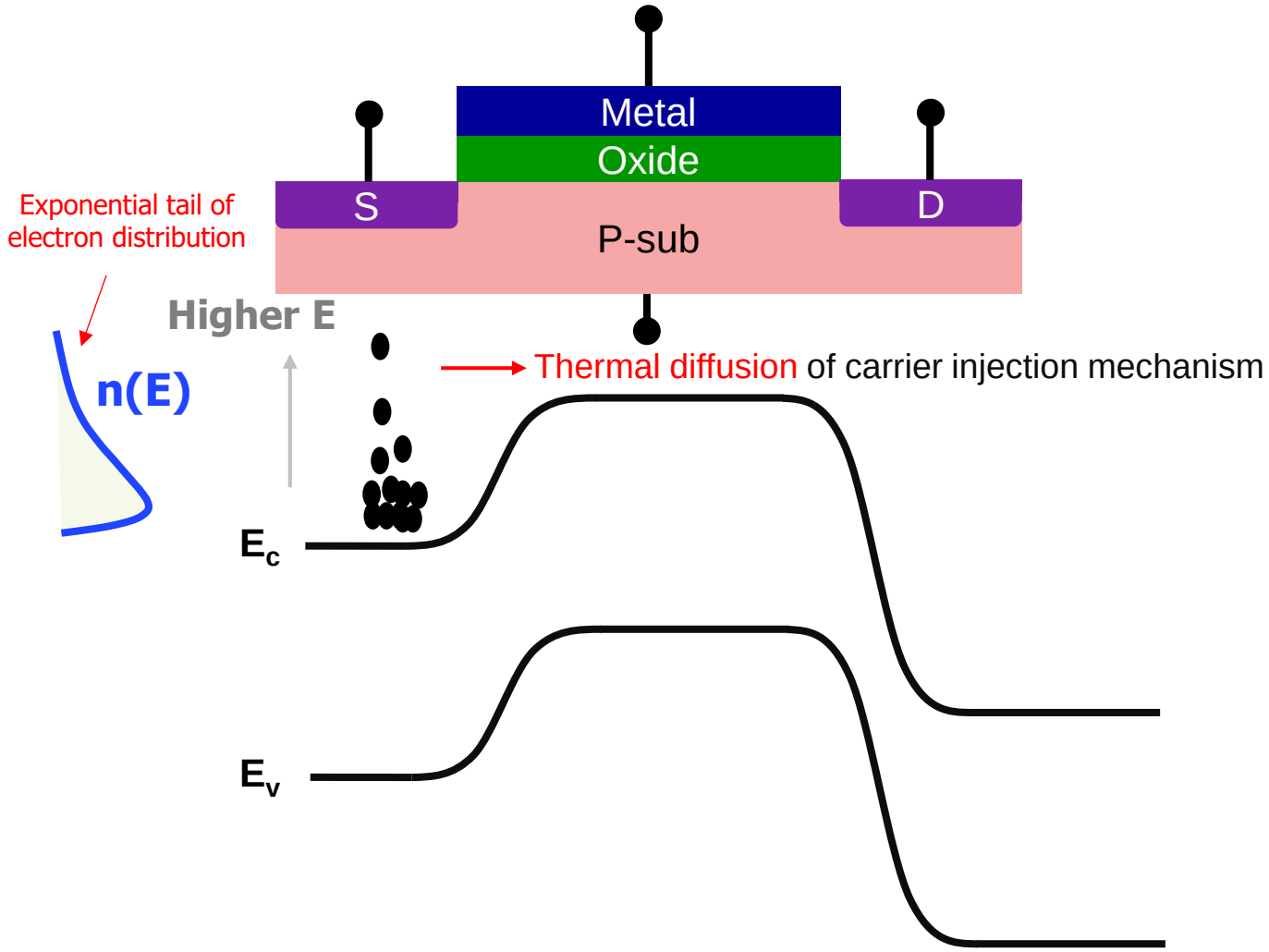
Carrier Distribution

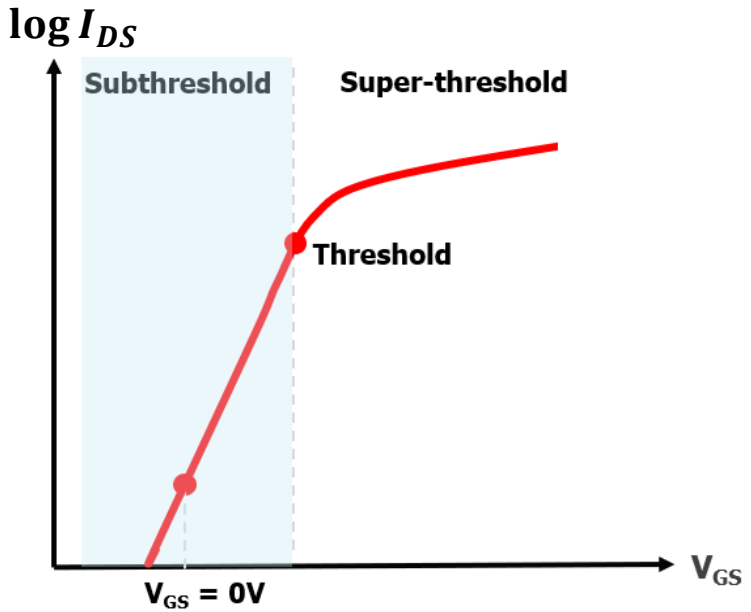


$$f(E) = \frac{1}{1 + e^{(E - E_f)/kT}}$$

MOSFET Operation [OFF State]

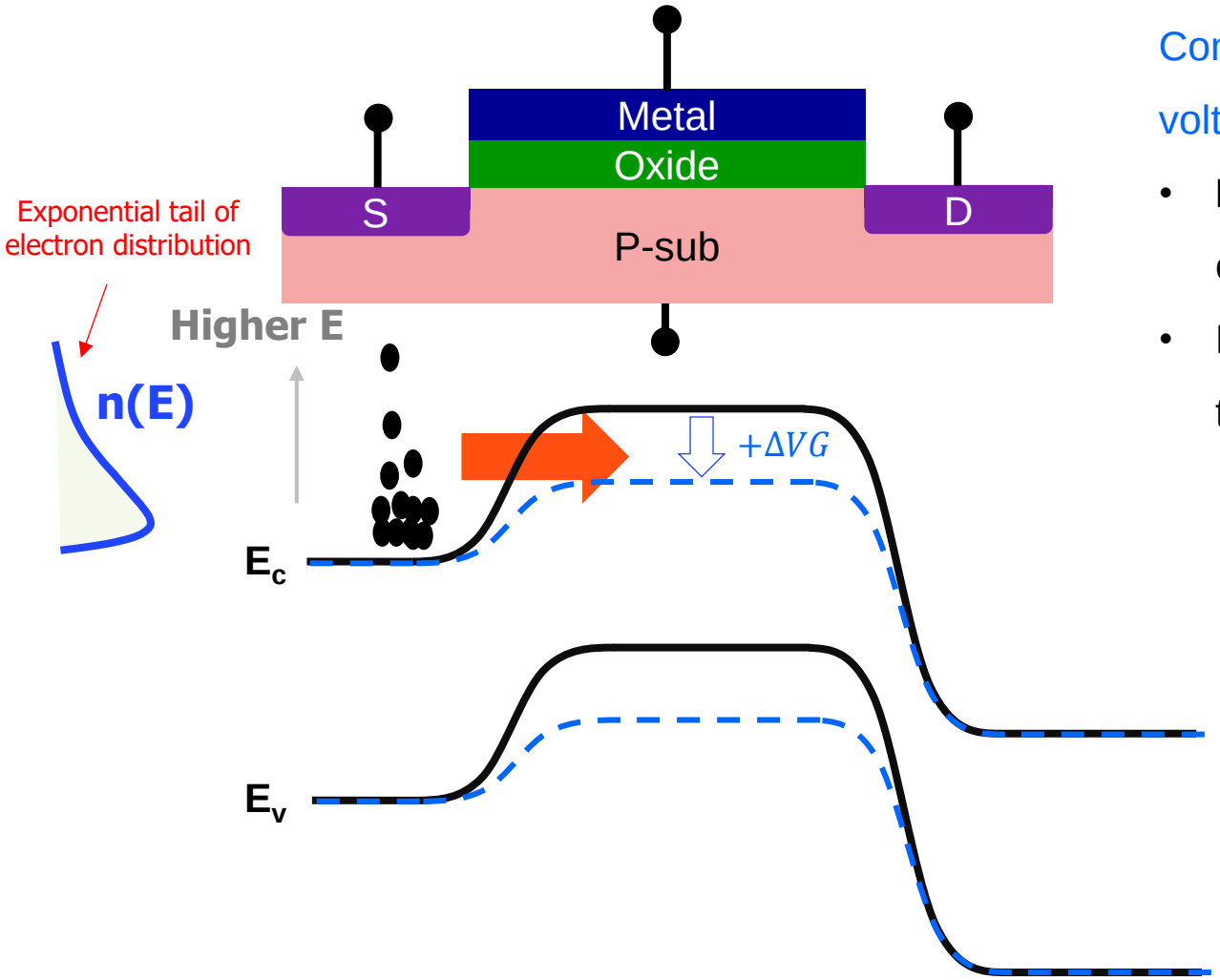
OFF is not completely OFF!





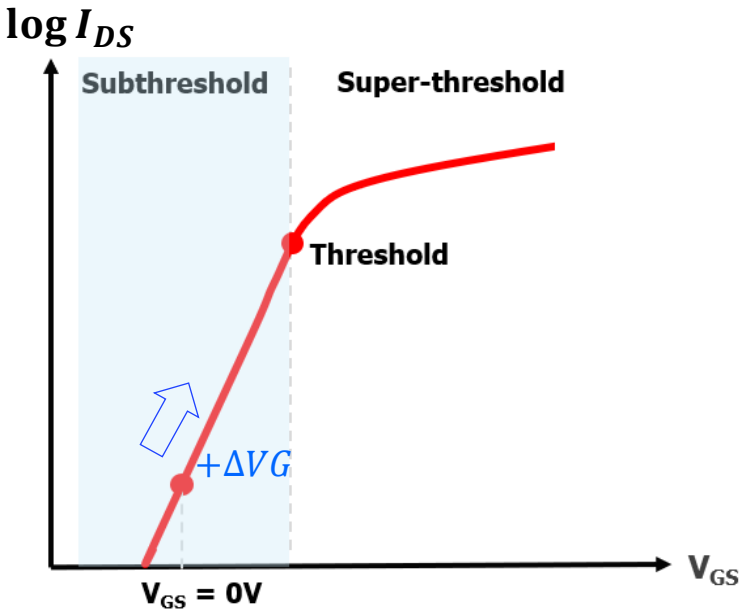
MOSFET Operation [OFF State → Increasing V_{GS}]

Why subthreshold slope is linear in log scale? (Exponential in linear scale)

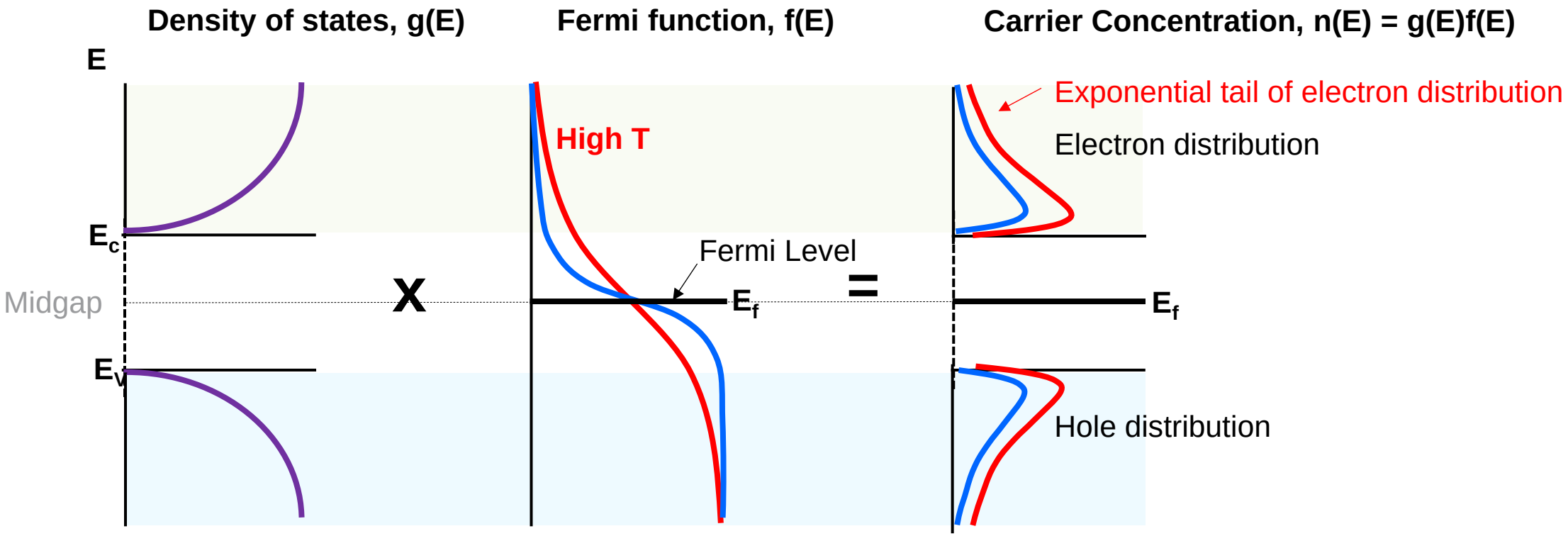


Consider a hypothetical scenario, a minor increase in the gate voltage (within the subthreshold region) can lead to:

- **Revealing exponentially increasing** tail distribution of electrons at the source
- Result in significant rise in the rate of thermionic diffusion from the source



Carrier Distribution [Low T vs High T]

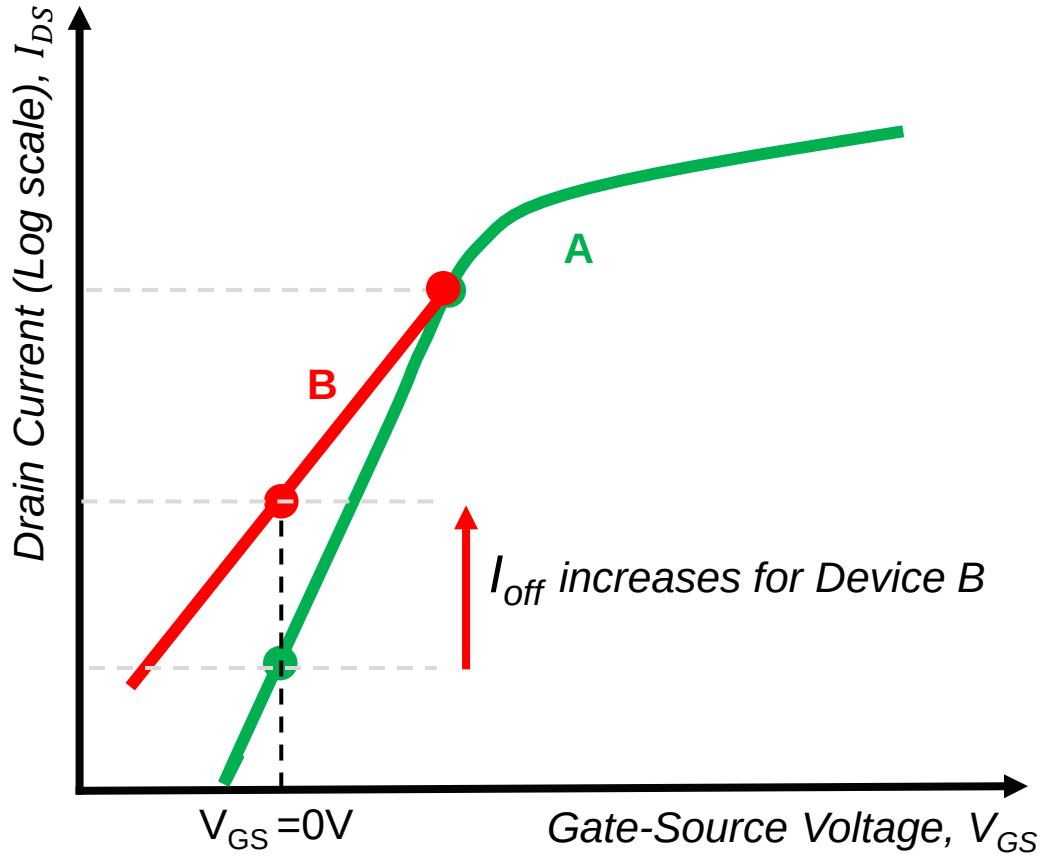


$$f(E) = \frac{1}{1 + e^{(E - E_f)/kT}}$$

Higher temperature results in larger amount of electron exponential tail distribution exposed at source which increases subthreshold leakage

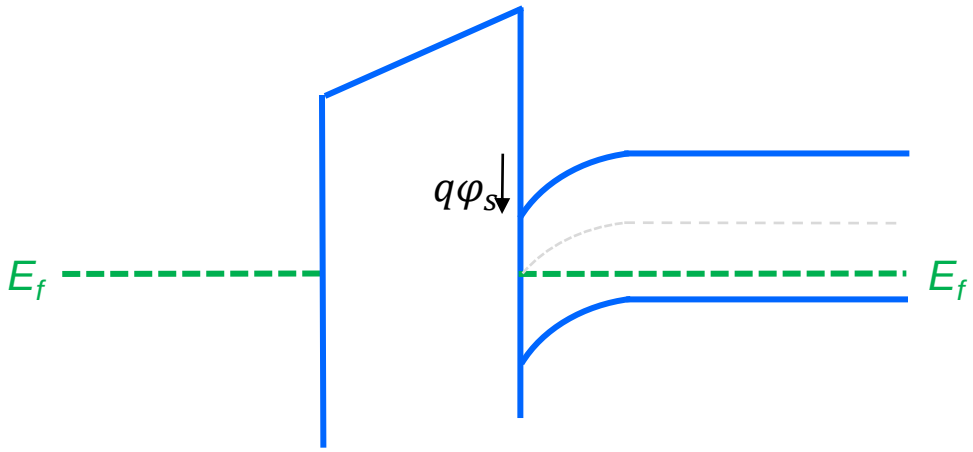
Subthreshold Leakage

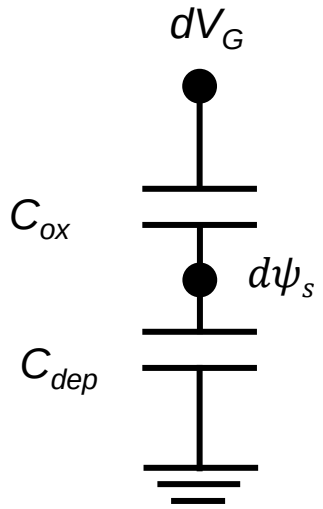
Poor vs Good Subthreshold Slope

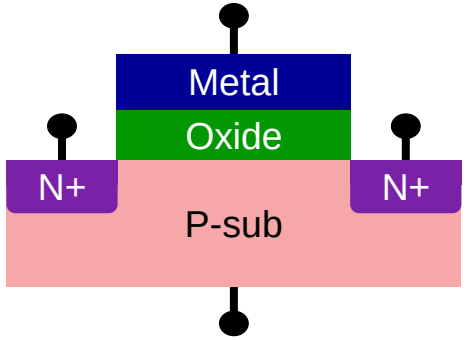


- Device B exhibits a poorer (larger) subthreshold slope (SS) compared to device A, despite having matched V_T
- Smaller SS (steeper slope) is necessary to minimize the OFF-state leakage
- Question: What methods can be employed to reduce SS, and what is the minimum achievable value?
- Answer will be provided on the following slide

Subthreshold Leakage







$$\frac{d\varphi_S}{dV_{GS}} = \frac{C_{ox}}{C_{ox}+C_{dep}} = \frac{1}{n}$$

$$n = 1 + \frac{C_{dep}}{C_{ox}}$$

$$d\varphi_S = \frac{dV_{GS}}{n}$$

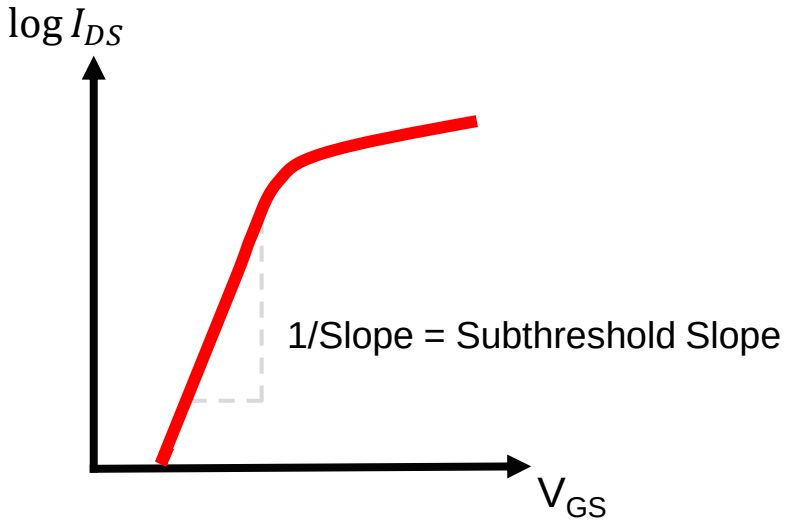
$$\varphi_S = Constant + \frac{V_{GS}}{n}$$

$$I_{DS} \propto n_s \propto exp\left(\frac{q\varphi_s}{kT}\right) \propto exp\left(\frac{q[Constant+\frac{V_{GS}}{n}]}{kT}\right) \propto exp\left(\frac{qV_{GS}}{nkT}\right)$$

$$d\ln I_{DS} = \frac{qdV_{GS}}{nkT}$$

$$2.3d\log I_{DS} = \frac{qdV_{GS}}{nkT}$$

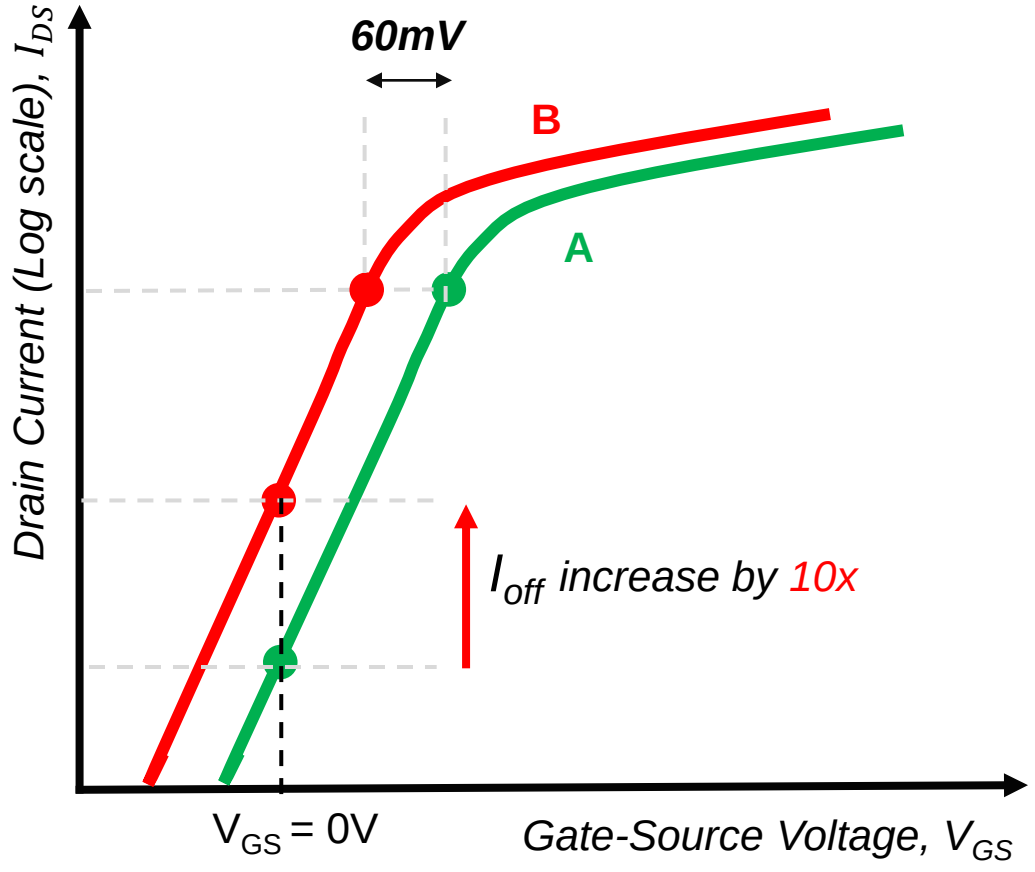
$$SS = \left[\frac{d\log I_{DS}}{dV_{GS}}\right]^{-1} = 2.3^* \frac{\mathrm{kT}}{\mathrm{q}}{}^*\mathrm{n} = 2.3^* \frac{kT}{q}\left[1 + \frac{C_{dep}}{C_{ox}}\right] = 60^*\left[1 + \frac{C_{dep}}{C_{ox}}\right] mV/dec$$



SS has minimum theoretical value of 60mV/decade at room temperature

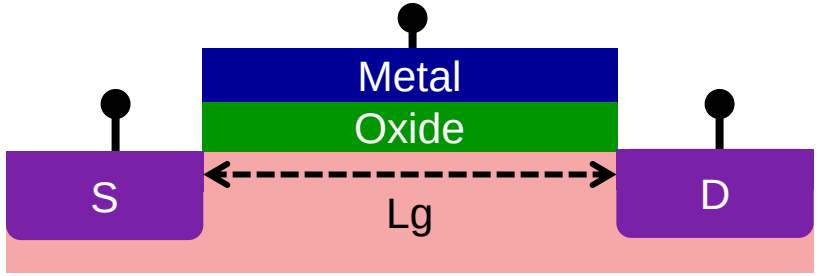
Subthreshold Conduction [Lowering V_T]

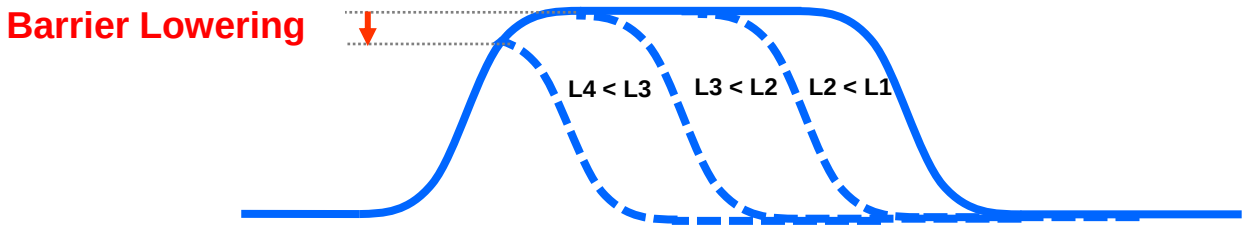
Why it matters, what is the issue with non-scalability of SS?



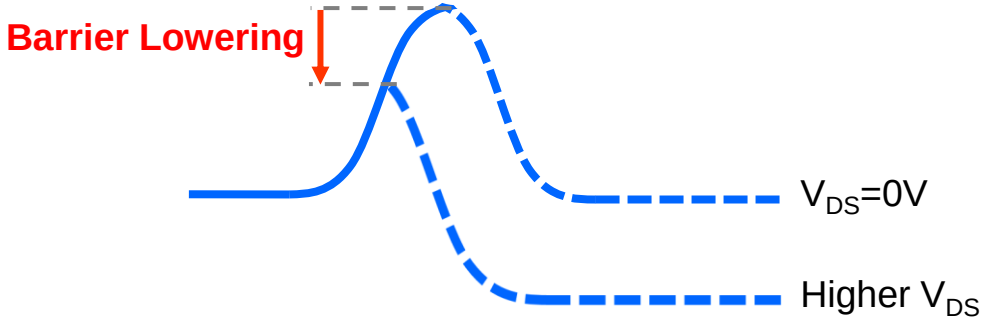
- Both Device A & B have similar SS (i.e: 60mV/decade)
- However, device B shows 10x increase in leakage for 60mV V_T reduction
- Non-scalability of SS increases standby power (static power)
- To reduce dynamic power ➔ V_{DD} and hence V_T needs to be scaled. Scaling V_T by 60mV increases **I_{off} by 10x**

Drain Induced Barrier Lowering [DIBL]



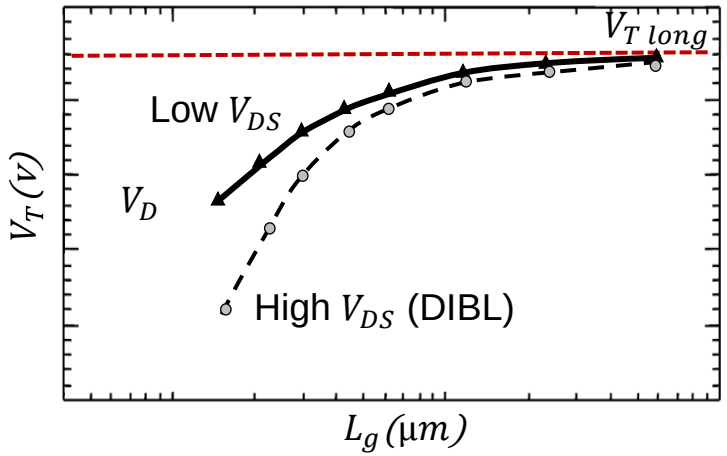


Field encroachment from drain, lowering electron injection barrier at source, worse impact at short gate length (at V_{DS}=0)

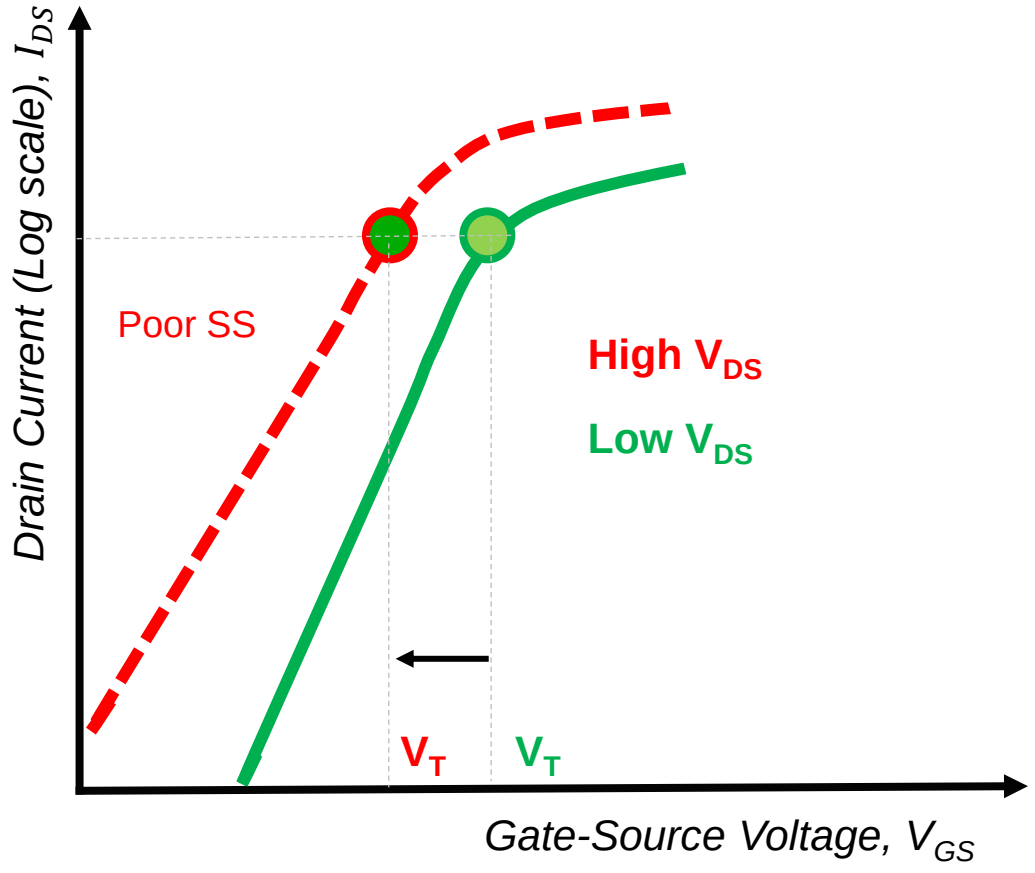


Barrier is further lowered with high V_{DS}

- Field encroachment from the drain reduces the electron injection barrier at the source, leading to V_T lowering that is influenced by:
  - Shorter channel (gate) length (Lg)
  - Elevated V_{DS}
- Gate is losing control over the channel as the drain exerting more influence
- This scenario also leads to an increase in I_{off} and deterioration of the subthreshold slope/swing (SS)



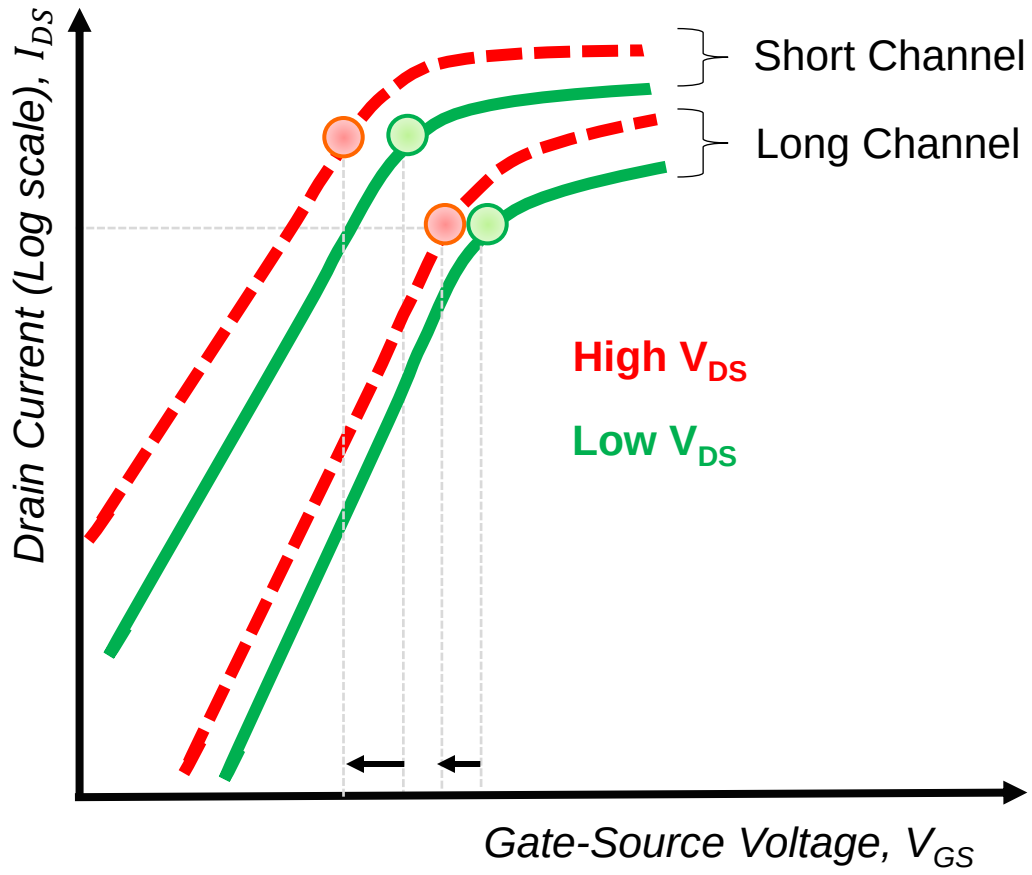
DIBL [V_{DS} Impact]



- DIBL reduces V_T at elevated V_{DS} levels
- DIBL Coefficient = Delta V_T/Delta V_{DS}
  - Unit: mV/V
  - Quantifies V_T lowering per unit increase in $V_{DS,}$ ideal case is zero
- DIBL degrades SS (larger)

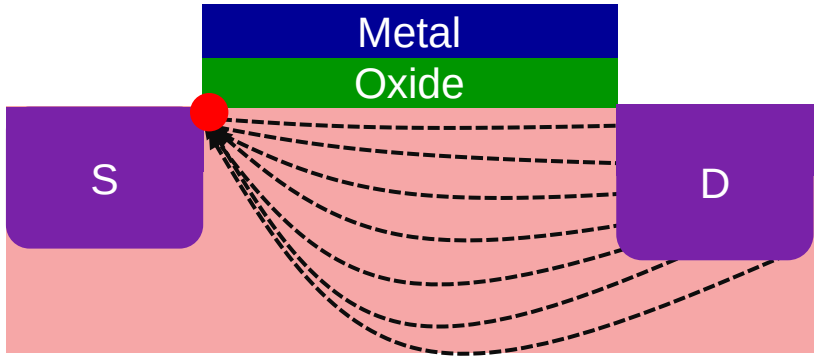
DIBL [V_{DS} Impact and Short vs Long Channel]

Short Channel Effect (SCE)

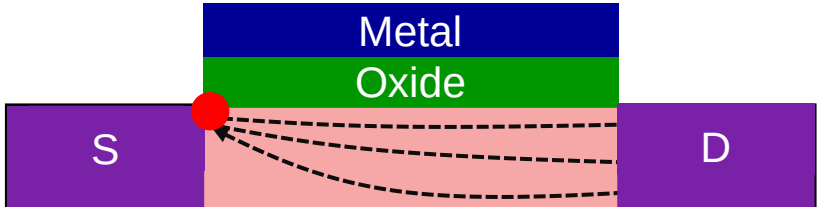


- Short channel will have larger drain electric field penetration towards source
- Short channel shows larger DIBL shift

Thin Body Channel ➔ Improves DIBL



Electric field encroachment from drain through bulk (more flux/fringing field interaction)

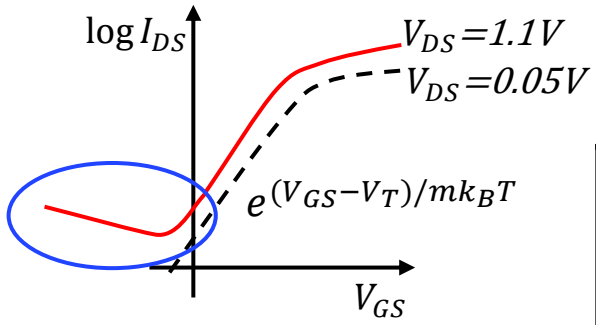


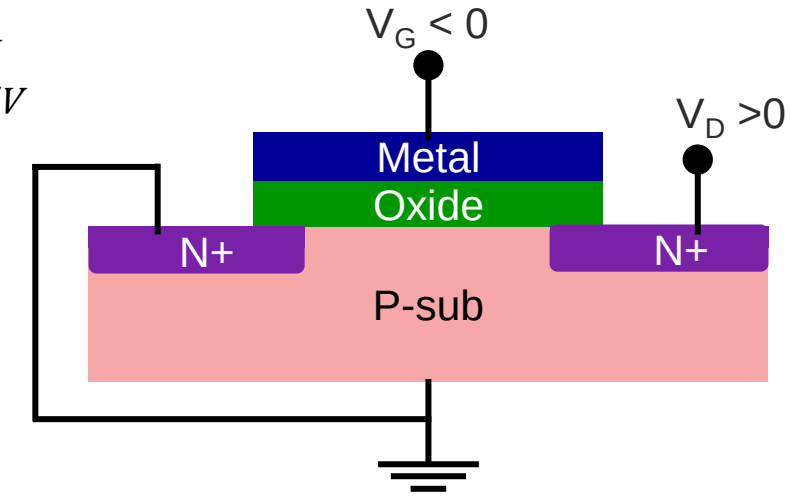
Electric field encroachment from drain is reduced significantly ➔ Better DIBL

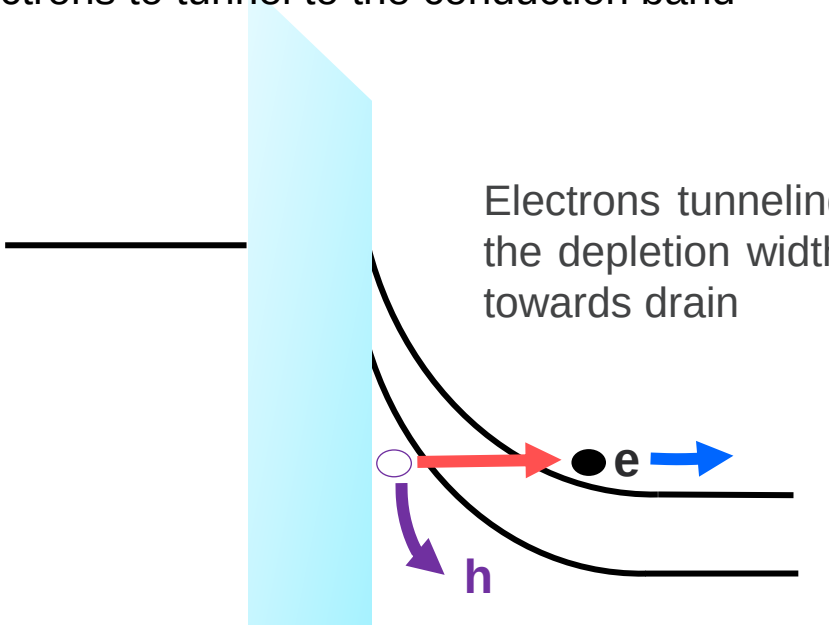
- The penetration of the electric field toward the source decreases (due to bulk encroachment) when using a thinner body
- Additional strategies to improve DIBL include
  - Shallow Source (S) /Drain (D) junctions,
  - Elevated S/D structures
  - Halo and retrograde wells implants

Gate Induced Drain Leakage (GIDL)

- GIDL typically occurs when the gate is biased to accumulation and the drain is ramped to reverse voltages
- The device is driven to deep depletion at gate-drain (N+) overlap region when gate is driven to accumulation and drain is reverse biased
- Strong vertical field across the oxide in gate-drain overlap region causes the valence band electrons to tunnel to the conduction band



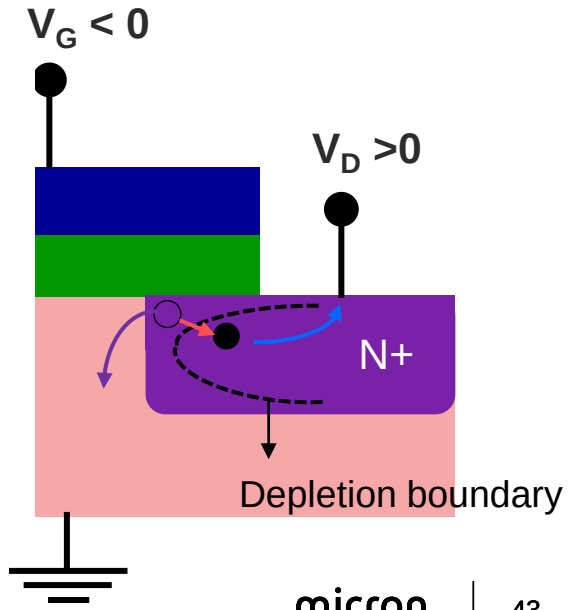




Electrons tunneling through the depletion width will flow towards drain

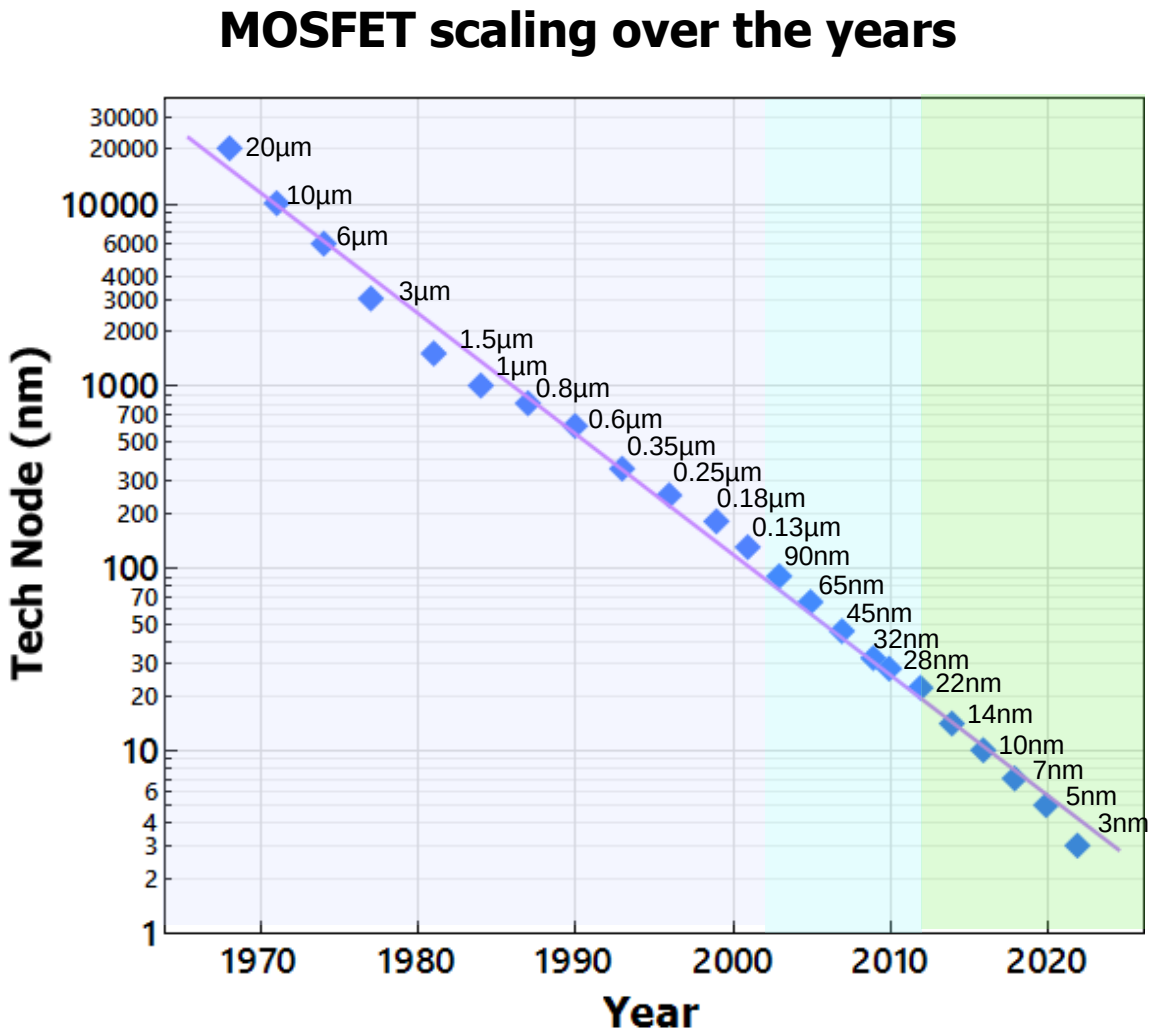
Vertical electric field at gate-drain overlap region

e-h pair generation through band-band tunneling across depletion layer



Closing Thoughts

- MOSFET is the heart of semiconductor industry
- Powerful and efficient semiconductor devices/increasing computing power is enabled by exponential increase in MOSFET counts
- **Understanding MOS technology device physics forms the basis semiconductor devices**



Glossary

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Glossary

Term or acronym	Definition/description
Accumulation	A condition in MOSCAP where the majority carriers accumulate at the surface due to the applied gate potential
Body	Bulk crystal or polycrystalline silicon region where the majority carriers accumulate, deplete or invert depending on the applied gate potential.
Conduction band	The energy band where conducting electrons occupy states close to the bottom (the conduction band edge).
Deep Depletion	A non-equilibrium condition where the depletion width becomes greater than the maximum depletion width to offset the missing minority carriers
Density of States	The number of electronic states per unit energy at each energy level that are available to be occupied by electrons
Depletion	A condition in MOSCAP where the majority carriers are repelled, exposing the depletion region
DIBL (Drain-Induced Barrier Lowering)	A short-channel effect in MOSFETs where the threshold voltage decreases as the drain voltage increases
Doping	The process of adding impurities to a semiconductor to change its electrical properties. Doping can create either n-type or p-type semiconductors
Drain	The terminal where the majority carriers exit the channel.
Gate	The metal electrode used to control the electric field and potential applied to the semiconductor body. This control influences the behavior of the majority carriers within the MOSCAP structure.
Gate overdrive	The voltage applied to the gate terminal of a MOS capacitor (MOSCAP) or MOSFET (Metal Oxide Semiconductor Field Effect Transistor) that exceeds the threshold voltage (VT). This excess voltage creates a stronger channel in the semiconductor, enhancing the device's performance
GIDL (Gate-Induced Drain Leakage)	A leakage current that occurs in MOSFETs when a high electric field is applied to the gate-drain overlap region
Inversion	A condition in MOSCAP where the surface is inverted to n-type silicon, and additional charge at the gate is equated with a surface charge at the semiconductors.

Glossary

Term or acronym	Definition/description
MOSCAP	Metal Oxide Semiconductor Capacitor. It is a two-terminal device used to understand the fundamentals of MOSFET operation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor. It is a four-terminal device used in both digital and analog applications
PN Junction	A junction formed by combining p-type and n-type semiconductors. It is the basic building block of many semiconductor devices
P-Sub (P-type substrate)	The bulk silicon region where the majority carriers (holes) accumulate, deplete, or invert depending on the applied gate potential
Source	The terminal where the majority carriers (electrons for n-type MOSFETs or holes for p-type MOSFETs) enter the channel
Subthreshold Slope/Swing (SS)	A measure of how effectively a MOSFET can switch from the off state to the on state. It is defined as the change in gate voltage required to change the drain current by one decade

References

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Reference

1. Fundamental of Modern VLSI Devices, Yuan Taur and Tak H. Ning
2. Modern Semiconductor Devices for Integrated Circuits, Chenming Hu
3. Semiconductor Fundamentals, Robert F. Pierret
4. Semiconductor Physics and Devices, Donald Neamen
5. Physics of Semiconductor Devices, Simon Sze

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