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Equalization Requirements for DDR5

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Abstract

Equalization, especially a non-linear type such as DFE, is relatively new for DDR.

Unlike SerDes channels, DDR is not always point-to-point, but can have multiple drops. Like previous generations of DDR, not all controllers will have the same capabilities.

So for a system designer, selecting an optimal controller for a given system topology is important. Different topologies will require unique controller capabilities. Conversely, a given controller’s capabilities will affect the topologies supported by that controller.

This paper analyzes the controller I/O transceiver characteristics requirements based on multiple realistic DDR5 topologies.

Author(s) Biography

Nitin Bhagwath is a Product Architect at Mentor Graphics. He has designed and architected high-speed systems for Hewlett Packard and Cisco for ten years. He has been with the high-speed simulation group at Mentor Graphics since 2012, where he advises simulation design on multi-gigabit SerDes signals, power integrity and DDR memory. Nitin represents Mentor Graphics at the JEDEC memory groups. Nitin has a bachelors in Electronic Engineering from Bangalore University, an MS in EE from Purdue University and an MBA from the Indian Institute of Management, Bangalore.

Arpad Muranyi joined Mentor Graphics Corporation in 2007. His work includes developing and testing advanced modeling and simulation technologies for Mentor's leading edge signal integrity simulation products. He also serves as the chairman of the IBIS Advanced Technology Modeling Task Group which is responsible for developing support for such new technologies in the IBIS specification. He was one of the co-founders of the IBIS specification. Before he joined Mentor, Arpad worked at Intel Corporation in Folsom, CA as a Signal Integrity engineer. Arpad graduated in 1991 from the California State University Sacramento with a BSEE degree.

Randy Wolff is a Principal Engineer at Micron Technology, Inc. and leads the Silicon SI team within the Signal Integrity R&D Group. He developed Micron's IBIS and HSPICE modeling program and is responsible for die-level SI including buffer model development for most DRAM, NAND and NOR FLASH products. He serves as Secretary of the IBIS Open Forum Committee. Randy is a Senior Member of IEEE. He graduated cum laude from Montana State University with a BSEE degree.

Shinichiro Ikeda is a Manager of Custom SoC Development Division at Socionext Inc. Currently, he manages the DDR IP team to support any memory controller and DDR-PHY. Since joining Socionext in 2015, he had worked at Fujitsu Semiconductor Ltd. as a manager of DDR IP team. He received his M.S degree in Electronics Engineering form Nagoya University in Japan.

Eiji Fujine is a hardware engineer at Socionext Inc. He is qualified as an iNARTE EMC engineer in 2015. After working as a CAD software engineer and a LSI-PKG-Board (LPB) co-Design engineer at Fujitsu VLSI, he works in DDR design methodology at
Socionext since 2015. He graduated in 1991 from the University of Mie in Japan with a BSEE degree.

Ryo Shibata is a hardware engineer at Socionext Inc. After working as a CAD software engineer and a LSI-PKG-Board (LPB) co-Design engineer at Fujitsu VLSI, he works in DDR design methodology at Socionext since 2015. He received his bachelor in Applied Physics from the University of Nagoya in Japan.

Yumiko Sugaya is a hardware engineer at Socionext Inc. Since 2012, she works on DDR subsystem (memory controller + DDR-PHY) development of SoC in Fujitsu VLSI and Socionext. She investigated and created SSO aware IBIS5.x, and provided DDR Design kits to PCB designer. She presented at Asian IBIS Summit (TOKYO) in 2015. She received her M.S degree in Physics form Shizuoka University in Japan.

Megumi Ono is a hardware engineer at Socionext Inc. 2010-2017, she worked on a team LSI-PKG-Board co-Design Methodology Development for SI/PI in Fujitsu Semiconductor and Socionext. Currently, she works in DDR design methodology at Socionext. She graduated in 2000 from the University of Aizu in Japan with a BSEE degree.

Chuck Ferry is a product marketing manager at Mentor Graphics Corporation. Chuck focuses on product definition and validation for signal integrity and power integrity solutions. He has spent the last 16 years tackling a broad range of high speed digital design challenges spanning from system level design to multi-gigabit channel analysis developing and incorporating detailed characterizations of the IC, packages, connectors and multiple boards. He has delivered signal integrity services and seminars using a wide range of EDA tools as well as performed modeling services creating and validating IC models. Chuck graduated Magna cum Laude from the University of Alabama with a BSE in electrical engineering and continued graduate course work in the areas of signal processing and hardware description languages.

Dr. Vladimir Dmitriev-Zdorov is a principal engineer at Mentor Graphics Corporation. He has developed a number of advanced models and novel simulation methods used in the company’s products. His current work includes development of efficient methods of circuit/system simulation in the time and frequency domains, transformation and analysis of multi-port systems, and statistical and time-domain analysis of SERDES links. He received Ph.D. and D.Sc. degrees (1986, 1998) based on his work on circuit and system simulation methods. The results have been published in numerous papers and conference proceedings.
Introduction

Operating a DDR4 memory channel at even speeds of 2666MT/s can be a challenge for multi-slot setups. So what will be required in the next-generation DDR5 memory busses to enable them to run at speeds of 3200MT/s and above? What are the implications for controllers, and how does one plan the supported topologies for a given controller?

DDR5 – What’s new

DDR5 continues the tradition of increasing data rates from previous generations. The data transfers are expected to be specified between 3200 to 6400 MT/s. DDR5 will continue to use single ended data nets as with previous generations.

To help manage the signal integrity issues arising from the high data rates, Decision Feedback Equalization (DFE) is expected to be incorporated into the DRAMs. This should help mitigate the effects of reflected signals.

DDR Memory – significant challenges

Though DDR busses are now reaching speeds of some SerDes protocols, there are a few significant differences between the two with respect to signal integrity. Two relevant differences are the number of drops and the lengths of the channels.

Multi-Drop Channel

With respect to the number of drops on the bus, SerDes channels are point-to-point. There are well terminated receivers at either end of the channel. Stubs are minimal for these channels.

DDR busses on the other hand can often be multi-drop. The Data signals are particularly vulnerable since they run at the full double data rate speed. Each DRAM load on the bus represents a rank on the bus. In such cases, the trace to the far end DRAM can act as a stub when the intended target DRAM is in the center. Similarly, if the center DRAM drives during a read transaction, the signal will be affected by the stub to the far end DRAM while the intended destination is the controller.

Short Channel

The second relevant difference is the length of the channel. Although there exist short-reach SerDes channels, SerDes busses are often much longer than DDR busses. These long channels significantly attenuate the signal at the high frequency of operation. So, for the longer SerDes channels, insertion loss and strategies to mitigate its effects are a dominant factor.

The DDR bus, however, is usually much shorter. So, insertion loss is not as much of a factor since the signal is not attenuated as much over a short distance. Consequently, reflected signals are also not attenuated as much with shorter channels. Any reflected
energy which occurs due to imperfect termination tends to stay in the channel for a larger number of bit intervals.

**Equalization – How it helps with DDR5**

Equalization has been used in SerDes and other high-speed busses for quite some time. It has also been incorporated in some DDR3 and DDR4 controllers. In general, equalization aims to manipulate the signal so as to compensate for the loss and dispersion of the channel.

Long, lossy channels for example, act as low-pass filters. Continuous-Time Linear Equalizers (CTLE) compensate for this behavior of the channel at the Rx by implementing a high-pass filter which offsets the low-pass behavior of the channel.

Feed-Forward Equalization (FFE) accomplishes a similar task, except at the transmitter side. Since transitions between logical states carry the highest frequency components, the energy for these transitions can be boosted more than the energy of transmitted waveforms near their steady state behavior.

For reflection dominated channels such as the DDR bus, Decision Feedback Equalizers (DFE) help the most by mitigating the effects of inter-symbol interference (ISI). Reflections from longer channels pose a particular challenge when the flight time exceeds the DFE tap length. Proper termination is usually the optimal solution for those situations.

**ISI**

ISI is the effect that a given symbol has on the response from subsequent symbols observed at the receiver. ISI can be caused by signals reflected due to improper termination, large capacitive loads in the channel, or dispersion effects where different frequencies are attenuated by different amounts (usually, the higher frequencies are attenuated more than the lower frequencies, causing the channel to behave like a low-pass filter).

Imperfect termination might arise due to stubs in the channel, on-die termination (ODT) values which don’t correctly match the channel’s impedance, impedance mismatches in packages, connectors or vias, or non-optimal driver impedances. In such cases, energy from one symbol remains in the channel for longer than the symbol duration. This residual energy overlapping with the subsequent symbols makes it more difficult to properly resolve the subsequent symbols at the receiver.
Figure 1 - ISI due to reflections

In Figure 1, the energy from the 1-to-0 transition can be seen to remain in the channel long enough to affect subsequent symbols. Here, the effect of the 1st symbol can be seen in the 3rd symbol. Even though the third symbol is transmitted in a low state, the margin at the third symbol has been reduced due to the effect of the first symbol.

Furthermore, the channel usually acts as a low-pass filter. This prevents much of the higher frequency spectrum of the signals – notably the edge transitions – from being transmitted correctly. This attenuation of the higher frequency components of the signal smears out the signal over time, once again affecting subsequent bits.

Figure 2 - ISI due to low pass channel

In Figure 2, the channel acts as a low pass filter, causing the sharp edges to become more flattened over time.
In real systems, ISI is caused by a combination of both effects. For short channels such as DDR, the reflective elements can be significant.

**Rx Continuous Time Linear Equalizer (CTLE)**

CTLE is used to compensate for the low-pass effect of the channel by implementing a high-pass filter at the receiver. The high-pass filter is designed to offset the low-pass channel to result in a relatively flat response across frequencies.

For short, reflection-dominated channels such as those in DDR, CTLE does not usually play as significant a part as other equalizers because CTLE is not particularly adept at compensating for reflective, low-loss channels.

CTLE is not expected to be used in DDR5 DRAM receivers, but may appear at the controller. The experiments below will show whether CTLE at the controller makes a significant difference.

**Rx Decision Feedback Equalizers (DFE)**

DFE works by attempting to compensate for the ISI energy which remains in the channel due to stubs and imperfect terminations. By estimating the behavior of a given transition on subsequent bits, the DFE can try to cancel out the influence on those subsequent bits.

![Figure 3 - Pulse Response Example at 2Gbps](image)

In Figure 3, a pulse response (an isolated 1 preceded and followed by a series of 0’s) of a channel is shown. Note that the channel is not necessarily representative of a typical expected DDR5 channel, but is used as an example to illustrate DFE. The first sample can be assumed to be made at 0.797ns, when the signal is at a peak. Note that this selection includes the pre-cursor effect as well. The subsequent samples will be at 1UI
intervals, or 1.297ns, 1.797ns, 2.297ns and 2.797ns for a 2Gbps signal. As can be seen in the diagram, some of these sample points deviate a non-trivial amount from the 0 level. This will affect the subsequent sample.

The response lasts until about 2.297ns, after which the residual energy is negligible. Since the impact of the bit is only for 3UI, a 3-bit DFE should be able to handle this case and take care of a significant amount of the reflected signal.

As mentioned earlier, DDR busses are prone to be reflective due to their short trace lengths (and therefore low total insertion loss), and their tendency to have stubs from multiple DRAM drops on the same bus.

DFE therefore offers a good solution for DDR signals which are prone to reflective ISI. Despite ISI caused by reflections, the signal at the receiver can use the DFE to account for anticipated ISI and mitigate its effects. For this reason, DDR5 will likely specify a 4-tap DFE for DRAMs.

Note in Figure 3 that ISI exists before the cursor (t=0.797) as well. DFE can’t help with this pre-cursor effect. DFE works at the receiver by analyzing the past bits, and so can cancel out the effects of the current transition on future bits (post-cursor). It does not know the value of the future bits, and so doesn’t have the means to cancel out any pre-cursor effects of those future bits.

**Tx Feed Forward Equalizer (FFE)**

FFE can be used at the driver to ensure that the energy driven at the higher frequencies is greater than the driven energy at the lower frequencies to compensate for the channel’s low-pass behavior. The high frequency component of the data stream is contained in the transitions, so the signal will have a higher amplitude during the transition than during steady state.

FFE has the ability to determine future bits in addition to the past bits. So, the shape of the bit can be manipulated in anticipation of a transition to also mitigate pre-cursor ISI caused by that transition. This is in contrast to DFE mentioned previously which can only compensate for post-cursor ISI.

![Figure 4 - Post-Cursor FFE](image)
FFE is not expected to be in the DDR5 specification for DRAMs. Controllers might decide to implement FFE based on requirements.

Controller Equalization for common topologies

Now, we can consider the equalization requirements at the controller side for common topologies. Equalization is expensive not only in terms of silicon real estate, but can also consume a significant amount of power. From a DRAM perspective, the equalization available is a four tap DFE. Controller equalization capabilities can vary quite a bit. In this section, we consider common DDR topologies, and the types of equalization which would optimize operations.

Test Setup overview

In the following examples, a Micron DDR5 IBIS model is used for both the DRAM as well as a proxy model for the controller. Since the IBIS file does not contain any characterization of the equalization behavior, the simulation tool, HyperLynx’s FastEye Channel Analysis was used for modeling the CTLE, FFE and DFE equalization.

For each channel setup, a worst-case bit pattern is generated. The worst-case bit pattern is derived from the response of the channel from a combination of a single step response and a pulse response. So, the response will have both rising and falling edge response information, and will take any asymmetries of the buffers’ rising and falling behavior into account. A series of worst-case bit patterns are generated which minimize the eye-opening for different vertical cross-sections of the eye, typically taken with about 0.1UI step, until the entire maximally stressed eye is built.

Tx FFE, if enabled, is optimized by minimizing the total effect from ISI at the sampling location by solving a system of equations with respect to the FFE taps. Rx CTLE assumes a two-pole, one-zero implementation similar to those used in SerDes channels such as PCIe-G3. It is optimized for all the parameters by a simple non-linear optimization algorithm with aims to minimize the ISI around the selected sampling location. DFE tap values are generated through a zero-forcing algorithm which eliminates the remaining post-cursors in the equalized bit response.

Note that crosstalk effects, SSO/SSN, and other power aware effects are not taken into account in these simulations. Furthermore, the strobe is not used to center the eye. Rather, the eye is wrapped around at 1UI intervals. A particular thing to note is that crosstalk will not be significantly mitigated by the use of equalization. So, while the following setups
highlight the benefits of equalization on ISI, crosstalk effects still need to be taken into account while doing the final system analysis.

**Single-Rank, embedded**

A common setup is for the controller and the DRAM to be in the same PCB, separated by a few inches. The DRAM is usually a single rank load, leading to a point-to-point data bus topology.

![Figure 6 - Single Rank with Controller and DRAM on same PCB](image)

The setup here has a controller connected to the DRAM through an approximately 3” trace. Two vias are used for the layer transitions. The data rate is assumed to be 4400MT/s (UI is 227.27ps). Only the write case is considered since the setup is approximately symmetric.

The pulse response in Figure 7 shows that there is not a significant amount of ringing taking place.
Figure 7 - Pulse response of Point-to-Point setup

The first case is with no equalization at either end, with the eye measured at the DRAM’s die.

Figure 8 - Point to point at 4400MT/s, no equalization

The eye-height is 430mV, and the eye width is 0.92UI.
The next step is to add the four tap DFE at the receiver end.

With the DFE, the eye-width increases by a small amount to 0.93UI (more-or-less unchanged), and the eye-height increases to 510mV.

Finally, we can try the setup with both a 4-tap DFE at the DRAM as well as a 3-tap (one pre-cursor, one post-cursor) FFE at the controller end.

In this case, the eye-width reduces by a marginal amount to 0.90UI while the eye height increases by a negligible amount to 522mV.

From this, it can be seen that not all implementations of DDR5 will necessarily require equalization. Equalization will increase power consumption. So, for short point-to-point setups on the same board, it is entirely possible that equalization will not benefit the system by much. Additionally, due to the short lengths involved, the TX FFE does not provide a great benefit. So, in this case, it is possible to design systems where the controller has no equalization capabilities.

Of course, the unknown here is the eye-mask requirements, which are still TBD.

<table>
<thead>
<tr>
<th></th>
<th>Tx FFE</th>
<th>Rx DFE</th>
<th>Eye-Width (UI)</th>
<th>Eye-Height (mV)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>None</td>
<td>None</td>
<td>0.90</td>
<td>416</td>
<td>Figure 8</td>
</tr>
<tr>
<td>2</td>
<td>None</td>
<td>4-Tap</td>
<td>0.93</td>
<td>510</td>
<td>Figure 9</td>
</tr>
<tr>
<td>3</td>
<td>3-tap (1 pre, 1 post cursor)</td>
<td>4-Tap</td>
<td>0.87</td>
<td>512</td>
<td></td>
</tr>
</tbody>
</table>

Table 1 - Embedded design at 4400MT/s

Two DIMM slots, with one populated 2-rank slot
When multi-DIMM setups are considered, the simplest realistic setup could be the near DIMM left unpopulated and the far DIMM populated. This will minimize the stub created by the near DIMM to just the trace on the motherboard and the connector itself.

In this case, the populated DIMM is assumed to be a 2-rank DIMM. One of the two ranks will have a 48-Ohm termination and the other will remain unterminated. Again, the effect of equalization on the receiver eye is analyzed. Similar to the previous case, only the write is considered.

![Figure 10 - One Populated DIMM setup](image)

The baseline data rate again is 4400MT/s.

<table>
<thead>
<tr>
<th></th>
<th>Tx FFE</th>
<th>Rx DFE</th>
<th>Eye-Width (UI)</th>
<th>Eye-Height (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>None</td>
<td>None</td>
<td>0.69</td>
<td>175</td>
</tr>
<tr>
<td>2</td>
<td>None</td>
<td>4-Tap</td>
<td>0.71</td>
<td>269</td>
</tr>
<tr>
<td>3</td>
<td>3-tap (1 pre, 1 post)</td>
<td>4-Tap</td>
<td>0.64</td>
<td>316</td>
</tr>
</tbody>
</table>

Table 2 - Write to one populated slot at 4400MT/s

In this case, DFE adds margin to the setup. Though there is a reasonably open eye (depending on the eye mask for DDR5) even without any equalization, this eye does not consider other sources of noise such as crosstalk. With realistic noise, DFE and FFE will likely become more important.

**Two DIMM slots, each with two ranks**

The two DIMM slot setup with both slots populated is probably the most interesting situation. When accessing either slot, a significant stub exists to the other slot which is not being accessed. So four cases are analyzed, and the effects of different equalization is analyzed in each case.

1. Write to near slot (48-Ohm at near Rx DIMM, 48-Ohm at far unused DIMM)

   The pulse response for this setup is shown in Figure 11.
Figure 11 - Pulse response. Write to near DIMM

The cursor is at 800ns, and the second ripple peak occurs at 1.713ns. This is almost exactly 4UI apart at 4400MT/s. So, a 4 tap DFE should take care of most of the ISI.

Figure 12 - 4400MT/s Write to near slot, no equalization
Figure 13 - 4400MT/s Write to near slot, 4-tap DFE, no FFE

Figure 14 - 4400MT/s Write to near slot, 4-tap DFE, 1pre-cursor/4post-cursor Tx FFE

<table>
<thead>
<tr>
<th></th>
<th>Tx FFE</th>
<th>Rx DFE</th>
<th>Eye-Width (UI)</th>
<th>Eye-Height (mV)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>None</td>
<td>None</td>
<td>-</td>
<td>-</td>
<td>Figure 12</td>
</tr>
<tr>
<td>2</td>
<td>None</td>
<td>4-Tap</td>
<td>0.651</td>
<td>198</td>
<td>Figure 13</td>
</tr>
<tr>
<td>3</td>
<td>3-tap (1 pre, 1 post)</td>
<td>4-tap</td>
<td>0.657</td>
<td>199</td>
<td>Figure 14</td>
</tr>
<tr>
<td>4</td>
<td>6-tap (1 pre, 4 post)</td>
<td>4-tap</td>
<td>0.680</td>
<td>246</td>
<td></td>
</tr>
</tbody>
</table>

Table 3 - Write to near DIMM at 4400MT/s

In this situation, the DFE at the DRAM plays an important role. Without DFE at the DRAM, the eye is closed. The DFE allows the eye to open to an adequate level. With
the DFE enabled at the DRAM, the FFE at the controller marginally helps the eye-height and eye-width, but only with a 6-tap FFE with one pre-cursor and four post-cursors.

Because the DRAM will have the DFE capability, the additional effect of the FFE is somewhat limited. However, we can see the effect of a hypothetical case where the DRAM does not have DFE at the RX, but the controller has the FFE at the TX.

**Figure 15 - 4400MT/s Write to near slot, no DFE, 1pre-cursor/4post-cursor Tx FFE**

<table>
<thead>
<tr>
<th>Tx FFE</th>
<th>Rx DFE</th>
<th>Eye-Width (UI)</th>
<th>Eye-Height (mV)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 3-tap (1 pre, 1 post)</td>
<td>None</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>6 5-tap (0 pre, 4 post)</td>
<td>None</td>
<td>0.746</td>
<td>187</td>
<td></td>
</tr>
<tr>
<td>7 6-tap (1 pre, 4 post)</td>
<td>None</td>
<td>0.714</td>
<td>218</td>
<td>Figure 15</td>
</tr>
</tbody>
</table>

**Table 4 - Effect of FFE on 2-rank write to near slot**

FFE can be seen to have a good impact on the result, provided there are an adequate number of taps to account for the significant post-cursor effects. Also, FFE can take into account the pre-cursor ISI, whereas DFE cannot.

However, since DFE is already available at the DRAM, the effect of the additional FFE at the Tx is incrementally not as much as if the only option were FFE.

2. **Write to far slot (48-Ohm at far Rx DIMM, 48-Ohm at near inactive DIMM)**

The pulse response for this setup is shown in Figure 16. The second ripple occurs about 1.09ns after the main cursor, or a bit over 4 UI. Though the 4th DFE tap might
not catch the peak of the ring-back, the second ripple is small enough to possibly not make a significant difference.

![Figure 16 - Pulse response. Write to far DIMM](image)

![Figure 17 - Eye for Write to far DIMM. No Equalization](image)

Although the eye without equalization is not optimally open, the case of writing to the far DIMM is clearly not the worst case. The pulse response does not have the same amplitude of ripples as the write to the near DIMM, and the eye diagram is somewhat open even without any equalization. With equalization, the eye opens even more.

<table>
<thead>
<tr>
<th>Notes</th>
<th>Tx FFE</th>
<th>Rx DFE</th>
<th>Eye-Width (UI)</th>
<th>Eye-Height (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>None</td>
<td>None</td>
<td>0.733</td>
<td>144</td>
</tr>
<tr>
<td>2</td>
<td>None</td>
<td>4-Tap</td>
<td>0.739</td>
<td>222</td>
</tr>
<tr>
<td>3</td>
<td>3-tap (1 pre-</td>
<td>4-tap</td>
<td>0.670</td>
<td>247</td>
</tr>
</tbody>
</table>
Table 5 - Write to far DIMM at 4400MT/s

3. Read from near slot (far DIMM slot 48Ohms, Controller 48Ohms)

The pulse response for this setup is shown in Figure 18.

![Figure 18 - Pulse Response. Read Middle DIMM](image)

The pulse response in Figure 18 shows the second ripple at about 910ps from the main cursor. At 4400MT/s, this corresponds to almost exactly 4UI. Therefore, a 4-Tap DFE would provide an optimal mitigation of this ISI. There are smaller ripples further on, but the effects should be minimal.
Figure 19 - Read from near DIMM at 4400MT/s. No Equalization

Figure 20 - Read from near DIMM at 4400MT/s. 4 tap DFE

<table>
<thead>
<tr>
<th></th>
<th>Rx CTLE</th>
<th>Rx DFE</th>
<th>Eye-Width (UI)</th>
<th>Eye-Height (mV)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>None</td>
<td>None</td>
<td>0.45</td>
<td>48</td>
<td>Figure 19</td>
</tr>
<tr>
<td>2</td>
<td>None</td>
<td>1-Tap</td>
<td>0.43</td>
<td>49</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>None</td>
<td>2-tap</td>
<td>0.65</td>
<td>118</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>None</td>
<td>3-Tap</td>
<td>0.67</td>
<td>156</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>None</td>
<td>4-Tap</td>
<td>0.72</td>
<td>212</td>
<td>Figure 20</td>
</tr>
</tbody>
</table>
Table 6 - Read from near DIMM at 4400MT/s

<table>
<thead>
<tr>
<th></th>
<th>Rx CTLE</th>
<th>Rx DFE</th>
<th>Eye-Width (UI)</th>
<th>Eye-Height (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>None</td>
<td>5-Tap</td>
<td>0.71</td>
<td>226</td>
</tr>
<tr>
<td>7</td>
<td>None</td>
<td>6-Tap</td>
<td>0.71</td>
<td>231</td>
</tr>
<tr>
<td>8</td>
<td>None</td>
<td>7-Tap</td>
<td>0.70</td>
<td>232</td>
</tr>
<tr>
<td>9</td>
<td>None</td>
<td>8-Tap</td>
<td>0.70</td>
<td>230</td>
</tr>
</tbody>
</table>

As predicted, about 4 taps of DFE at the controller are the optimal number for this setup. More taps have diminishing returns for the setup. Below 2 taps, there might not be an adequate eye-opening at the controller.

Enabling a 2-pole, 1-zero CTLE at the controller did not improve the waveform. Note that this result is only valid with the controller package assumed with this experiment. Any change in the controller’s package might change the effect of CTLE during read transactions.

4. Read from far slot (48-Ohm on near DIMM, 34-Ohm Driver DIMM, 48-Ohm Rx)

The pulse response is shown in Figure 21. The reflected energy does not last very long and diminishes quite a bit after the first ripple.

![Figure 21 - Pulse Response. Read from far DIMM](image-url)

<table>
<thead>
<tr>
<th></th>
<th>Rx CTLE</th>
<th>Rx DFE</th>
<th>Eye-Width (UI)</th>
<th>Eye-Height (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>None</td>
<td>None</td>
<td>0.67</td>
<td>174</td>
</tr>
<tr>
<td>2</td>
<td>None</td>
<td>1-Tap</td>
<td>0.68</td>
<td>186</td>
</tr>
</tbody>
</table>
Table 7 - Read from far DIMM at 4400MT/s

Only 4 taps are needed to attain a reasonable eye opening with this setup. Enabling CTLE did not improve the eye.

5. Data Rate for Writes to Near DIMM

As was shown in Table 3, DFE is needed to open the eye at the DRAM. However, the pulse response in Figure 11 shows the second ripple at 900ps from the main cursor. At higher data rates, this becomes more than four UI long, possibly becoming a significant factor when the limited 4-tap DFE in the DRAM no longer compensates for the reflected signal.

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Tx FFE</th>
<th>Eye-Width (UI)</th>
<th>Eye-Height (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4800</td>
<td>3-Tap (1 pre)</td>
<td>0.53</td>
</tr>
<tr>
<td>2</td>
<td>5200</td>
<td>3-Tap (1 pre)</td>
<td>0.266</td>
</tr>
<tr>
<td>3</td>
<td>5600</td>
<td>None</td>
<td>0.256</td>
</tr>
<tr>
<td>4</td>
<td>5600</td>
<td>3-Tap (1 pre)</td>
<td>0.187</td>
</tr>
<tr>
<td>5</td>
<td>5600</td>
<td>5-Tap (2 pre)</td>
<td>0.213</td>
</tr>
<tr>
<td>6</td>
<td>6400</td>
<td>None</td>
<td>0.228</td>
</tr>
<tr>
<td>7</td>
<td>6400</td>
<td>3-Tap (1 pre)</td>
<td>0.073</td>
</tr>
<tr>
<td>8</td>
<td>6400</td>
<td>5-Tap (2 pre)</td>
<td>0.094</td>
</tr>
</tbody>
</table>

Table 8 - Data Rate results for write to near DIMM

As can be seen, for data rates above 5200MT/s, the eye opening becomes compromised. Mitigating this might require a careful design of both the DIMM and the motherboard if two slot DIMMs are to be supported at these speeds.

From the analysis of the different setups, it is evident that the most critical situations are Writes and Reads to the near DIMM. During these transactions, DFE plays the most significant role.
During Writes, the 4-Tap DFE at the DRAM provides a significant boost to the eye opening. The controller’s FFE does add some extra margin, and it may be useful in designs which struggle to pass otherwise.

During Reads, there is no equalization assistance at the DRAM. At the controller, the most useful feature again is DFE. At least 4 taps are required, though this minimum requirement will depend on the exact channel’s response. However, too many taps do not necessarily add much benefit.

Limitations and assumptions of methodology used

Channel response based analysis makes several assumptions which are not necessarily appropriate for DDR busses. Although the results may be reasonable approximations, they may not be accurate enough. Below are some of the assumptions:

1. LTI: The buffers and the channel are assumed to be Linear and Time Invariant. However, several effects such as Simultaneous Switching Noise will make the system time variant. These effects are not taken into account in channel response based simulations.

2. CDR: One of the most popular statistical simulation environments, IBIS-AMI, does not have provisions for a strobe input. It assumes an internal CDR, which is not the case for DDR.

Alternative Simulation Methodology

One alternative would be to use IBIS models with the Verilog-A language extensions. Verilog-A models can be incorporated into traditional IBIS models through the [External Model] or [External Circuit] keywords.

Verilog-A models can support digital signal processing algorithms in the buffer models. There are two advantages to this method – the incorporation of non-LTI effects and the ability to incorporate equalization algorithms.

The capability to incorporate non-LTI effects would be similar to that of traditional IBIS. IBIS 5.0, for example, allows the creation of power-aware IBIS models which take time-variant power effects into consideration with the buffer model.

Furthermore, Verilog-A allows the coding of any equalization algorithms, such as DFE, using event based execution, which is not a capability of I-V curve based legacy IBIS models. The signal processing algorithms written in Verilog-A do not slow down the speed of execution significantly because they can be written in an event driven manner. Consequently, the DFE code does not have to be executed at each time-step of the analog engine.

Summary

DDR channels are prone to reflection-based ISI effects. As such, equalization techniques which mitigate reflections will be useful for the higher data rates of DDR5.
While point-to-point topologies in DDR5 might work without equalization, topologies involving DIMMs or other add-on cards will require equalization at the DRAM and the controller. DFE is particularly useful in mitigating the effects of reflective ISI involved in DDR channels.

Further investigation is needed in formulating a simulation methodology incorporating non-LTI effects such as DFE and power-aware SSO/SSN with DDR specific requirements such as strobe-based clocking.