Technical Note

Bypass Capacitor Selection for High-Speed Designs

Introduction

In order to guarantee better performance from high-speed digital integrated circuits (ICs), manufacturers are tightening power supply noise margins. With lower power supply noise margins, the designer needs to pay closer attention to local bypass capacitor selection.

As bus speeds increase and switching times decrease, proper selection of local bypass capacitors for high-speed digital ICs is becoming increasingly complex. With wider parts becoming prevalent in cache subsystems, the amount of current required from the bypass capacitor to decouple noise from the current transients switching across the power bus is increasing. At the same time that the current transients become larger, the need to choose smaller capacitance values is becoming more important. Smaller capacitance values offer lower series inductance.

The role of the bypass capacitor is to decouple the power supply bus from the IC. Figure 1 on page 2 shows the equivalent circuit of a decoupling loop. The objective is to eliminate the effects of the power bus inductance and resistance (R1, Rg2, L2, Lg2 in Figure 1) so that transient currents flowing across the power bus do not cause excessive noise at the power and ground pins of the IC. Therefore, the bypass capacitor should have low effective series resistance (ESR) and series inductance while having a large enough capacitance value to supply current to the IC during switching.

Several factors need to be considered when selecting local bypass capacitors. These factors include selecting the proper capacitor value, dielectric material, geometry and the location of the capacitor in relation to the IC. Careful observance of fundamental principles will determine how well the capacitor can suppress switching noise.

Selecting the correct bypass capacitor in a high-speed design has economic and design reliability consequences. You may be tempted to place any large value capacitor across the power pins for bypass. But choosing a value that exceeds the necessary value can result in higher series inductance, increased expense, and inferior electrical or nominal value stability characteristics.

Figure 1:   Bypass Decoupling Loop
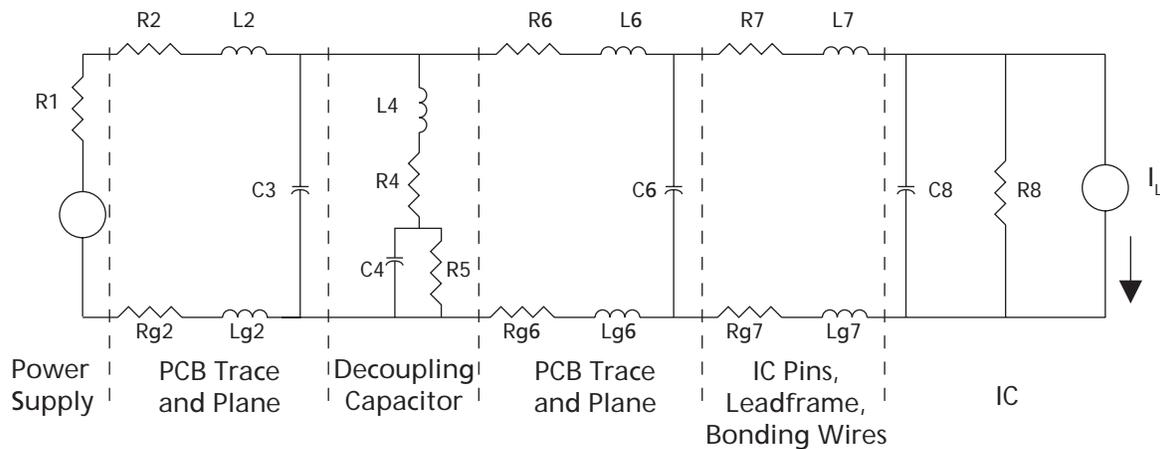
Selecting a Capacitor Value

There are two methods for selecting a bypass capacitor. One method uses a simple calculation that relies upon the load being driven by the outputs from the IC. The second method uses the maximum allowed reactance of the bypass circuit to determine the number and size of the bypass elements. Using the first method, you can get an approximation of the ideal value without having to determine the impedance characteristics of other components in the system. The second method considers the impedance routing back to the power supply.

The importance of adequate bypass is especially apparent when designing with today's faster memory devices. The following example shows the methodology that should be used for any high-speed memory device. Using the SyncBurst SRAM you can have as many as 36 outputs firing simultaneously for each IC. If each output is driving a large load, the current surge can be very high. For example, if you are driving a 30pF load from 0V to 3V with 2ns edges, the transient current will be:

$$I = \frac{CdV}{dt}$$

$$I = \frac{30pF(3V)}{2ns}$$

$$I = 45mA$$

Therefore, the current demanded by the SRAM switching all 36 outputs is 36 x 45mA = 1.62A in 2ns. The SRAM has a V_{DD} tolerance of 3.3V +0.3V/-0.165V. If you consider some droop from the power bus and a switching time of 2ns, and allow a maximum voltage dip (DV) on the SRAM of -0.05V, the choice of bypass capacitor becomes:

$$C = \frac{Idt}{dv}$$

$$C = 64nF$$

Choosing a value of 70nF will allow for variations due to temperature and aging. Better yet, choose two 34nF and place them in parallel to help reduce ESR. If you were to select a large capacitor, such as a 0.47µF, you could be adding unnecessary inductance that can cause glitching on the supply lines and violate the IC power supply noise specification.

For example, using the relationship $V = L \times di/dt$, if a series inductance as small as 1.5nH is present, then under the conditions described above glitching could be as high as 1.4V. When considering the entire bypass loop, however, actual glitching will probably be much less because of parallel inductances and capacitances.

In looking at simulation and empirical data, glitching on the bypass capacitor can be quite significant depending on the number of outputs switching and the impedance of the PCB and power bus. Simulation results for Micron's 32K x 36 SyncBurst SRAM have shown that under worst-case conditions (all outputs driving LOW to HIGH, 66 MHz bus), as little as 1nH bypass series inductance can cause noise on the supply that violates the low side of 3.3V +0.3V/-0.165V supply specification. Changing the size of bypass capacitance has little effect on changing the peaking of this noise since the series inductance of the bypass capacitor dominates the effective impedance across the capacitor under high current with very fast switching times.

Considering the effects of series inductance, the method for calculating a bypass capacitor based on charge sharing presented in the previous example may not provide the needed low impedance path necessary to bypass a high-speed, wide I/O device such as the SyncBurst SRAM. You may need to use a method of calculation based on the reactance of the bypass capacitor in relation to the reactance of the bypass loop.

Reference 1 offers a method for calculation based on the allowed reactance of the local bypass capacitor. The result of this calculation is a capacitor array that is intended to be distributed around the PCB. It is very important to note that this design method assumes solid power and ground planes.

In this example, it is assumed that you are using solid power and ground planes and you are bypassing the entire board. The choice for board level bypass capacitors is made much the same way as the following example illustrates for choosing a local bypass capacitor. When determining the board-level bypass, you must determine the power bus inductance and bypass the board from the supply noise that can occur from large current spikes switching across the power bus inductance.

The following example assumes you have already selected a board level bypass. Suppose you wanted to determine the local bypass capacitor for a SyncBurst SRAM. You need to determine the maximum reactance the circuit can tolerate and stay within the 3.3V +0.3V/ -0.165V supply margin. If you are allowing a total change in voltage across the supply pins of 0.05V and the current is changing by around 1.62A, then the maximum reactance at the supply pins becomes:

$$X_{MAX} = \frac{\Delta V}{\Delta I}$$

$$X_{MAX} = 31mW$$

The highest frequency for which the board-level bypass capacitor is effective for bypassing supply noise is determined by its series inductance. The board-level bypass is used to bypass supply noises at frequencies higher than the frequencies not bypassed by the power supply (FBYPASS). Yet the board-level bypass is usually too large to bypass frequencies higher than FBYPASS. If you use an electrolytic for board-level bypass, a typical series inductance is 5nH.

$$F_{BYPASS} = \frac{X_{MAX}}{2\pi L_{SERIES}} = 982 \text{ kHz}$$

There is another frequency (Ref. 1) called the knee frequency. It can be shown that most energy in digital pulses concentrates below the knee frequency and that the behavior of a circuit at the knee frequency determines its processing of a step edge. Therefore, behavior of the circuit at frequencies above the knee frequency hardly affects digital performance. The knee frequency for any digital signal is related to the rise and fall time of its digital edges, but not its clock rate. The knee frequency is given as:

$$F_{KNEE} = \frac{0.5}{T_r} = 250\,\text{MHz for } T_r = 2\text{ns}$$

Next, calculate how much inductance you can tolerate in the circuit.

$$L_{TOT} = \frac{X_{MAX}}{2\pi F_{KNEE}} = \frac{X_{MAX} \times Tr}{\pi}$$
$$L_{TOT} = 19.7\text{pH}$$

The data sheet for a common surface mount chip capacitor shows a series inductance of around 1.5nH. Use this number to find the number of capacitors needed in the array to sufficiently reduce inductance.

$$N = \frac{L_{SERIES}}{L_{TOT}}$$

For this example, N = 76.

The total array bypass must have an impedance less than X_{MAX} down to the frequency FBYPASS. This is true since the board-level bypass capacitor bypasses frequencies below FBYPASS. The array bypass values are determined as follows:

$$C_{ARRAY} = \frac{1}{2pF_{BYPASS}\,X_{MAX}}$$
$$C_{ARRAY} = 5.23\mu F$$
$$C_{ELEMENT} = \frac{C_{ARRAY}}{N}$$
$$C_{ELEMENT} = 69\text{nF}$$

From this calculation, in order to minimize the effects of series inductance in the bypass capacitors, you must distribute 76 64nF capacitors around the board. This bypass will only take care of one SyncBurst SRAM switching into 30pf loads used in this example. Any other high-speed circuits that could be switching at the same time as the SRAM would require additional bypass.

From this analysis, it may seem that 76 capacitors distributed around a PCB is a bit unreasonable. There are alternatives to the standard EIA-sized capacitors available that can significantly reduce series inductance and help eliminate the need to add such a large number of parallel capacitors. Some of these alternatives are mentioned below.

Dielectric and Geometry

Just as important as selecting the correct capacitance value is selecting the correct dielectric material and device geometry. Some materials have better dielectric properties but sacrifice temperature and aging characteristics. Multilayer ceramic (MLC) capacitors are available in a variety of sizes and dielectric materials.

The capacitance value you select can not only determine the size of the component but also the dielectric material. Depending upon your design goal, selection of the dielectric is not a trivial matter.

For example, suppose you decide to just place 0.47µF bypass capacitors throughout your design. Not only are you adding unnecessary series impedance, but you may end up selecting a capacitor that uses Z5U formulation instead of X7R for a dielectric. The Z5U formulation provides a high dielectric constant compared to X7R and other common ceramic formulations. Yet Z5U has inferior temperature and aging stability compared to X7R. Figure 2 shows examples of typical temperature characteristic curves taken from manufacturers' data sheets. These curves show a comparison between the temperature dependence of capacitance for Z5U and X7R. If you calculated a 64nF capacitor, you could choose an X7R dielectric and get better capacitance stability over temperature while at the same time reducing overall series inductance.

**Figure 2:   Temperature Dependence of Capacitance**
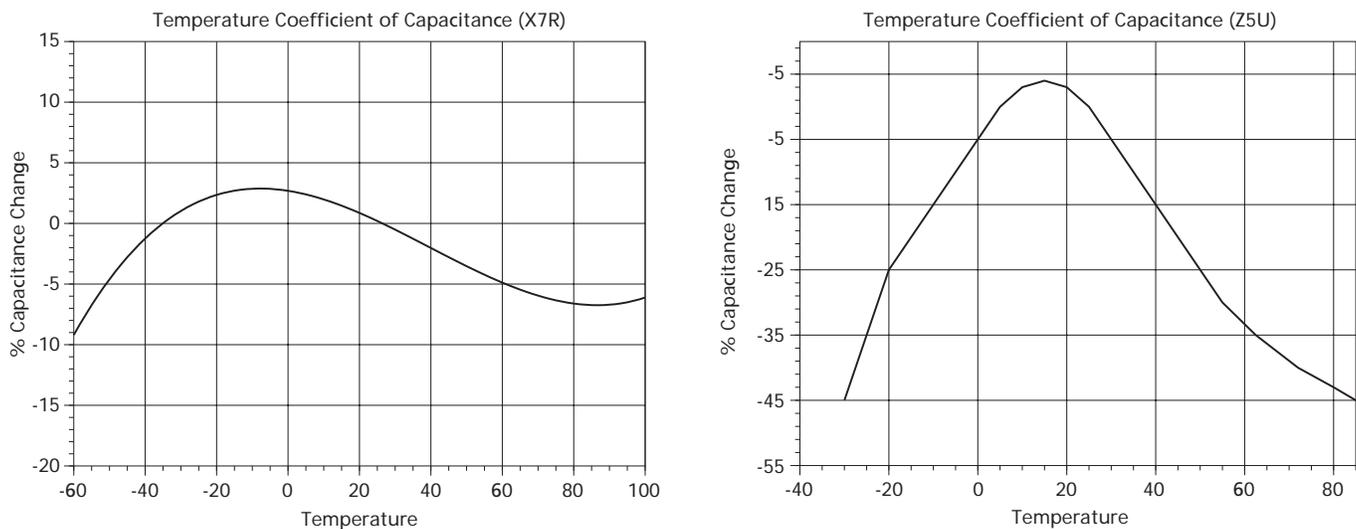
Remember that selecting a large capacitance value in a high-speed design can result in high inductance and defeat the purpose of the bypass capacitor. Reducing series inductance is the primary concern for high-speed design. There are other methods applied by capacitor manufacturers that can, in conjunction with careful component selection, reduce overall series inductance.

The length-width aspect ratio of the capacitor has an effect on inductance. The EIA standard sizes for MLC capacitors are specified by a four digit number. For example, a 0805 is a chip capacitor with a length of 0.08 inches and a width of 0.05 inches. This size ratio results in an inductance of about 2nH. At extremely high frequencies, this much capacitance can cause severe glitching. Reversing this size ratio can result in much lower inductance. AVX Corporation (Myrtle Beach, SC) has developed reverse aspect ratio capacitors. Reversing the aspect ratio so that the width is greater than the length has the effect of lowering the series inductance. AVX has also developed a line of capacitors known as Low Inductance Capacitor Arrays (LICA). The LICA product family allows you to connect to more than one of the same value capacitor within the same package. Each capacitor is designed to reduce inductance through internal design structures (perpendicular current paths) and interconnect methods (C4 "flip-chip" technology).

In addition to reducing series inductance, it is often advantageous to reduce effective series resistance (ESR). The dissipation factor given in manufacturer data sheets indicates the relative ESR for a component. However, low ESR can cause unexpected problems in designs where long power bus leads are present, such as a design where several high-speed ICs are connected to the power bus in parallel.

Figure 3 shows an example of a long LC resonator with the power bus acting as a low-loss inductor between each bypass capacitor (Ref. 2). If repetitive pulses are applied to the power bus in this circuit, ringing can build in amplitude, resulting in a very noisy power bus. To solve this problem, electrolytic capacitors, which have inherently high ESR, can be placed across the bus to help dampen the ringing.

Figure 3: Power Bus LC Resonator
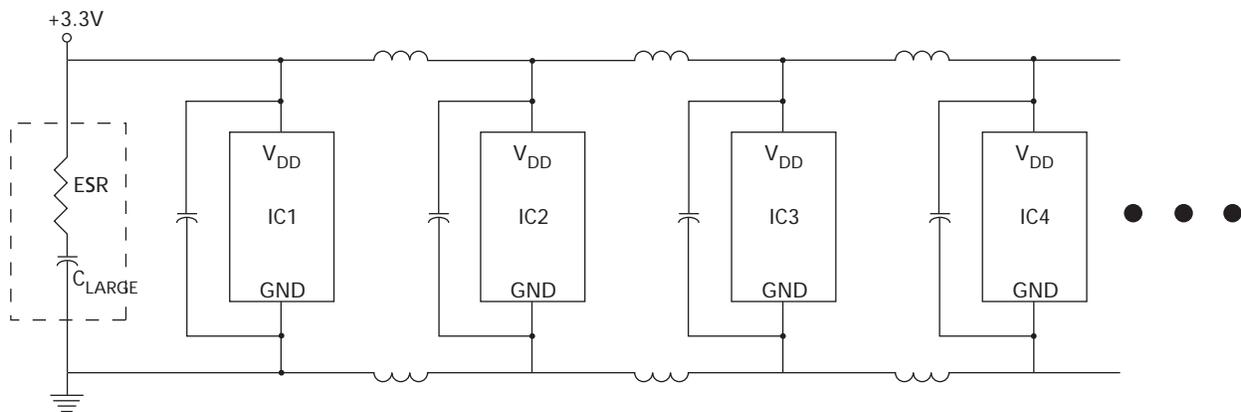
Placement of Capacitor

The placement of the capacitor in relation to the IC can have as much to do with determining its effectiveness as selecting the correct value. The rule of thumb is to place the capacitor as close as possible to the IC. This will minimize inductance caused by long lead lengths (in designs without solid power and ground planes) and minimize transit delays from the capacitor to the IC. Capacitors that fit under the IC can result in the shortest lead lengths.

However, some packages, such as TQFP, cannot accommodate capacitors mounted under the package. To help solve this problem, you can mount capacitors across the power bus very near the memory devices. Figure 4 on page 7 suggests a configuration that will reduce bus inductance for two 100-pin TQFP devices.

Figure 4 shows parallel combinations of capacitors to help minimize the inductance of each element. The figure illustrates one possible configuration. Of course, all designs must be evaluated individually. This configuration will help bypass all of the several power and grounds found on this package as long as the bypass capacitors are very near the ICs and there are solid power and ground planes.

Figure 4:   Bypassing Two High-Speed, 100-Pin TQFP Packages

Bypass Capacitors
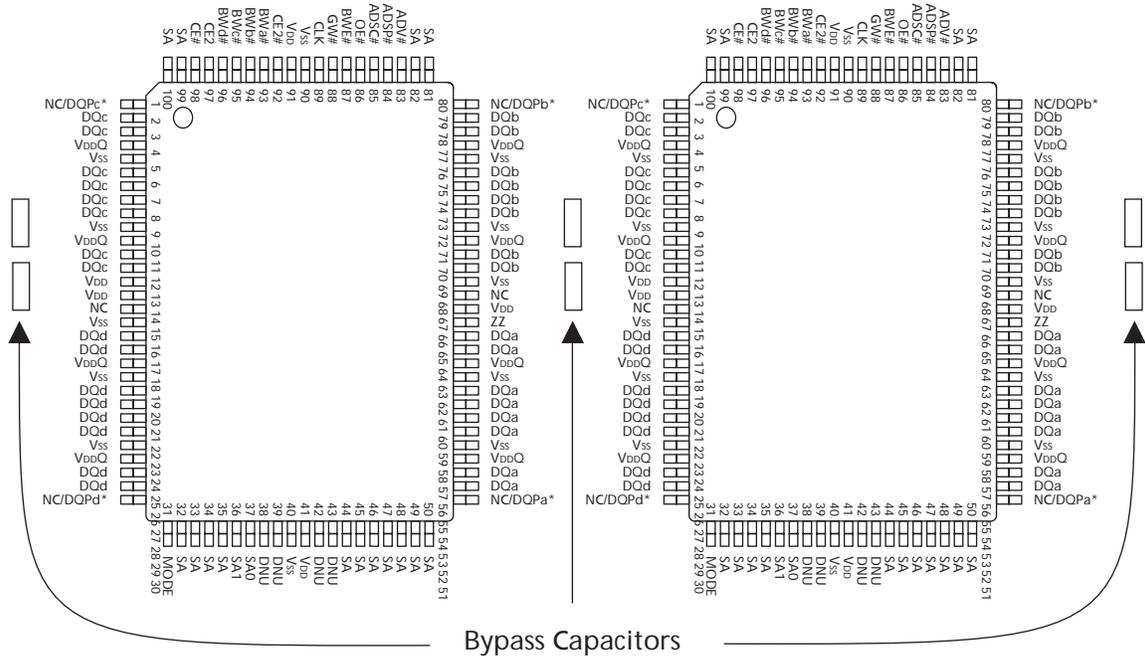
Conclusion

The solution for providing power supply decoupling for high-speed circuits rely upon the characteristics of the bypass elements. Items to keep in mind when selecting a bypass solution are as follows:

1. The inductance of the bypass capacitor is more a determining factor for the effectiveness of the bypass than the capacitance value. Therefore, select bypass capacitors based on series inductance values.

2. Distribute bypass elements throughout the PCB, yet concentrate bypass elements close to the ICs demanding large current transients—even if you have solid power and ground planes. Keep the bypass capacitors as close as possible to the ICs.

3. Use the impedance method presented above to determine the total inductance your design can tolerate and carefully select low inductance capacitors to bypass ICs demanding high current transients.

References

Johnson, Howard, and Martin, Graham, "High-Speed Digital Design: A Hand Book of Black Magic," Englewood Cliffs, NJ: Prentice Hall, ISBN 0-13-395724-1.

Pease, Robert, "Troubleshooting Analog Circuits," Stoneham, MA: Butterworth-Heinemann, ISBN 0-7506-9184-0.

Revision History