Technical Note

Migrating from S29GL-S Device to MT28EW NOR Flash Device

MT28EW NOR Flash Devices

Introduction

This technical note describes the process for converting a system design from the Spansion® S29GL-S device to the Micron® MT28EW single-level cell 45nm NOR Flash device, including 128Mb, 256Mb, 512Mb, and 1Gb densities. The MT28EW higher reliability and performance are ensured through the advanced technology and product design improvements. MT28EW features a large buffer size up to 512 words for advanced program performance. Erase performance is largely improved to meet all variable system design considerations. Moreover, MT28EW supports both ×8 and ×16 data bus for legacy controllers compatibility. This document was written based on device information available at publication time. In case of inconsistency, information contained in the relevant MT28EW data sheet supersedes the information in this technical note.

This technical note does not provide detailed device information. The standard density-specific device data sheet provides a complete description of device functionality, operating modes, and specifications.

Comparative Overview

The MT28EW is compatible with the S29GL-S 128Mb, 256Mb, 512Mb, and 1Gb devices, but features superior program and erase performance. Micron MT28EW supports both a x8 and x16 data bus, while S29GL-S supports only a x16 data bus.

If the system design requires x16 bus only along with floating BYTE#, please contact Micron sales representatives.

Table 1: Part Number Comparison

Notes 1 to 3 apply to the entire table

Memory Size	Package Type		Part Numbers		Notes
			Micron MT28EW	Spansion S29GL-S	
1Gb	56-pin TSOP (14mm x 20mm)	High	MT28EW01GABA1HJS-0SIT	S29GL01GS10TFI01x S29GL01GS11TFIV1x	–
		Low	MT28EW01GABA1LJS-0SIT	S29GL01GS10TFI02x S29GL01GS11TFIV2x	–
	64-ball LBGA (11mm x 13mm) [4]	High	MT28EW01GABA1HPC-0SIT	S29GL01GS10FHI01x S29GL01GS11FHIV1x	4
				S29GL01GS10DHI01x S29GL01GS11DHIV1x	
		Low	MT28EW01GABA1LPC-0SIT	S29GL01GS10FHI02x S29GL01GS11FHIV2x	4
				S29GL01GS10DHI02x S29GL01GS11DHIV2x	
512Mb	56-pin TSOP (14mm x 20mm)	High	MT28EW512ABA1HJS-0SIT	S29GL512S10TFI01x S29GL512S11TFIV1x	–
		Low	MT28EW512ABA1LJS-0SIT	S29GL512S10TFI02x S29GL512S11TFIV2x	–
	64-ball LBGA (11mm x 13mm) [4]	High	MT28EW512ABA1HPC-0SIT	S29GL512S10FHI01x S29GL512S11FHIV1x	4
				S29GL512S10DHI01x S29GL512S11DHIV1x	
		Low	MT28EW512ABA1LPC-0SIT	S29GL512S10FHI02x S29GL512S11FHIV2x	4
				S29GL512S10DHI02x S29GL512S11DHIV2x	

Table 1: Part Number Comparison (Continued)

Notes 1 to 3 apply to the entire table

Memory Size	Package Type		Part Numbers		Notes
			Micron MT28EW	Spansion S29GL-S	
256Mb	56-pin TSOP (14mm x 20mm)	High	MT28EW256ABA1HJS-0SIT	S29GL256S90TFI01x S29GL256S10TFIV1x	–
		Low	MT28EW256ABA1LJS-0SIT	S29GL256S90TF102x S29GL256S10TFIV2x	–
	64-ball LBGA (11mm x 13mm) [4]	High	MT28EW256ABA1HPC-0SIT	S29GL256S90FHI01x S29GL256S10FHIV1x	4
				S29GL256S90DHI01x S29GL256S10DHIV1x	
		Low	MT28EW256ABA1LPC-0SIT	S29GL256S90FHI02x S29GL256S10FHIV2x	4
				S29GL256S90DHI02x S29GL256S10DHIV2x	
128Mb	56-pin TSOP (14mm x 20mm)	High	MT28EW128ABA1HJS-0SIT	S29GL128S90TFI01x S29GL128S10TFIV1x	–
		Low	MT28EW128ABA1LJS-0SIT	S29GL128S90TFI02x S29GL128S10TFIV2x	–
	64-ball LBGA (11mm x 13mm) [4]	High	MT28EW128ABA1HPC-0SIT	S29GL128S90FHI01x S29GL128S10FHIV1x	4
				S29GL128S90DHI01x S29GL128S10DHIV1x	
		Low	MT28EW128ABA1LPC-0SIT	S29GL128S90FHI02x S29GL128S10FHIV2x	4
				S29GL128S90DHI02x S29GL128S10DHIV2x	

Notes:
1. To integrate line items on a variety of customer applications, the MT28EW device unifies the speed and voltage options.
2. For valid combination details, refer to www.micron.com/products and www.spansion.com.
3. Micron materials support the complete industrial temperature range.
4. Micron MT28EW does not support the 64-ball BGA 9mm x 9mm package; the ballout is identical to the 11mm x 13mm 64-ball BGA.

Table 2: Features Comparison

Feature	MT28EW	S29GL-S	Notes
Process technology	45nm single-level cell (SLC) floating gate	65nm MirrorBit Eclipse	1
Density	128Mb 256Mb 512Mb 1Gb	128Mb 256Mb 512Mb 1Gb	

Table 2: Features Comparison (Continued)

Feature	MT28EW	S29GL-S	Notes
Package	64-ball LBGA (11mm x 13mm), 56-pin TSOP (14mm x 20mm)	64-ball fortified BGA (LAA064) (11mm x 13mm) (LAE064) (9mm x 9mm) 56-pin TSOP (14mm x 20mm)	2
Ambient operating temperature	–40°C to 85°C	–40°C to 85°C	
Block architecture	Uniform 128KB	Uniform 128KB	
Data bus	x8/x16	x16	3
Page read size	16 words	16 words	
Extended memory block	128 words (8 + 120)	512 words (256 x 2)	
Program write buffer size	512-word	256-word	4
Single word program	Yes	Yes	
NOP	–	256	9
V_{CC} range	2.7V to 3.6V	2.7V to 3.6V	
V_{CCQ} range	1.65~V_{CC}	1.65~V_{CC}	
V_{PP} accelerated (TYP)	9V	No	6
CFI version	1.3	1.5	5
High voltage auto select (A9)	No	No	
Individual block write protection	Yes	Yes	
Permanent block locking (OTP block)	Yes	Yes	
Hardware protection	Yes	Yes	
Unlock bypass	Yes	No	
Chip erase	Yes	Yes	
Multiblock erase	Yes	No	
RY/BY# pin	Yes	Yes	
Blank check	Yes	Yes	7
Data polling	Yes	Yes	
Read/clear status register (by command)	No	Yes	
Lock register	Yes	Yes	8
EFI CRC	Yes	No	

Notes:
1. MT28EW SLC floating gate technology provides improved performance and optimized quality and reliability.
2. Micron MT28EW does not support the 64-ball BGA 9mm x 9mm package; the ballout is identical to the 11mm x 13mm 64-ball BGA.
3. Micron MT28EW supports both x8 and x16 bus operations. The MT28EW BYTE# must be asserted to a valid V_{IH}/V_{IL}; otherwise, the device fails to work properly.

4. Although the MT28EW features a larger program write buffer than the S29GL-S, no software updates are required during migration. However, software updates leveraging the MT28EW device's larger write buffer can yield improved performance. To configure the MT28EW device software, query CFI word address 2Ah (x16)/54h (x8) on the buffer size option, in either x8 or x16 mode. Linux kernel version 2.6.13 and later supports to probe the buffer size from individual device CFI.
5. For details, refer in this document to Software Considerations for CFI Revisions.
6. By applying 9V (nominal) to V_{PP}/WP# pad, the MT28EW device supports V_{PPH} unlock bypass, accelerated buffered programming, and ACCELERATED CHIP ERASE operations. The 56-pin TSOP package pin 16 and the 64-ball LBGA package ball B4 are V_{PP}/WP# on MT28EW.
7. Micron's BLANK CHECK command is different from that of the Spansion S29GL-S device.
8. Some MT28EW lock register bit definitions are different from S29GL-S lock register bit definitions. For details, refer in this document to Software Considerations.
9. NOP (number of program operations per line) applies only to the S29GL-S device.

Hardware and Mechanical Considerations

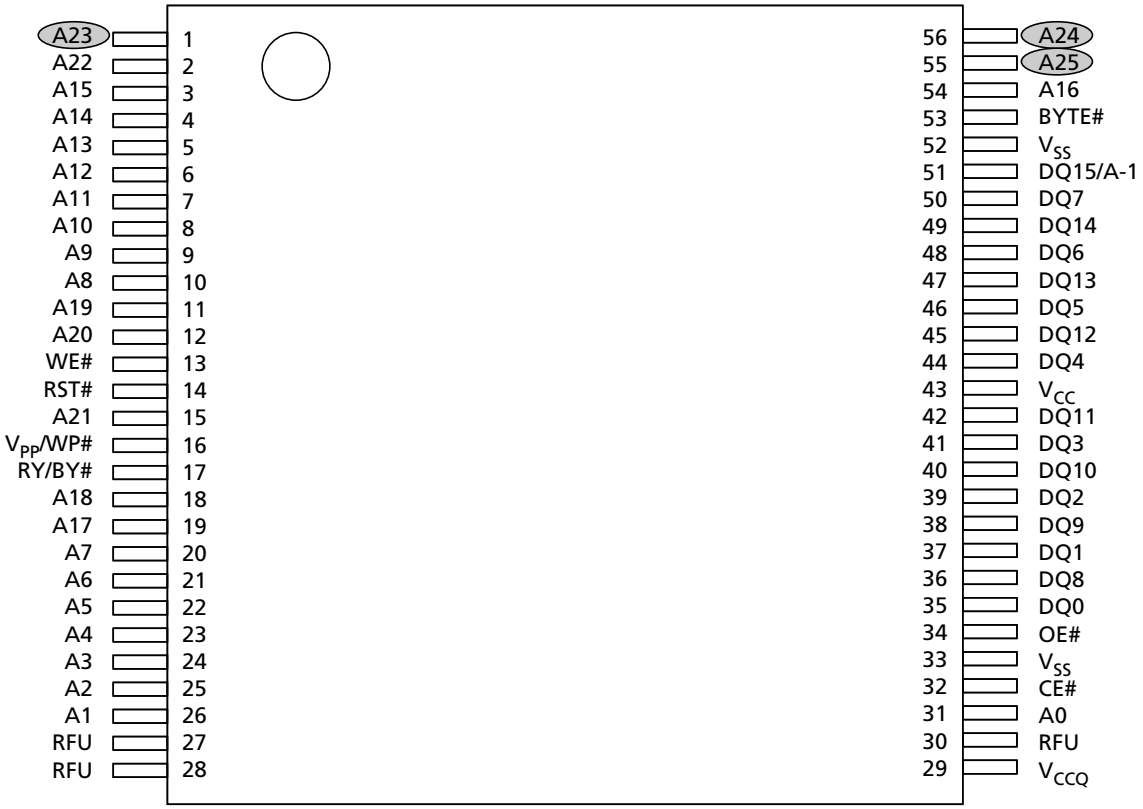
Packages and Ballouts

The MT28EW device is available in 56-pin TSOP and 64-ball LBGA packages, both RoHS compliant and halogen-free. For compatibility, the pin and ball assignments and the physical dimensions are equivalent to the S29GL-S.

Because the 64-ball BGA (9mm x 9mm) and the 64-ball BGA (11mm x 13mm) ballouts are the same, a PCB layout change is not required during conversion. Surface mount placement programs might be changed to adapt the different outer dimensions.

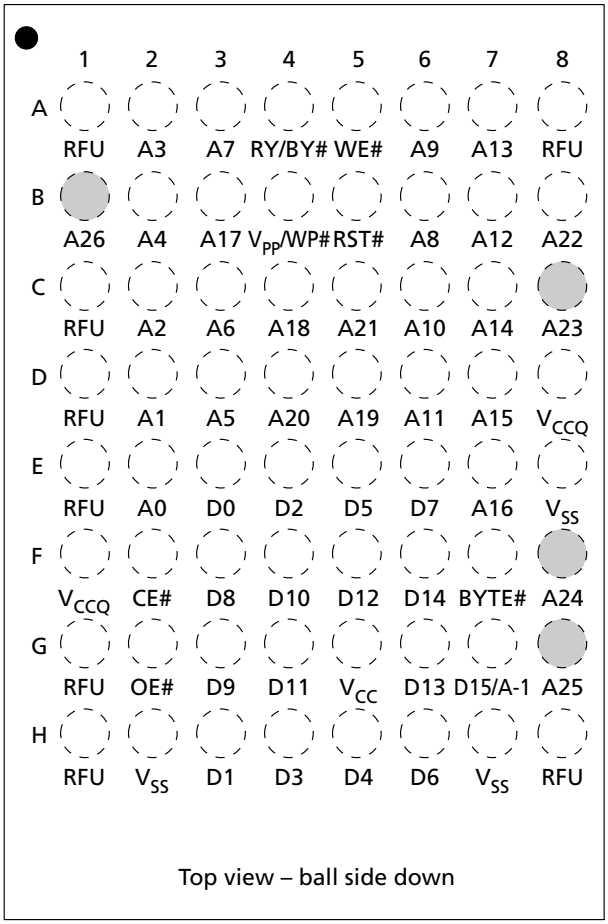
Systems migrating from a fortified BGA to an LBGA should not need to modify the re-flow process in manufacturing.

Figure 1: Micron MT28EW 56-Pin TSOP (Top View)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256Mb and above; otherwise, it is RFU.
3. A24 is valid for 512Mb and above; otherwise, it is RFU.
4. A25 is valid for 1Gb; otherwise, it is RFU.

Figure 2: Micron MT28EW 64-Ball LBGA



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256Mb and above; otherwise, it is RFU.
3. A24 is valid for 512Mb and above; otherwise, it is RFU.
4. A25 is valid for 1Gb; otherwise, it is RFU.

Signals

Table 3: Signal Comparison

Name		Type	Description	Notes
MT28EW	S29GL-S			
A[MAX:0]	A[MAX:0]	Input	Address inputs	
DQ15/A-1	DQ15	I/O	Pin 51 or ball G7	1
DQ[14:0]	DQ[14:0]	I/O	Data inputs/outputs	
CE#	CE#	Input	Chip enable	
OE#	OE#	Input	Output enable	
RST#	RESET#	Input	Reset	
WE#	WE#	Input	Write enable	
BYTE#	RFU	Input	Pin 53 or ball F7	1
RY/BY#	RY/BY#	Output	Ready/Busy	
V_{PP}/WP#	WP#	Input	Pin 16 or ball B4	2
RFU	DNU	–	Pin 28 or ball E1	3
V_{CC}	V_{CC}	Supply	Supply voltage	
V_{CCQ}	V_{IO}	Supply	Input/Output buffer supply voltage	
V_{SS}	V_{SS}	–	Ground	

Notes:
1. Micron MT28EW supports both x8 and x16 bus operations. The MT28EW BYTE# must be asserted to a valid V_{IH}/V_{IL}; otherwise, the device fails to work properly.
2. Micron MT28EW supports ACCELERATED CHIP ERASE and BUFFER PROGRAM functions; S29GL-S does not.
3. RFU: Reserved for future use; DNU: Do not use. The Spansion S29GL-S device may bond an internal signal to the package connector signal, pin 28/Ball E1. Because it is not connected internally on MT28EW, no hardware change is expected during conversion.

Input/Output Capacitance

Table 4: Input/Output Capacitance Comparison

Parameter	MT28EW		S29GL-S FBGA (LAA)		S29GL-S TSOP		Unit
	Min	Max	Typ	Max	Typ	Max	
C_{IN}	3	11	4	9	3	8	pF
C_{OUT}	3	6	3	7	3	6	pF

Power Supply Decoupling

Flash memory devices require careful power supply decoupling to prevent external transient noise from affecting device operations, and internally generated transient noise from affecting other devices in the system.

Ceramic chip capacitors of 0.01µF to 0.1µF should be used between each V_{CC}, V_{CCQ}, and V_{PP} supply connection or system ground pin. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the device package, or on the opposite side of the printed circuit board close to the center of the device package footprint.

Larger electrolytic or tantulum bulk capacitors (4.7µF to 33.0µF) should also be distributed as needed throughout the system to compensate for voltage sags and surges caused by circuit trace inductance.

Transient current magnitudes depend on the capacitive and inductive loading on the device's outputs. For best signal integrity and device performance, high-speed design rules should be used when designing the printed-circuit board. Final signal reflections (overshoot and undershoot) may vary by each system.

Software Considerations

Command Set

The MT28EW and S29GL-S devices have compatible command sets; however, S29GL-S supports commands that MT28EW does not support, such as ENTER/CLEAR STATUS REGISTER commands (70h/71h) and separate PROGRAM SUSPEND/RESUME commands (51h/50h). Basic data polling method and common ERASE/PROGRAM and SUSPEND/RESUME commands (B0h/30h) are supported by S29GL-S.

Manufacturer ID and Auto Select Comparison

Table 5: Auto Select Comparison

Description		Address	Value	Notes
Manufacturer ID				
MT28EW		(Base) + 00h	0089h	1
S29GL-S			0001h	
Device ID				
Cycle 1		(Base) + 01h	227Eh	–
Cycle 2	128Mb	(Base) + 0Eh	2221h	–
	256Mb		2222h	–
	512Mb		2223h	–
	1Gb		2228h	–
Cycle 3		(Base) + 0Fh	2201h	–
Protection register indicator – V_{PP}/WP# locks highest block				
MT28EW: Factory locked		(Base) + 03h	0099h	2
MT28EW: Factory unlocked			0019h	
S29GL-S: Factory locked and customer locked			FFFFh	
S29GL-S: Factory locked and customer unlocked			FFBFh	
Protection register indicator – V_{PP}/WP# locks lowest block				
MT28EW: Factory locked		(Base) + 03h	0089h	2
MT28EW: Factory unlocked			0009h	
S29GL-S: Factory locked and customer locked			FFEFh	
S29GL-S: Factory locked and customer unlocked			FFAFh	

Notes:
1. Micron and Spansion manufacturer IDs are different, and a slight software modification is required during migration.
2. MT28EW does not support DQ6 to indicate the lock status of customer lockable region (8h-7Fh, word mode) from address (base)+03h. S29GL-S supports DQ6 to indicate the status of region (100h-1FFh, word mode).

Unlock Bypass Mode

Micron MT28EW features unlock bypass mode, which is not a feature in the M29GL-S device. No software change is required during conversion from M29GL-S.

System applications using the unlock bypass mode to facilitate shorter programming commands should not use the auto select mode when entering unlock bypass mode on the MT28EW. The low-level driver provides proper sample code for unlock bypass mode use cases.

When AAh/55h/90h operation codes are used to read information under unlock bypass mode, an additional F0h command code must be issued after the AUTO SELECT READ command to return to unlock bypass mode.

In the following code example, the F0h command is written to any address during the first cycle:

```
FlashWrite(ANY_ADDR, (uCPUBusType)CMD(0x00F0));
```

To access auto select information, use the following command sequence (AAh/55h/90h), but only when the device is not in unlock bypass mode. The following example demonstrates how to use auto select mode to read information from the device:

```
ReturnType ReadAutoSelectCode(uCPUBusType *addr, uCPUBusType *ucrCode)
{
/*Send the auto select command */
FlashWrite(ConvAddr(0x00555), (uCPUBusType)CMD(0x00AA));

/* first cycle */
FlashWrite(ConvAddr(0x002AA), (uCPUBusType)CMD(0x0055));

/* second cycle */
FlashWrite(ConvAddr(0x00555), (uCPUBusType)CMD(0x0090));

/* third cycle */
/* Read the code */
*ucrCode = FlashRead(addr);

/* Return to read array mode */
FlashWrite(ANY_ADDR, (uCPUBusType)CMD(0x00F0);

/* first cycle: write 0x00F0 to any address */
/* Check flash response (more flashes could give different results) */

return FlashResponseIntegrityCheck(ucrCode); }
```

READ PASSWORD Command

The READ PASSWORD command is used to verify the password used in password protection mode. To verify the 64-bit password, the complete command sequence must be entered four times at four consecutive addresses selected by A[1:0].

In MT28EW, when the password mode lock bit is programmed and the user attempts to read the password, the device will output 00h onto the I/O data bus.

In S29GL-S, when the password mode lock bit is programmed and the user attempts to read the password, the device will output FFh onto the I/O data bus.

EXIT PROTECTION COMMAND SET

The MT28EW device provides three software protection modes: volatile, nonvolatile, and password protection. The device is shipped with all blocks unprotected. On first

use, the device can be activated in either the nonvolatile protection or password protection mode.

On MT28EW, the EXIT PROTECTION COMMAND SET (90h/00h) command is applied to exit the lock register, password protection, nonvolatile protection, volatile protection, and nonvolatile protection bit lock bit command set modes and return the device to read mode.

The S29GL-S device supports an alternative single command F0h to exit the above modes as well.

EXIT EXTENDED MEMORY BLOCK Command

The EXIT PROTECTION COMMAND SET (AAh/55h/90h/00h) command is applied to exit EXTENDED MEMORY BLOCK modes and return the device to read mode. S29GL-S supports an alternative single command F0h to reset device to read array data as well.

BLOCK ERASE Command

The MT28EW supports multi-block erase, unlike the S29GL-S device. Multi-block erase allows queuing of multiple BLOCK ERASE operations within the timeout period after ERASE CONFIRM command (30h) to minimize command overhead. The system can monitor DQ3 to determine whether the block erase timer has timed out.

Caution: Any command other than BLOCK ERASE or ERASE SUSPEND during the timeout period resets the device to read mode. The data pattern in this block will not be successfully erased.

BLANK CHECK Command

The MT28EW supports a block BLANK CHECK command using the EFI protocol different from the single command set (33h) of S29GL-S.

Please refer to the related data sheets for the implementation details.

Table 6: MT28EW EFI BLANK CHECK Operations

Command and Code/ Subcode	Address and Data Cycles												
		1st		2nd		3rd		4th		5th		6th	
	Bus Size	A	D	A	D	A	D	A	D	A	D	A	D
EFI BLANK CHECK SET-UP (EB/76h)	x8	AAA	AA	555	55	BAd	EB	BAd	76	BAd	00	BAd	00
	x16	555		2AA									
EFI BLANK CHECK CONFIRM and READ (29h)	x8	BAd	29										
	x16												

Data Polling

MT28EW supports data polling only to determine the status of operations such as PROGRAM, ERASE, and BLANK CHECK. It is consistent with the legacy data polling on S29GL-S.

DQ3 – Block erase timer: On the MT28EW device, the DQ3 bit does not transition to logic 1 until ~50 microseconds has elapsed following the last BLOCK ERASE command

cycle (30h); this allows entry of additional BLOCK ADDRESS and ERASE command pairs. The S29GL-S does not support this block erase queuing feature. During BLOCK ERASE operations on S29GL-S, the DQ3 bit immediately transitions to logic 1 after the last ERASE command (30h) cycle to indicate that the ERASE operation has begun.

DQ5 – Error bit: If a DQ5 time-out event occurs on a Flash device, a software RESET command is required to clear DQ5 and return the device to a ready state. MT28EW clears the DQ5 error bit immediately after a software RESET command is issued. S29GL-S can continue to indicate that it is busy for up to 2µs following the RESET command.

Status Register

MT28EW does not support the status register method while S29GL-S enables it as an alternative method.

Lock Register

MT28EW and S29GL-S have different lock register definitions The MT28EW extended memory block is under default unlock state when shipped from the Micron factory (DQ0 = 1 as default). S29GL-S uses lock register DQ6 and DQ0 to indicate the lock state of the separate region. The SSR region 0 is under default lock on S29GL-S device.

See related data sheet for further details.

Table 7: Lock Register Bit Definitions

Bit	MT28EW		S29GL-S	
	Name	Default Settings	Name	Default Settings
DQ[15:9]	Reserved	1	Reserved	1
DQ8	Reserved	1	Reserved	0
DQ7	Reserved	1	Reserved	X
DQ6	Reserved	1	SSR Region 1 (customer) lock bit	1
DQ[5:3]	Reserved	1	Reserved	1
DQ2	Password protection mode lock bit	1	Password protection mode lock bit	1
DQ1	Nonvolatile protection mode lock bit	1	Persistent protection mode lock bit	1
DQ0	Extended memory protection mode lock bit	1	SSR Region 0 (factory) lock bit	0

Extended Memory Block

Micron MT28EW has 128word extended memory block with two regions 8 words +120 words. It is recommended to use block 0 address + offset to access the extended memory block content.

Table 8: MT28EW Extended Memory Block Address and Data

Address (x8)	Address (x16)	Data		
		Micron Prelocked	Customer lockable	
000000h-00000Fh	000000h-000007h	Secure ID number	Determined by customer (default)	Secure ID number
000010h-0000FFh	000008h-00007Fh	Protected and unavailable		Determined by customer

Table 9: S29GL-S Secure Silicon Region

Address Range (x16)	Content	Size
0000h to 00FFh	Factory-locked secure silicon region	256 Words
0100h to 01FFh	Customer-locked secure silicon region	256 Words

Note: 1. Spansion S29GL-S has 512 words Secure Silicon Region with two regions 256 words + 256 words.

CFI Comparison

MT28EW and S29GL-S CFI differences exist because of the different device features and performance characteristics. S29GL-S does not support x8 mode.

To enter the CFI mode on the MT28EW device, the command code 98h is issued to address 555h, while on the S29GL-S device, the address is 55h. It is recommended to follow the formal definition for future compatibility.

Table 10: CFI Comparison

Note 1 applies to entire table.

Address	Description	MT28EW	S29GL-S	Notes
1Dh	V_{PPH} (programming) supply minimum program/erase voltage	0085h	0000h	
	Bits[7:4] hex value in volts			
	Bits[3:0] BCD value in 100mV			
1Eh	V_{PPH} (programming) supply maximum program/erase voltage	0095h	0000h	
	Bits[7:4] hex value in volts			
	Bits[3:0] BCD value in 100mV			
1Fh	Typical timeout for single byte/word program = 2^nµs	0005h	0006h	
23h	Maximum timeout for byte/word program = 2^n times typical timeout	0003h	0003h	
28h 29h	Flash device interface code description 0 = x8 only 0 = x16 only 0 = x8 or x16	0002h 0000h	0001h 0000h	
2Ah 2Bh	Maximum number of bytes in multiple-byte write = 2^n	000xh 0000h	0009h 0000h	2
43h	Major version number, ASCII	0031h	0031h	
44h	Minor version number, ASCII	0033h	0035h	

Table 10: CFI Comparison (Continued)

Note 1 applies to entire table.

Address	Description	MT28EW	S29GL-S	Notes
4D	V_{PPH} supply minimum program/erase voltage	0085h	0000h	
	Bits[7:4] hex value in volts			
	Bits[3:0] BCD value in 100mV			
4E	V_{PPH} supply maximum program/erase voltage	0095h	0000h	
	Bits[7:4] hex value in volts			
	Bits[3:0] BCD value in 10mV			
51h - 79h	S29GL-S extended address range	–	xxxxh	3

Notes:
1. On MT28EW, once BYTE# is tied HIGH (x16 mode), the data output in CFI 2Ah is 000Ah. It turns to 80h when BYTE# is tied LOW (x8 mode).
2. MT28EW supports the CFI version 1.3 and S29GL-S supports the CFI version 1.5.
3. Unlike S29GL-S, on the MT28EW device, CFI 51h~79h is reserved. Refer to Spansion S29GL-S for detail information.

Performance Comparison

Shown here are key specification differences between MT28EW and S29GL-S. All data-sheet parameters should be confirmed using a real application to ensure a successful conversion from S29GL-S to MT28EW. The MT28EW features improved typical program and erase performance.

Table 11: Program and Erase Performance Comparison (-40°C to 85°C)

Parameter	MT28EW		S29GL-S		Unit	Notes
	Typ	Max	Typ	Max		
Erase						–
Block erase	200	1100	275	1100	ms	–
Erase timeout	50	–	0	–	µs	4
Program (Word mode)						–
Single word	25	200	125	400	µs	–
Write-to-buffer (16 words)	50	–	200	750		–
Write-to-buffer (32 words)	92	460	220	750		–
Write-to-buffer (64 words)	117	600	250	750		1
Write-to-buffer (128 words)	171	900	320	750		1
Write-to-buffer (256 words)	285	1500	420	750		1
Write-to-buffer (512 words)	512	2000	–	–		–
Accelerated full buffered program	410	–	–	–		–
NOP (number of program operations per line)	–	–	–	256		2
Program/Erase Suspend						–
Erase suspend latency time	–	20	–	40	µs	–
Program suspend latency time	–	15	–	40		–
Erase/Program or suspend to next resume (^{t}RES)	100	–	100	–		3
Nonvolatile Protection						–
Set nonvolatile protection bit time	25	200	125	400	µs	–
Clear nonvolatile protection bit time	80	1100	275	1100	ms	–
Blank Check						–
Blank check: main block	3.2	–	7.6	9.0	ms	–

Notes:
1. In applications that apply a shorter timeout value than the MT28EW 128-, 256-, and 512-word BUFFER PROGRAM operation time, some modification may be required to meet the maximum values considering the life cycle application. Most system designs using common Linux should not need to consider the time-out modifications.
2. MT28EW does not require this specification as long as the buffer program is within the 512 word buffer.
3. This typical value allows an ERASE operation to progress to completion. It is important to note that the algorithm might never finish if the ERASE operation is always suspended less than this specification.

4. MT28EW enables the multiple ERASE operation with time-out typical spec of 50µs. The S29GL-S does not support this feature.

Table 12: Read AC Performance Comparison – 3V (–40°C to 85°C)

Parameter	Symbol		MT28EW		S29GL-S		Unit
	Legacy	JEDEC	Min	Max	Min	Max	
Address valid to output valid	^{t}ACC	^{t}AVQV	–	95/70	–	100/90	ns
Page address access	^{t}APA	^{t}AVQV1	–	15/20	–	15/20	ns
OE# LOW to output valid	^{t}OE	^{t}GLQV	–	25	–	25	ns

Table 13: Write AC Performance Comparison – 3V (–40°C to 85°C)

Parameter	Symbol		MT28EW		S29GL-S		Unit
	Legacy	JEDEC	Min	Max	Min	Max	
WRITE cycle time	^{t}WC	–	60	–	60	–	ns
WE# LOW to WE# HIGH	^{t}WP	^{t}WLWH	35	–	25	–	ns
WE# HIGH to WE# LOW	^{t}WPH	^{t}WHWL	20	–	20	–	ns
Input valid to WE# HIGH	^{t}DS	^{t}DVWH	30	–	30	–	ns
Program/Erase valid to RY/BY# LOW	^{t}BUSY	^{t}WHRL	–	90	–	80	ns

Table 14: Power Consumption Comparison (–40°C to 85°C)

Parameter	Symbol	MT28EW		S29GL-S		Unit
		Typ	Max	Typ	Max	
Read						
V_{CC} random read current	I_{CC1}	26	31	55	60	mA
V_{CC} page read curent	I_{CC1}	12	16	9	25	
V_{CC} Standby Current						
128Mb	I_{CC2}	50	120	70	200	µA
256Mb		65	136	70	200	
512Mb		70	150	70	200	
1Gb		75	165	70	200	
Program/Erase						
V_{CC} erase current	I_{CC3}	35	50	45	100	mA
V_{CC} program current	I_{CC3}	35	50	45	100	

Table 15: Power-On and Reset Timings Comparison

Parameter	Symbol		MT28EW		S29GL-S		Unit	Notes
	Legacy	JEDEC	Min	Max	Min	Max		
V_{CC} power valid to RST# HIGH	^{t}VCS	^{t}VCHPH	300	–	300	–	µs	1
RST# LOW to read mode during program erase	^{t}READY	^{t}PLRH	–	25	–	35	µs	
RST# pulse width	^{t}RP	^{t}PLPH	100	–	200	–	ns	
RST# HIGH to CE# LOW, OE# LOW	^{t}RH	^{t}PHEL, ^{t}PHGL	50	–	50	–	ns	
RY/BY# HIGH to CE# LOW, OE# LOW	^{t}RB	^{t}RHEL, ^{t}RHGL	0	–	0	–	ns	–
CE# HIGH to CE# LOW	^{t}CEH	^{t}EHEL	–	–	20	–	ns	2
Initialization voltage	V_{RST}	–	–	–	1.0	–	V	–
Duration of $V_{CC} \leq V_{RST, min}$	–	^{t}PD	–	–	15	–	µs	–
Low V_{CC} lock-out voltage	V_{LKO}	–	2.0	–	2.25	2.5	V	–

Notes:
1. Power supply transitions should only occur when RST# is LOW.
2. Micron MT28EW supports either CE# HIGH or LOW during Flash power-up before ^{t}VCS is met, unlike S29GL-S. Therefore ^{t}CEH does not apply to MT28EW. This difference would not require any migration change.

Note: Generally, most designs have been adapted to Flash power-on timings and should not have conversion problems.

During power-down or voltage drops below V_{LKO} on the S29GL-S device, V_{CC} and V_{IO} must drop below the minimum of V_{CC} Reset ($V_{RST, min}$) for a period of ^{t}PD in order for the device to initialize correctly when V_{CC} and V_{IO} rise again to their operating ranges.

Designs following V_{RST} and ^{t}PD should not induce a negative impact on MT28EW device during conversion. On the MT28EW device, V_{RST} and ^{t}PD should not be applied since power-up initialization is optimized. A complete initialization (^{t}VCS) is needed when the device is powered up from a voltage below the normal operating range. Refer to the Power Supply Decoupling heading in this document to stabilize power supply risks to design risks.

System Validation

Because Linux is a widely used operating system in the embedded application, system-level validations have been performed with the following environment on Micron MT28EW 128Mb, 256Mb, 512Mb, and 1Gb devices.

- ARM9, 3.3V, x16 I/O, CPU: 202.8 MHz
- Memory bus clock: 101.4 Mhz
- Linux version: 2.6.22 and 3.11.6, HZ = 200
- File system: JFFS2 and UBIFS

MTD Validation

The basic functions and stress tests applied by Linux MTD driver have been performed with Linux test project (LTD) utility. It demonstrates robust compatibility and good performance.

Table 16: Typical Write Speed Comparison

Size	MT28EW	S29GL-S	Unit
10KB	1.9	1.0	MB/s
100KB	2.3	1.1	
1MB	2.4	1.1	
4MB	2.4	1.2	

Notes:
1. It is measured through the function that time dd if = /dev/urandom of = /dev/mtd0 bs = 1k count = 20/200/2000/8000 seek = 0 conv = sync. The performance is subject to change by different system application.
2. The typical data is measured on limited samples. MTD driver includes a typical delay time probed from CFI 1Fh (x16) after the Flash WRITE operation kicks off.

Table 17: Typical Format Speed

Format		Size	MT28EW	S29GL-S	Unit
JFFS2	Blank Flash	16MB	17.3	34.1	s
		32MB	34.6	65.1	
	100% Dirty Flash	16MB	19.6	33.1	
		32MB	37.1	64.0	
UBIFS	Blank Flash	16MB	17.9	34.4	
		32MB	34.7	65.5	
	100% Dirty Flash	16MB	19.7	33.2	
		32MB	37.2	65.0	

Notes:
1. It is measured through the function that time flash_eraseall -jq /dev/mtd0; time ubiformat -yq /dev/mtd0. The system performance is subject to change by different system application.
2. The typical data is measured on limited samples. MTD driver includes a typical delay time after the Flash ERASE operation kicks off; namely half of the time-value probed from CFI 21h (x16). It mediates the performance advantage of MT28EW on blank Flash formatting.

File System Validation

All file operations including READ, WRITE, DELETE, and partitions, including FORMAT, MOUNT, and UNMOUNT have been validated on both the JFFS2 and the UBIFS file system.

Stress Tests

Stress reliability test is performed to validate the power loss cycling more than 40,000 times on both chip level and system level. ERASE SUSPEND operation is stressed up to 40,000 cycles. All subsequent READ, WORD PROGRAM, and BUFFER PROGRAM operations after an ERASE SUSPEND command could work successfully.

Related Information

Table 18: Document List

Document/Tool
Parallel NOR Flash Embedded Memory MT28EW datasheet (all densities)
S29GL_128S_01GS_00: rev 07 SPANSION® MirrorBit® Eclipse™ Flash Non-Volatile Memory Family S29GL-S 1-Gbit, 512-Mbit, 256-Mbit, 128-Mbit 3.0 Volt Core with Versatile I/O datasheet
TN-13-12: Software Driver for M29EW NOR Flash Memory
Application Note 309046: Power Loss Recovery for NOR Flash Memory
TN-13-30: System Design Considerations with Micron Flash Memory
TN-13-07: Patching the Linux Kernel and U-Boot for Micron M29 Flash Memory

Notes:
1. Contact your local Micron or distribution sales office to request additional documentation.
2. Visit www.micron.com for technical documentation.

Revision History

Rev. A – 9/14

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992