Technical Note

Migrating from S29GL-N/P Devices to MT28EW NOR Flash Devices

Introduction

This technical note describes the process for converting a system design from the Spansion® S29GL-N or S29GL-P device to the Micron® MT28EW single-level cell NOR Flash device, including 128Mb, 256Mb, 512Mb and 1Gb densities.

The higher reliability and performance characteristics of the MT28EW are ensured through advanced technology and product design improvements. The MT28EW features a large buffer size up to 512 words for advanced program performance. Erase performance is largely improved to meet all variable system design considerations. Moreover, MT28EW supports both ×8 and ×16 data bus for legacy controllers compatibility.

This document was written based on device information available at publication time. In case of inconsistency, information contained in the relevant MT28EW data sheet supersedes the information in this technical note. This document does not provide detailed device information. The standard density-specific device data sheet provides a complete description of device functionality, operating modes, and specifications.

Comparative Overview

The MT28EW is compatible with the S29GL-P and S29GL-N 128Mb, 256Mb, 512Mb, and 1Gb devices, but features superior program and erase performance.

Table 1: Part Number Comparison

Notes 1 to 3 apply to the entire table

Memory Size	Package Type	Part Numbers		
		Micron MT28EW	Spansion S29GL-P	Spansion S29GL-N
1Gb	56-pin TSOP (14mm x 20mm)	MT28EW01GABA1HJS-0SIT	S29GL01GPxxTxxx1x	
		MT28EW01GABA1LJS-0SIT	S29GL01GPxxTxxx2x	
	64-ball LBGA (11mm x 13mm)	MT28EW01GABA1HPC-0SIT	S29GL01GPxxFxxx1x	
		MT28EW01GABA1LPC-0SIT	S29GL01GPxxFxxx2x	
512Mb	56-pin TSOP (14mm x 20mm)	MT28EW512ABA1HJS-0SIT	S29GL512PxxTxxx1x	S29GL512NxxTxIx1x
		MT28EW512ABA1LJS-0SIT	S29GL512PxxTxxx2x	S29GL512NxxTxIx2x
	64-ball LBGA (11mm x 13mm)	MT28EW512ABA1HPC-0SIT	S29GL512PxxFxxx1x	S29GL512NxxFxIx1x
		MT28EW512ABA1LPC-0SIT	S29GL512PxxTxxx2x	S29GL512NxxFxIx2x
256Mb	56-pin TSOP (14mm x 20mm)	MT28EW256ABA1HJS-0SIT	S29GL256PxxTxxx1x	S29GL256NxxTxIx1x
		MT28EW256ABA1LJS-0SIT	S29GL256PxxTxxx2x	S29GL256NxxTxIx2x
	64-ball LBGA (11mm x 13mm)	MT28EW256ABA1HPC-0SIT	S29GL256PxxFxxx1x	S29GL256NxxFxIx1x
		MT28EW256ABA1LPC-0SIT	S29GL256PxxTxxx2x	S29GL256NxxFxIx2x
128Mb	56-pin TSOP (14mm x 20mm)	MT28EW128ABA1HJS-0SIT	S29GL128PxxTxxx1x	S29GL128NxxTxIx1x
		MT28EW128ABA1LJS-0SIT	S29GL128PxxTxxx2x	S29GL128NxxTxIx2x
	64-ball LBGA (11mm x 13mm)	MT28EW128ABA1HPC-0SIT	S29GL128PxxFxxx1x	S29GL128NxxFxIx1x
		MT28EW128ABA1LPC-0SIT	S29GL128PxxTxxx2x	S29GL128NxxFxIx2x

Notes:
1. To integrate line items on a variety of customer applications, the MT28EW device unifies the speed and voltage options.
2. For valid combination details, refer to www.micron.com/products and www.spansion.com.
3. Micron materials support the complete industrial temperature range.

Table 2: Features Comparison

Feature	MT28EW	S29GL-P	S29GL-N	Notes
Process technology	45nm single-level cell (SLC) floating gate	90nm MirrorBit	110nm MirrorBit	1
Density	128Mb 256Mb 512Mb 1Gb	128Mb 256Mb 512Mb 1Gb	128Mb 256Mb 512Mb	
Package	64-ball LBGA (11mm x 13mm), 56-pin TSOP (14mm x 20mm)	64-ball fortified BGA (LAA064) (11mm x 13mm), 56-pin TSOP (14mm x 20mm)	64-ball fortified BGA (LAA064), (11mm x 13mm) 56-pin TSOP (14mm x 20mm)	
Block architecture	Uniform 128KB	Uniform 128KB	Uniform 128KB	
Data bus	x8/x16	x8/x16	x8/x16	
Page read size	16 words	8 words	8 words	2
Extended memory block	128 words (8 + 120)	128 words (8 + 120)	128 words (8 + 120)	
Program write buffer size	256-word (x8 mode) 512-word (x16 mode)	32-word	16-word	3
V_{CC} range	2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V	
V_{CCQ} range	1.65~VCC	1.65~VCC	1.65~VCC	
V_{PP} accelerated (TYP)	9V	12V	12V	4, 5
CFI version	1.3	1.3	1.3	
High voltage auto select (A9)	No	Yes	Yes	4, 6
Individual block write protection	Yes	Yes	Yes	
Permanent block locking (OTP block)	Yes	Yes	Yes	
Hardware protection	Yes	Yes	Yes	
Unlock bypass	Yes	Yes	Yes	4, 5
Chip erase	Yes	Yes	Yes	
RY/BY# pin	Yes	Yes	Yes	
Blank check	Yes	No	No	7
Multiblock erase	Yes	Yes	Yes	
Data polling	Yes	Yes	Yes	
EFI CRC	Yes	No	No	

Notes:
1. MT28EW SLC floating gate technology provides improved performance and optimized quality and reliability.
2. Although the MT28EW features a larger page read size than the S29GL-P, no software updates are required during migration. However, software updates leveraging the

MT28EW device's larger page read buffer can yield improved read performance. To configure the MT28EW device's software, query CFI word address 4Ch.

3. Although the MT28EW features a larger program write buffer than either the S29GL-P or S29GL-N, no software updates are required during migration. However, software updates leveraging the MT28EW device's larger write buffer can yield improved performance. To configure the MT28EW device's software, query CFI word address 2Ah on the buffer size option, in either x8 or x16 mode (Refer to TN-13-07 for detail patch).
4. To avoid damaging the device, designs applying V_{PP}/WP# voltages higher than 9.5V (MAX) should be modified. V_{PP}/WP# should not remain at V_{PPH} for more than 80 hours cumulative.
5. By applying 9V (nominal) to the V_{PP}/WP# pad, the MT28EW device supports V_{PPH} unlock bypass, accelerated buffered programming, and accelerated chip erase operations. The 56-pin TSOP package pin 16 should be modified, and the 64-ball LBGA package ball B4 should be modified.
6. The MT28EW device does not support high voltage auto select on address A9. Instead, use the following command sequence to enter auto select mode: AAh/55h/90h. Applying 12 volts to address A9 or V_{PP} may damage the device.
7. Refer to the Micron datasheet for detailed blank check command sets.

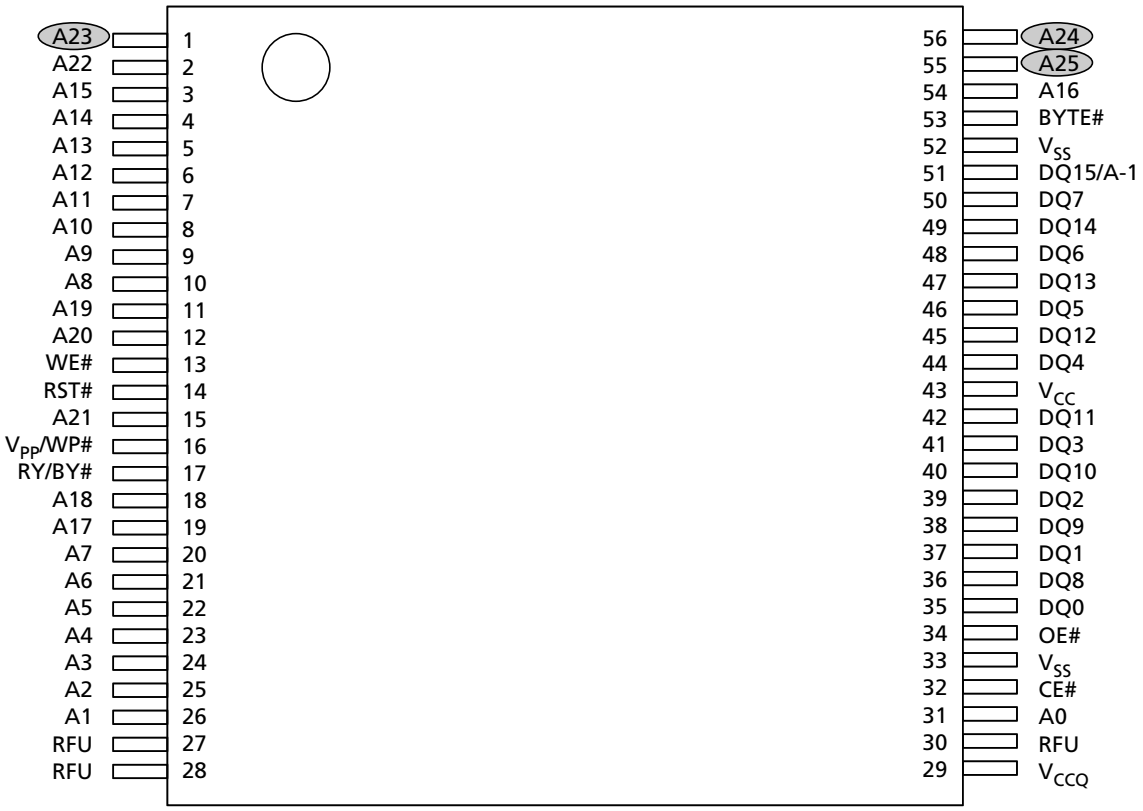
Hardware and Mechanical Considerations

Packages and Ballouts

The MT28EW device is available in 56-pin TSOP and 64-ball LBGA packages, both lead-free. For compatibility, the pin and ball assignments and the physical dimensions are equivalent to the S29GL-P and S29GL-N.

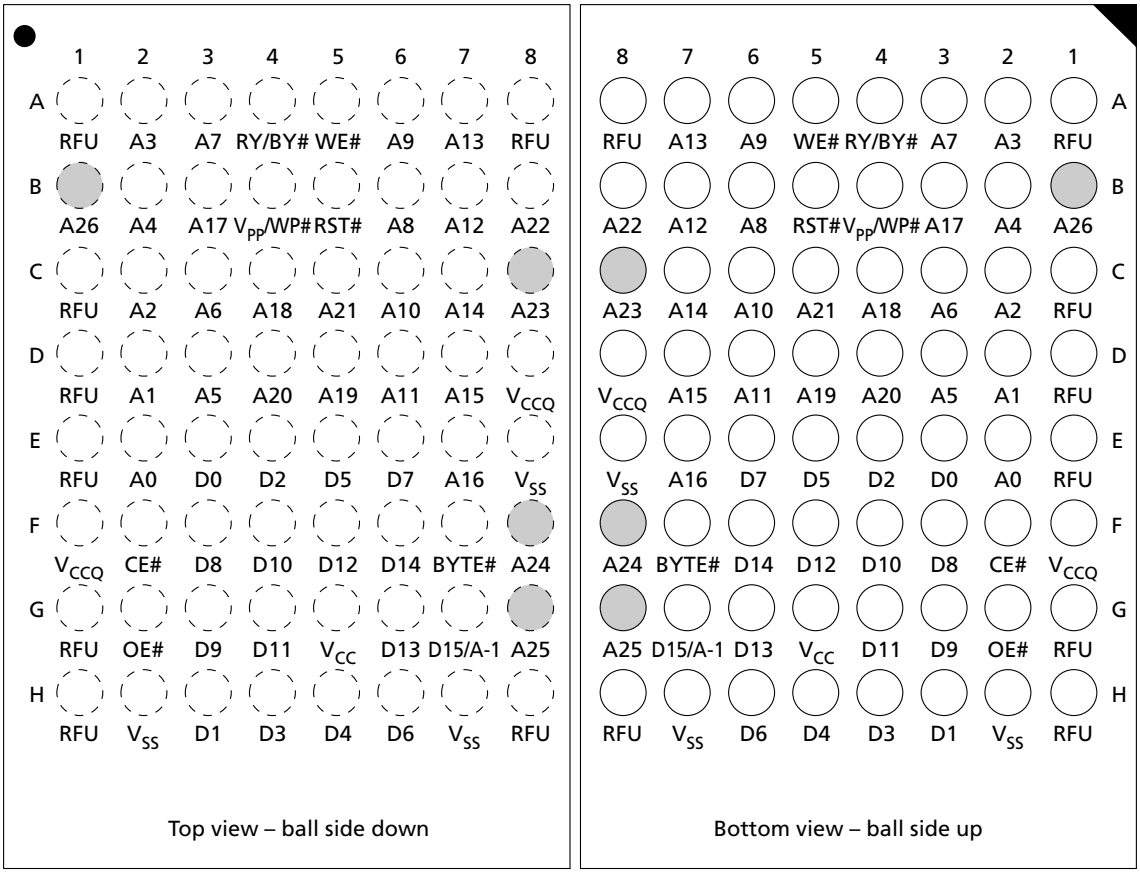
Systems migrating from a fortified BGA to an LBGA should not need to modify the re-flow process in manufacturing.

Figure 1: 56-Pin TSOP (Top View)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256Mb and above; otherwise, it is RFU.
3. A24 is valid for 512Mb and above; otherwise, it is RFU.
4. A25 is valid for 1Gb; otherwise, it is RFU.

Figure 2: 64-Ball LBGA



Notes:
1. A-1 is the least significant address bit in x8 mode.
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3. A24 is valid for 512Mb and above; otherwise, it is RFU.
4. A25 is valid for 1Gb; otherwise, it is RFU.

Signals

Table 3: Signal Comparison

MT28EW	S29GL-P & S29GL-N	Type	Description
A[MAX:0]	A[MAX:0]	Input	Address inputs
BYTE#	BYTE#	Input	Byte/Word organization select cannot be floated
CE#	CE#	Input	Chip enable
OE#	OE#	Input	Output enable
RST#	RESET#	Input	Reset
WE#	WE#	Input	Write enable
V_{PP}/WP#	WP#/A_{CC}	Input	Acceleration power/write protect input
DQ15/A-1	DQ15/A-1	I/O or Input	Data input/output or address input
DQ[14:8]	DQ[14:8]	I/O	Data inputs/outputs
DQ[7:0]	DQ[7:0]	I/O	Data inputs/outputs
RY/BY#	RY/BY#	Output	Ready/Busy
V_{CC}	V_{CC}	Supply	Supply voltage
V_{CCQ}	V_{IO}	Supply	Input/Output buffer supply voltage
V_{SS}	V_{SS}	–	Ground
NC	NC	–	No connect

Input/Output Capacitance

Table 4: Input/Output Capacitance Comparison

Parameter	MT28EW		S29GL-P		S29GL-N		Unit
	Min	Max	Min	Max	Min	Max	
C_{IN}	3	11	6	10	3.5	9	pF
C_{OUT}	3	7	10	12	3.9	12	pF

Note: 1. C_{IN} values for RESET, WP#/A_{CC}, and CE# in the S29GL-N/P device are likely higher than the listed value.

Power Supply Decoupling

Flash memory devices require careful power supply decoupling to prevent external transient noise from affecting device operations, and to prevent internally generated transient noise from affecting other devices in the system.

Ceramic chip capacitors of 0.01µF to 0.1µF should be used between each V_{CC}, V_{CCQ}, and V_{PP} supply connection or system ground pin. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the device package, or on the opposite side of the printed circuit board close to the center of the device package footprint.

Larger electrolytic or tantulum bulk capacitors (4.7µF to 33.0µF) should also be distributed as needed throughout the system to compensate for voltage sags and surges caused by circuit trace inductance.

Transient current magnitudes depend on the capacitive and inductive loading on the device's outputs. For best signal integrity and device performance, high-speed design rules should be used when designing the printed-circuit board. Final signal reflections (overshoot and undershoot) may vary by each system.

Software Considerations

Command Set

The MT28EW command set is fully compatible with that of S29GL-P and S29GL-N; therefore, no command change in the software is required. Micron provides some unique commands to support enhanced features such as EFI Blank check and EFI CRC functions.

Manufacturer ID and Auto Select Comparison

On the MT28EW, the only way to use auto select mode is to issue an AUTO SELECT ENTRY (90h) command. The S29GL-N/S29GL-P can use auto select mode via a high voltage (A9) method. Micron and Spansion have different manufacturer IDs; therefore, a slight modification in the software is required during migration.

The secure version of the MT28EW device does not have the same manufacturer ID as the standard version. To obtain the manufacturer ID of the secure version, contact your local Micron sales offices for MT28EW Security Addendum.

Table 5: Auto Select Comparison – Word Mode

Description		Address	MT28EW	S29GL-P	S29GL-N
Manufacturer ID		(Base) + 00h	0089h	0001h	0001h
Device ID (cycle 1)		(Base) + 01h	227Eh	227Eh	227Eh
Device ID (cycle 2)	128Mb	(Base) + 0Eh	2221h	2221h	2221h
	256Mb		2222h	2222h	2222h
	512Mb		2223h	2223h	2223h
	1Gb		2228h	2228h	–
Device ID (cycle 3)		(Base) + 0Fh	2201h	2201h	2201h
Protection register indicator – V_{PP}/WP# locks highest block	Factory locked	(Base) + 03h	0099h	0099h	0098h
	Factory unlocked		0019h	0019h	0018h
Protection register indicator – V_{PP}/WP# locks lowest block	Factory locked		0089h	0089h	0088h
	Factory unlocked		0009h	0009h	0008h
Block protection	Protected	(Base) + 02h	0001h	0001h	0001h
	Unprotected		0000h	0000h	0000h

Unlock Bypass Mode

When the MT28EW device is in unlock bypass mode (AAh/55h/20h), the use of auto select mode (AAh/55h/90h) is not recommended. However, if auto select mode is used to read information when the device is in unlock bypass mode, an additional F0h command must be issued after AUTO SELECT READ to return to unlock bypass mode. Then, a subsequent auto select mode command must be issued to read out correct ID information.

This additional command is not required for S29GL device.

In the following code example, the F0h command is written to any address during the first cycle:

```
FlashWrite(ANY_ADDR, (uCPUBusType)CMD(0x00F0));
```

To access auto select information, use the following command sequence (AAh/55h/90h), but only when the device is not in unlock bypass mode. The following example demonstrates how to use auto select mode to read information from the device:

```
ReturnType ReadAutoSelectCode(uCPUBusType *addr, uCPUBusType *ucrCode)
{
/*Send the auto select command */
FlashWrite(ConvAddr(0x00555), (uCPUBusType)CMD(0x00AA)); /* first cycle */
FlashWrite(ConvAddr(0x002AA), (uCPUBusType)CMD(0x0055)); /* second cycle */
FlashWrite(ConvAddr(0x00555), (uCPUBusType)CMD(0x0090)); /* third cycle */

/* Read the code */
*ucrCode = FlashRead(addr);

/* Return to read array mode */
FlashWrite(ANY_ADDR, (uCPUBusType)CMD(0x00F0); /* first cycle: write 0x00F0 to any
address */

/* Check flash response (more flashes could give different results) */
return FlashResponseIntegrityCheck(ucrCode);
}
```

EXIT PROTECTION COMMAND SET

The Micron device provides three software protection modes: volatile, nonvolatile, and password protection. The device is shipped with all blocks unprotected. On first use, the device can be activated in either the nonvolatile protection or password protection mode.

The EXIT PROTECTION COMMAND SET (90/00h) command is used to exit the lock register, password protection, nonvolatile protection, volatile protection, and nonvolatile protection bit lock bit command set modes and return the device to read mode. The second cycle for the Micron device must be 00h while the Spansion device may accept other command codes to exit the above modes.

CFI Comparison

CFI differences exist between MT28EW and S29GL-P/S29GL-N due to device features and performance characteristics.

Table 6: CFI Comparison

Address	Description	MT28EW	S29GL-P	S29GL-N	Notes
1Dh	V_{PPH} (programming) supply minimum PROGRAM/ERASE voltage	0085	0000	0000	
	Bits[7:4] hex value in volts				
	Bits[3:0] BCD value in 100mV				

Table 6: CFI Comparison (Continued)

Address	Description	MT28EW		S29GL-P		S29GL-N	Notes
1Eh	V_{PPH} (programming) supply maximum PROGRAM/ERASE voltage	0095		0000		0000	
	Bits[7:4] hex value in volts						
	Bits[3:0] BCD value in 100mV						
1Fh	Typical timeout for single byte/word PROGRAM = 2^nµs	0005		0006		0007	
20h	Typical timeout for maximum size BUFFER PROGRAM = 2^nµs	0009		0006		0007	1
21h	Typical timeout for individual BLOCK ERASE = 2^nms	0008		0009		000A	
22h	Typical timeout for full-chip ERASE = 2^nms	128Mb	000F	128Mb	0010	0000 (not supported)	
		256Mb	0010	256Mb	0011		
		512Mb	0011	512Mb	0012		
		1Gb	0012	1Gb	0013		
23h	Maximum timeout for byte/word PROGRAM = 2^n times typical timeout	0003		0003		0003	
24h	Maximum timeout for BUFFER PROGRAM = 2^n times typical timeout	0002		0005		0005	
25h	Maximum timeout per individual BLOCK ERASE = 2^n times typical timeout	0003		0003		0004	
26h	Maximum timeout for chip ERASE = 2^n times typical timeout	0003		0002		0000	
2Ah	Maximum number of bytes in multiple-byte write = 2^n	x8 mode	08	0006		0005	
		x16 mode	000A				
45h	Address-sensitive unlock (bits[1:0])	001C		0014		0010	
	0 = required, 1 = not required						
	Silicon revision number (bits[7:2])						
4C	Page mode	0003		0002		0002	
	00 = not supported						
	01 = 4-word page						
	02 = 8-word page						
	03 = 16-word page						
4D	V_{PPH} supply minimum PROGRAM/ERASE voltage	0085h		00B5h		00B5h	
	Bits[7:4] hex value in volts						
	Bits[3:0] BCD value in 100mV						

Table 6: CFI Comparison (Continued)

Address	Description	MT28EW	S29GL-P	S29GL-N	Notes
4E	V_{PPH} supply maximum PROGRAM/ ERASE voltage	0095h	00C5h	00C5h	
	Bits[7:4] hex value in volts				
	Bits[3:0] BCD value in 100mV				

Note: 1. S29GL-N/P device defines this value as a minimum instead of a maximum; that is, the typical timeout for a minimum size buffer write = 2^nµs

Performance Comparison

The MT28EW features significantly improved program and erase performance.

Table 7: Program and Erase Performance Comparison (Word Mode)

Parameter	MT28EW		S29GL-P		S29GL-N		Unit
	Typ	Max	Typ	Max	Typ	Max	
Block Erase							
Block erase	200	1100	500	3500	500	3500	ms
Accelerated chip Erase							
128Mb	23	-	-	-	-	-	s
256Mb	47	-	-	-	-	-	
512Mb	95	-	-	-	-	-	
1Gb	190	-	-	-	-	-	
Chip Erase							
128Mb	26	–	64	–	64	–	s
256Mb	52	–	128	–	128	–	
512Mb	104	–	256	–	256	–	
1Gb	208	–	512	–	–	–	
Program/Erase Suspend							
Erase suspend latency time	15	20	5	20	5	20	µs
Program suspend latency time	10	15	5	15	5	20	
Program, x16							
Single word	25	200	60	480	60	–	µs
Write-to-buffer (16 words)	50 (0.64MB/s)	–	–	–	240 (0.07 MB/s)	–	
Write-to-buffer (32 words)	92 (0.7 MB/s)	460	480 (0.07 MB/s)	–	–	–	
Write-to-buffer (64 words)	117 (1.1 MB/s)	600	–	–	–	–	
Write-to-buffer (128 words)	171 (1.5 MB/s)	900	–	–	–	–	
Write-to-buffer (256 words)	285 (1.8 MB/s)	1500	–	–	–	–	
Write-to-buffer (512 words)	512 (2.0 MB/s)	2000	–	–	–	–	
Accelerated full buffered program	–	410 (2.5 MB/s)	–	–	–	–	

Table 8: Read AC Performance Comparison – 3V

Parameter	Symbol		MT28EW		S29GL-P		S29GL-N		Unit	Notes
	Legacy	JEDEC	Min	Max	Min	Max	Min	Max		
Address valid to output valid	^{t}ACC	^{t}AVQV	–	95	–	90–110	–	90–110	ns	1
Page address access	^{t}APA	–	–	20	–	25	–	25	ns	
OE# LOW to output valid	^{t}OE	^{t}GLQV	–	25	–	25	–	25	ns	

Note: 1. For MT28EW, maximum value is 70ns for 128M/256M only.

Table 9: Power Consumption Comparison

Parameter	Symbol	MT28EW		S29GL-P		S29GL-N		Unit
		Typ	Max	Typ	Max	Typ	Max	
Read								
V_{CC} random read current	I_{CC1}	26	31	30	55	30	50	mA
V_{CC} page read curent	I_{CC1}	12	16	1	10	1	10	
Standby								
1Gb Vcc standby current	I_{CC2}	75	230	1	5	1	5	µA
512Mb V_{CC} standby current		70	200	1	5	1	5	
256Mb V_{CC} standby current	I_{CC2}	65	136	1	5	1	5	
128Mb V_{CC} standby current		50	120	1	5	1	5	
Program/Erase								
V_{CC} erase current	I_{CC3}	35	50	50	90	50	90	mA
V_{CC} program current	I_{CC3}	35	50	50	90	50	90	

Power-on and Reset Timings

Because many of the more common processors support the MT28EW timings, there should be no adverse effect from timing differences.

Table 10: Reset Timing Comparison

Condition/Parameter	Symbol		MT28EW		S29GL-P		S29GL-N		Unit
	Legacy	JEDEC	Min	Max	Min	Max	Min	Max	
V_{CC} power valid to RST# HIGH	^{t}VCS	^{t}VCHPH	300	–	35	–	50	–	µs
RST# LOW to read mode during program or erase	^{t}READY	^{t}PLRH	–	25	–	35	–	20	µs
RST# pulse width	^{t}RP	^{t}PLPH	100	–	3500	–	500	–	ns
RST# HIGH to CE# LOW, OE# LOW	^{t}RH	^{t}PHEL, ^{t}PHGL	50	–	200	–	50	–	ns
RY/BY# HIGH to CE# LOW, OE# LOW	^{t}RB	^{t}RHEL, ^{t}RHGL	0	–	0	–	0	–	ns

Related Information

Table 11: Document List

Document/Tool
Parallel NOR Flash Embedded Memory MT28EW datasheet (all densities)
S29GL-P_00: SPANSION® MirrorBit® S29GL-P 1-Gbit, 512-Mbit, 256-Mbit, 128-Mbit 3.0 Volt-only Page Mode Flash Memory datasheet
S29GL-N_00: SPANSION® MirrorBit® S29GL-N 512-Mbit, 256-Mbit, 128-Mbit 3.0 Volt- only Page Mode Flash Memory datasheet
TN-13-12: Software Driver for M29EW NOR Flash Memory
Application Note 309046: Power Loss Recovery for NOR Flash Memory
TN-13-30: System Design Considerations with Micron Flash Memory
TN-13-07: Patching the Linux Kernel and U-Boot for Micron M29 Flash Memory

Notes:
1. Contact your local Micron or distribution sales office to request additional documentation.
2. Visit http://www.micron.com for technical documentation.

Revision History

Rev. B – 09/15

- Updated performance based on latest datasheet
- Removed 2Gb density information

Rev. A – 05/14

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992