

Technical Note

Asynchronous Page Mode Read in M29W320DT/B 32Mb, 3V Supply NOR Flash Memory (Automotive Grade) Devices

Introduction

This technical note describes the asynchronous page mode read feature available in the following 32Mb, 3V supply NOR flash memory (automotive grade) devices:

- M29W320DB70N3E/F
- M29W320DB70ZA3F
- M29W320DB7AN6E/F
- M29W320DB7AZA6E/F
- M29W320DB80ZA3E/F
- M29W320DT70N3E

See the M29W320DT/B data sheet for additional information on these devices.

General Description

The M29W320D is a 32Mb (4Mb x 8 or 2Mb x 16) non-volatile memory device that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6 V) supply.

The devices specified in this technical note support asynchronous page mode read and page read from all blocks of the array. See the M29W320DT/B data sheet for more information on array organization.

The asynchronous page mode read feature consists of:

- Page size: 4 words or 8 bytes
- Page access: 25ns

Figure 1: Logic Diagram

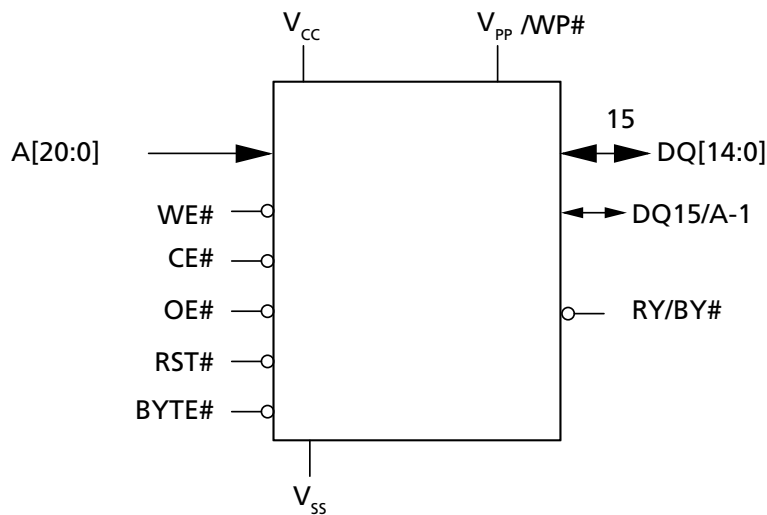




Table 1: Signal Names

A[20:0]	Address Inputs
DQ0-DQ7	Data Input/Output
DQ8-DQ14	Data Input/Output
DQ15A-1	Data Input/Output or Address Input
CE#	Chip Enable
OE#	Output Enable
WE#	Write Enable
RST#	Reset/Block temporary unprotect
RY/BY#	Ready/Busy output
BYTE#	Byte/word organization select
V _{CC}	Core Power Supply
V _{PP} /W _P #	V _{PP} /Write Protect
V _{SS}	Ground
NC	Not Connected Internally

PAGE READ

BUS READ operations read from the memory cells, or specific registers, in the command interface. To accelerate the READ operation, the memory array can be read in page mode, where data is internally read and stored in a page buffer.

Page size is 4 words (8 bytes) and is addressed by address inputs A[1:0] in x16 bus mode and A[1:0] plus DQ15/A-1 in x8 bus mode.

A valid BUS READ operation involves setting the desired address on the address inputs, applying a LOW signal (V_{IL}) to Chip Enable (CE#) and Output Enable (OE#), and keeping Write Enable (WE#) HIGH (V_{IH}). The data input/outputs will output the value. See the following figure and table for details of when the output becomes valid.

Figure 2: Page Read AC Waveforms

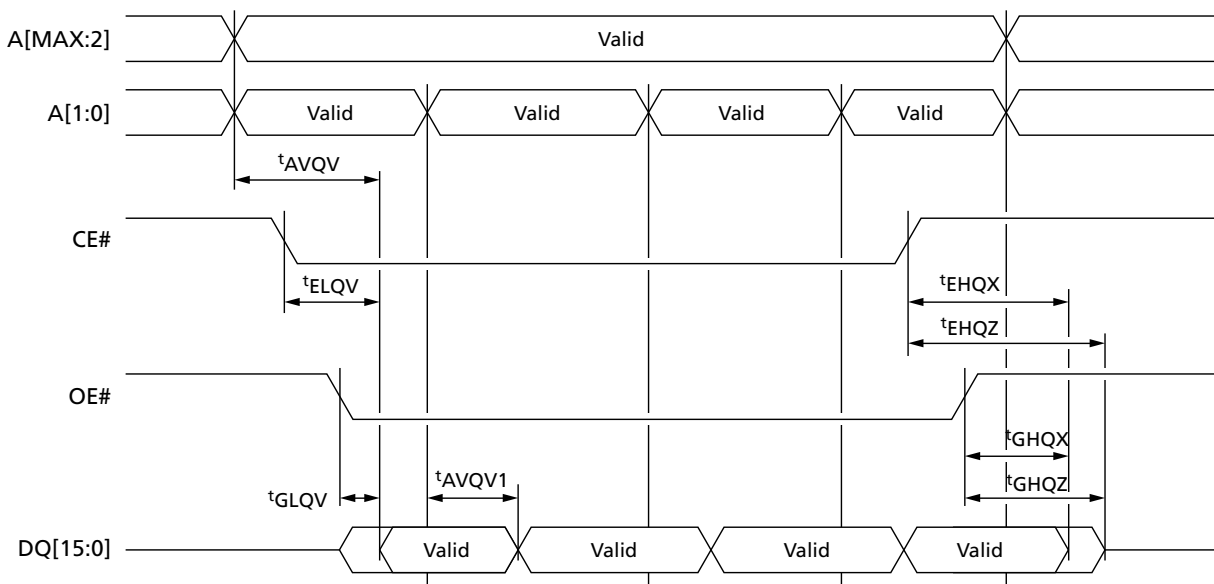




Table 2: Page Read AC Characteristics

Parameter	Symbol	Alt	Test Condition	M29W320D		Unit	
				70/7A	80		
Address valid to output valid	t_{AVQV}	t_{ACC}	CE# = V_{IL} , OE# = V_{IL}	MAX	70	80	ns
Address valid to output valid (page)	t_{AVQV1}	t_{PAGE}	CE# = V_{IL} , OE# = V_{IL}	MAX	25	25	ns
CE# LOW to output transition	t_{ELQX}^1	t_{LZ}	OE# = V_{IL}	MIN	0	0	ns
CE# LOW to output valid	t_{ELQV}	t_{CE}	OE# = V_{IL}	MAX	70	80	ns
OE# LOW to output transition	t_{GLQX}^1	t_{OLZ}	CE# = V_{IL}	MIN	0	0	ns
OE# LOW to output valid	t_{GLQV}	t_{OE}	CE# = V_{IL}	MAX	30	30	ns
CE# HIGH to output High-Z	t_{EHQZ}^1	t_{HZ}	OE# = V_{IL}	MAX	25	25	ns
OE# HIGH to output High-Z	t_{GHQZ}^1	t_{DF}	OE# = V_{IL}	MAX	25	25	ns

Note: 1. Sampled only; not 100% tested.



Revision History

Rev. A – 9/12

- Initial release

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