AN2685
Application note

How to migrate from S29GL128P to M29W128GH/L Flash memories

Introduction

The objective of this application note is to explain how to migrate an application based on the S29GL128P Flash memory to an M29W128GH/L Flash memory. The purpose of this document is not to provide detailed information on the devices, but to highlight the similarities and differences between them. The comparison takes into consideration the signal descriptions, packages, architecture, software command set, performance, and block protections.

The S29GL128P and M29W128GH/L are 128 Mbit (8 Mb x 16 or 16 Mb x 8) Flash memories that can be read, erased and reprogrammed using a single low supply voltage.

Both memories are divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

Program and erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

Group of blocks can be protected to prevent accidental program or erase commands from modifying the memory. On both devices, the highest or lowest memory block can also be protected by using a hardware method.

All devices have an extra block, the extended block, of 128 words (256 bytes). It can be accessed using a dedicated command. The extended block can be protected and so is useful for storing security information. However the protection is not reversible, once protected the protection cannot be undone.

In this document, the S29GL128P, highest and lowest block protected (01 and 02 model), will be referred to as S29GL128P, and the M29W128GH (highest block protected) and the M29W128GL (lowest block protected) will be referred to as M29W128G unless otherwise specified.

Please refer to the S29GL128P and M29W128G datasheets for additional information on devices.

Contents

List of tables

List of Figures

1 Memory architecture and protection groups

The S29GL128P and the M29W128G memory arrays are divided into uniform blocks. In particular, they have 128 blocks of 64 Kwords (128 Kbytes) each.

Both devices have an extended memory block of 128 words in x 16 mode or of 256 bytes in x 8 mode. See ***Section 3 Software command set*** for a description of the extended memory block commands.

On the S29GL128P and M29W128G, all blocks are protected individually. The protection granularity is always 64 Kwords or 128 Kbytes.

2 Hardware migration

This section provides a detailed comparison between S29GL128P and M29W128G signals and package pin-out.

2.1 Signal description

Table 1 gives a comparison between the S29GL128P and M29W128G signals.

On both devices, the V_{PP} function allows the memory to use an external high voltage power supply to reduce the time required for fast program operations. The Write Protect (WP) function provides a hardware method of protecting the outermost memory block:

- When V_{PP}/WP is Low, $V_{IL,}$ the highest or lowest block is protected on both the M29W128G and S29GL128P devices.
- When V_{PP}/WP is High, V_{IH}, the memory reverts to the previous protection status of the outermost block.

Upon customer request, on the M29W128G devices, applying 12 V to the V_{PP}/WP pin will temporarily unprotect any block previously protected (including the two outermost blocks). In addition, the V_{PP}/WP pin can be left floating or unconnected due to an internal pull-up.

In both devices, V_{CCQ} provides the power supply to the I/O pins and enable all outputs to be powered independently from V_{CC}.

Table 1 Signal description for the S29GL128P and M29W128G devices

Name		Description	Direction
S29GL128P	**M29W128G**		
A0-A22		Address inputs	Inputs
DQ0-DQ7		Data inputs/outputs	I/O
DQ8-DQ14		Data inputs/outputs	I/O
DQ15A–1 (or DQ15)		Data input/output or address input (or data input/output)	I/O
CE	E	Chip Enable	Input
OE	G	Output Enable	Input
WE	W	Write Enable	Input
RESET	RP	Reset/Block Temporary Unprotect	Input
RY/BY	RB	Ready/Busy output	Output
BYTE		Byte/word organization select	Input
V_{CC}		Supply voltage	Supply
WP/ACC	V_{PP}/WP	Supply voltage for fast program (optional) or write protect	Input
V_{SS}		Ground	–

2.2 Packages

The S29GL128P and M29W128G are delivered in TSOP56 - 14 x 20 mm, and TBGA64 - 10 x 13 mm, 1 mm pitch packages. Compared with S29GL128P, the package size of M29W128G TBGA64 is smaller than that of S29GL128P BGA64 - 11 x 13mm. In addition, M29W128G holds a different BGA ball size from what S29GL128P does. The BGA ball size of M29W128G ranges from 0.35mm to 0.5mm while the BGA ball size of S29GL128P ranges from 0.5mm to 0.7mm.

The M29W128G is fully pin-to-pin compatible with the S29GL128P. See ***Figure 1*** and ***Figure 2***, in conjunction with ***Table 1***.

Refer to the S29GL128P and M29W128G datasheets for details on the packages.

Figure 1 S29GL128P TSOP56 connections

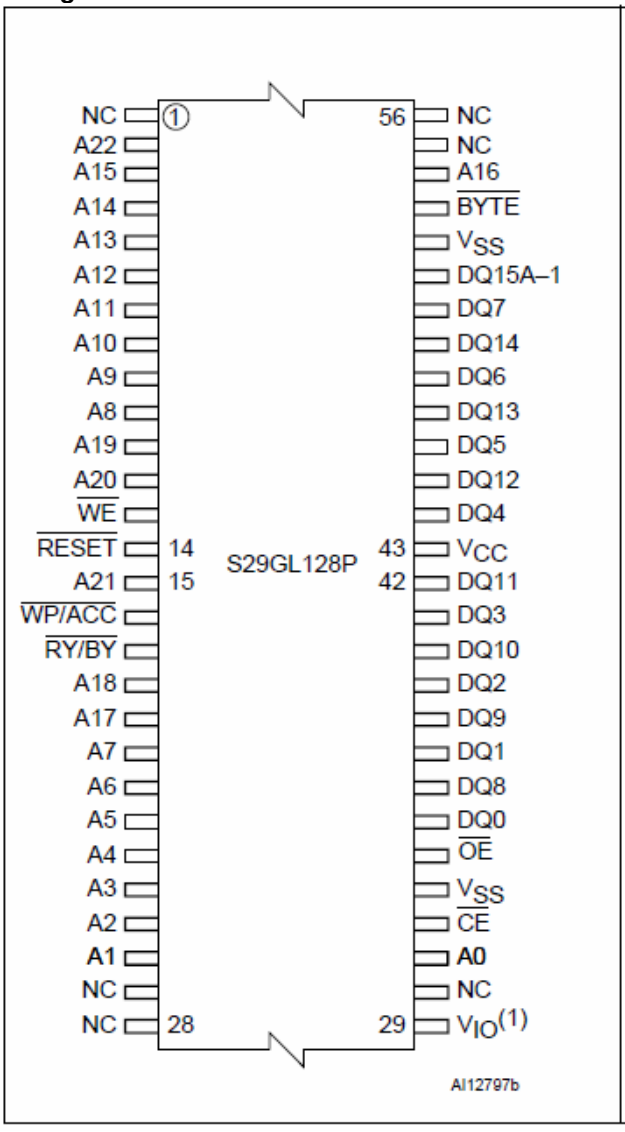
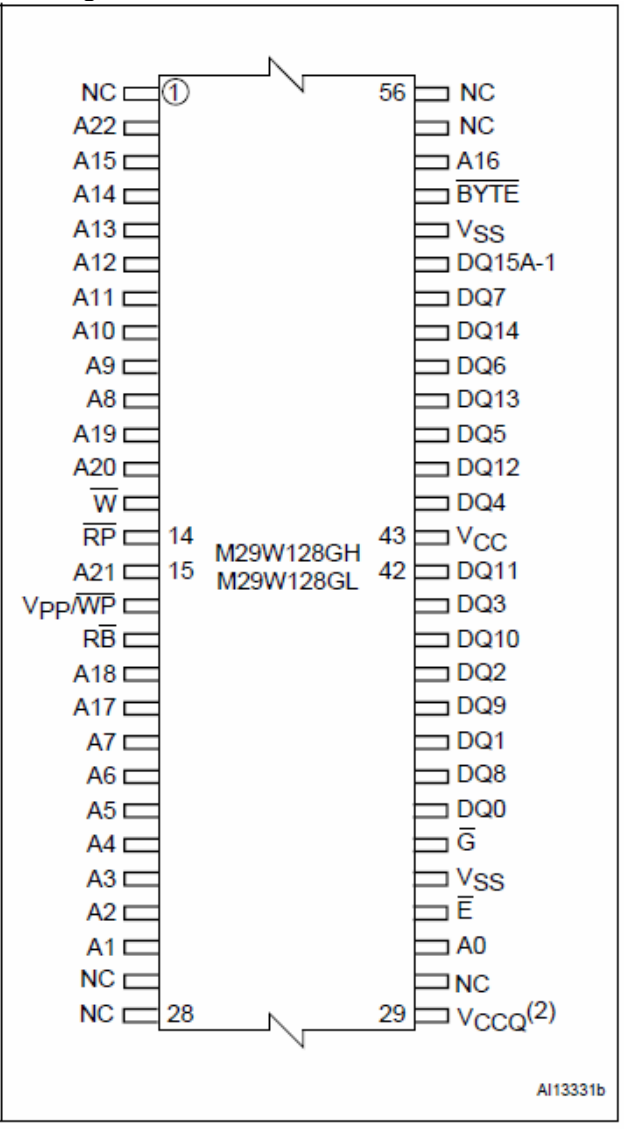


Figure 2 M29W128G TSOP56 connections



1. V_{IO} = 1.65V to V_{CC}
2. V_{CCQ} = 1.65V to V_{CC}

Figure 3 S29GL128P TBGA64 connections

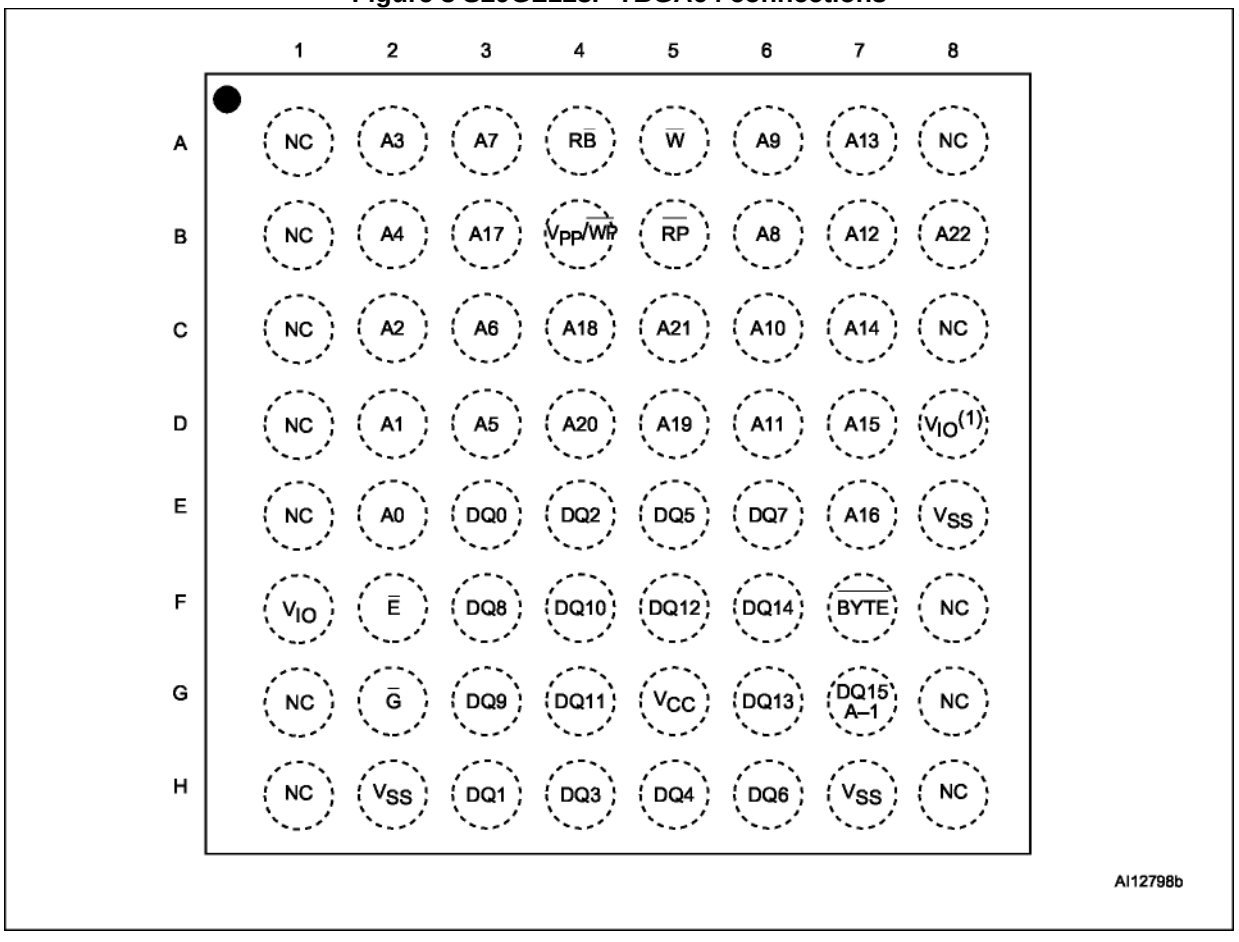
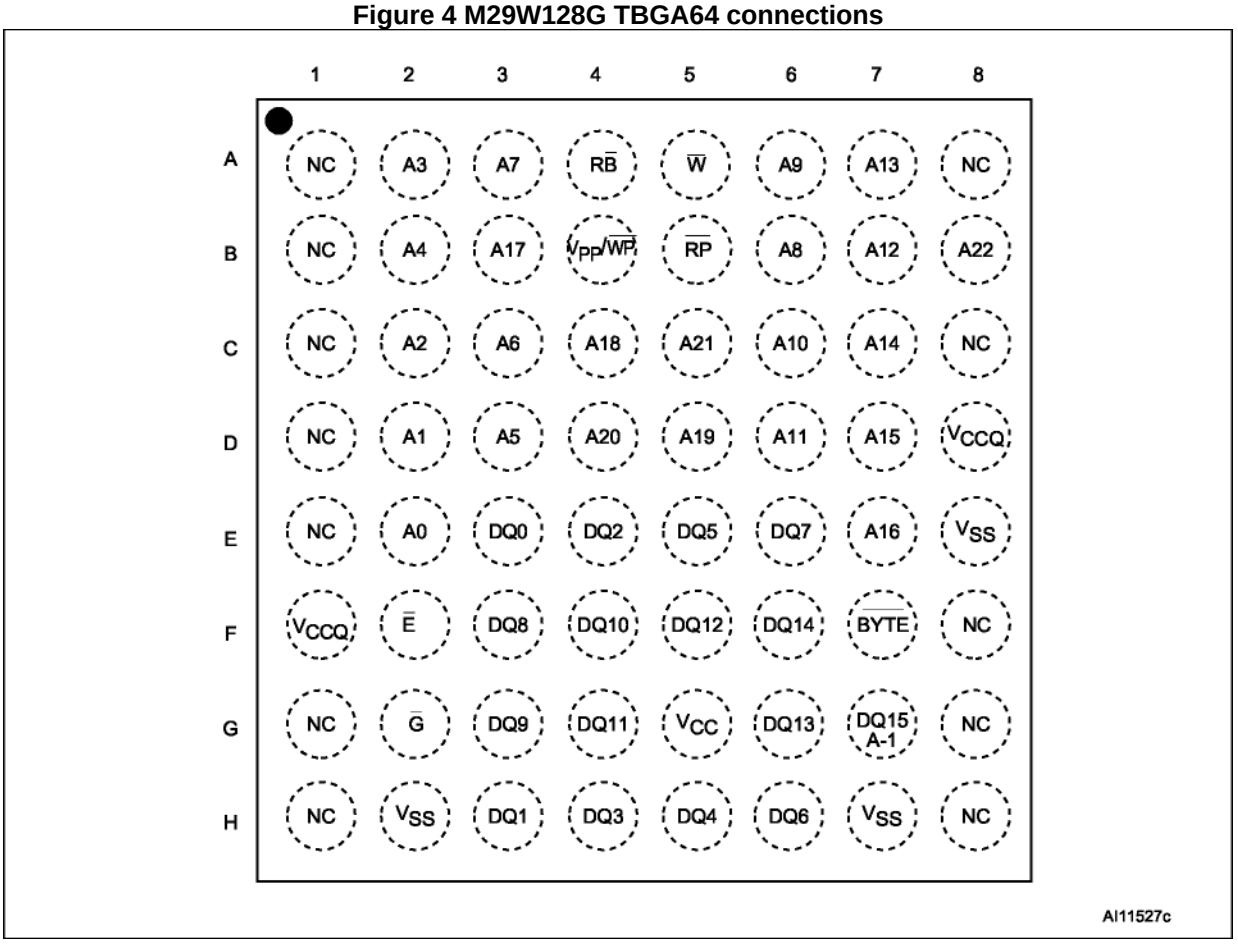


Figure 4 M29W128G TBGA64 connections



3 Software command set

The S29GL128P and M29W128G feature an identical set of standard commands. The commands are compliant with the JEDEC standard.

Table 2 Command set

Command	S29GL128P	M29W128G
Read/Reset	X	X
Auto Select	X	X
Program	X	X
Write Buffer	X	X
Unlock Bypass	X	X
Unlock Bypass Program	X	X
Unlock Bypass Reset	X	X
Chip Erase	X	X
Block Erase	X	X
Program/Erase Suspend	X	X
Program/Erase Resume	X	X
Read CFI Query	X	X
Enter Extended Block	X	X
Exit Extended Block	X	X
Enhanced Buffered Program	-	X

3.1 Fast program commands

The S29GL128P and the M29W128G devices both feature fast program commands. Since the write to buffer program is available on both devices, it is recommended to use this command if a minimum number of changes is required for the migration. On the other side, to reach the best programming speed with M29W128G devices, it is recommended to use enhanced buffered program with V_{PP}=V_{PPH} (see ***Table 3 M29W128G fast program commands (16-bit mode)*** and ***Table 6 M29W128G fast program commands (8-bit mode)***).

The Enhanced Buffered Program command is only available on M29W128G devices. It is valid in x 16 mode only and makes use of the device's 256-word write buffer to speed up programming. To use the Enhanced Buffered Program command, all the 256 words must be loaded into the write buffer in an increasing address order. Each write buffer has the same A22-A8 addresses. The Enhanced Buffered Program command dramatically reduces system programming time.

Table 3 M29W128G fast program commands (16-bit mode)

Command	Length	Bus write operations(1)											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer Program	N+5	555	AA	2AA	55	BAd	25	BAd	N(2)	PA (3)	PD	WBL (4)	PD
Write to Buffer Program Confirm	1	BAd (5)	29										
Buffered Program Abort and Reset	3	555	AA	2AA	55	555	F0						

1. X Don't care, PA Program Address, PD Program Data, BAd Any address in the Block, WBL Write Buffer Location. All values in the table are in hexadecimal.
2. The maximum number of cycles in the command sequence is 36. N+1 is the number of words to be programmed during the write to buffer program operation.
3. Each buffer has the same A22-A5 addresses. A0-A4 are used to select a word within the N+1 word page.
4. The 6th cycle has to be issued N time. WBL scans the word inside the page.
5. BAd must be identical to the address loaded during the write to buffer program 3rd and 4th cycles.

Table 4 S29GL128P Write to Buffer command (16-bit mode)

Command	Cycles	Bus write cycles											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer(1)	WC + 5	555	AA	2AA	55	BA(2)	25	BA(2)	WC(2)	$PA_{(2)}$	PD(2)	WBL(2)	PD(2)

1. The total number of cycles in the command sequence is determined by the number of words to be written to the write buffer. The maximum number of cycles is 20.
2. BA Block Address, WC Number of words to be programmed - 1, PA Program Address, PD Program Data, WBL Write Buffer Location (address must be within the same write buffer page as PA).

Table 5 M29W128G enhanced buffered program commands (16-bit mode)

Command	Length	Bus write operations																	
		1st		2nd		3rd		4th			...		257th		258th	259th			260th
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Enhanced Buffered Program	259	555	AA	2AA	55	BAd	33	BAd (00)	Data	...	...					BAd (FF)	Data		
Enhanced Buffered Program Confirm	1	BAd (00)	29																

Table 6 M29W128G fast program commands (8-bit mode)

Command	Length	Bus write operations(1)																	
		1st		2nd		3rd		4th		5th		6th			7th		8th		9th
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer Program	N+5	AAA	AA	555	55	BAd	25	BAd	N(2)	PA(3)	PD	WBL	PD						
Write to Buffer Program Confirm	1	BAd(5)	29																
Buffered Program Abort and Reset	3	AAA	AA	555	55	AAA	F0												

1. X Don't care, PA Program Address, PD Program Data, BAd Any address in the Block, WBL Write Buffer Location. All values in the table are in hexadecimal.
2. The maximum number of cycles in the command sequence is 68. N+1 is the number of bytes to be programmed during the Write to Buffer Program operation.
3. Each buffer has the same A22-A5 addresses. A0-A4 and A-1 are used to select a byte within the N+1 byte page.
4. The 6th cycle has to be issued N time. WBL scans the word inside the page.
5. BAd must be identical to the address loaded during the write to buffer program 3rd and 4th cycles.

Table 7 S29GL128P Write to Buffer command (8-bit mode)

Command	Length	Bus write cycles											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer(1)	BC+5	AAA	AA	555	55	BA(2)	25	BA	BC(2)	PA(2)	PD(2)	WBL(2)	PD

1. The total number of cycles in the command sequence is determined by the number of bytes to be written to the write buffer. The maximum number of cycles is 30.
2. BA Block Address, WC Number of bytes to be programmed - 1, PA Program Address, PD Program Data, WBL Write Buffer Location (address must be within the same write buffer page as PA).

3.2 Program operation fails detection

In M29W128G devices, it is possible to detect program operation fails, even during a write to buffer or enhanced buffered program, when changing programmed data from '0' to '1', that is when reprogramming data in a portion of memory already programmed. The resulting data will be the logical OR between the previous value and the current value.

In S29GL128P devices, this functionality is not available.

3.3 Device codes and auto select codes

The auto select codes are composed of the manufacturer code, the device code, the block protection status, and the extended memory block verify code.

The S29GL128P and M29W128G devices have different manufacturer code, device code, and extended memory block verify code.

The S29GL128P and M29W128G devices use identical commands and address inputs to read the auto select codes. Two methods are available to access the auto select codes:

- In the first method, an Auto Select command is issued (see ***Table 2 Command set***) to place the device in auto select mode. The auto select codes can then be read by using a bus read operation with addresses and control signals set as shown in ***Table 8 Bus operations for accessing the auto select codes***.
- In the high voltage method, the same sequence of bus read operations as in the first method is issued, except that A9 is set at V_{ID}.

Table 8 Bus operations for accessing the auto select codes

Operation	E	G	W	Address inputs		Data inputs/outputs		
				x 8 mode	x 16 mode	x 8 mode		x 16 mode
				DQ15A-1, A0-A21	A0-A21	DQ14-DQ8	DQ7-DQ0	DQ15A-1, DQ14-DQ0
Read manufacturer code	V_{IL}	V_{IL}	V_{IH}	A0-A3 = V_{IL}, A6 = V_{IL}, A9 = V_{ID}, others V_{IL} or V_{IH}		Hi-Z	see *Table 9*	
Read device code				A0 = V_{IH}, A1-A3 = V_{IL}, A6 = V_{IL}, A9 = V_{ID}, others V_{IL} or V_{IH}				
Blockprotection status				A0,A2,A3, A6= V_{IL}, A1= V_{IH}, A9 = V_{ID}, A12-A21 = Block address, others V_{IL} or V_{IH}				
Extended memory block verify code				A0-A1 = V_{IH}, A2-A3 = V_{IL}, A6 = V_{IL}, A9 = V_{ID}, others V_{IL} or V_{IH}				

Table 9 Auto select codes

Auto select code	Spansion		Numonyx		Spansion		Numonyx	
	S29GL128P (01 model)[1]	S29GL128P (02 model)[2]	M29W128GH	M29W128GL	S29GL128P (01 model)[1]	S29GL128P (02 model)[2]	M29W128GH	M29W128GL
	x 16 mode				x 8 mode			
Manufacturer code	0001h		0020h	0020h	01h		20h	
Device code	227Eh 2221h 2201h		227Eh 2221h 2201h	227Eh 2221h 2200h	7Eh+21h+01h		7Eh+21h+01h	7Eh+21h+00h
Block protection status	01h (protected) 00h (unprotected)[3]		0001h (protected) 0000h (unprotected)		01h (protected) 00h (unprotected)			
Extended memory block verify indicator	XX99h (factory locked) XX19h (not factory locked)(3)	XX89h (factory locked) XX09h (not factory locked)(3)	0099h (factory locked) 0019h (not factory locked)	0089h (factory locked) 0009h (not factory locked)	99h (factory locked) 19h (not factory locked)[3]	89h (factory locked) 09h (not factory locked)[3]	99h (factory locked) 19h (not factory locked)	89h (factor y locked) 09h (not factory locked)

1. Highest block protected by driving V_{PP}/WP High.
2. Lowest block protected by driving V_{PP}/WP High.
3. DQ8 to DQ15 are 'don't care'.

3.4 0xFF Command Tolerance

M29W128G doesn't tolerate 0xFF (SW reset command for Intel flash) as a valid command, and once 0xFF is issued to the device, like in some system, the M29W128G will enter unexpected state. Adding a 0xF0 command systematically after 0xFF command is necessary.

S29GL128P device tolerates 0xFF command. Nothing will happen if it is issued 0xFF command.

3.5 Difference in CFI operation

When exiting CFI mode on M29W128G device, Read/Reset command (0xF0h) is used to return the device to the previous mode (Main Array Read or Auto Select Mode). ***Table 10 CFI exit sequence*** shows the detail exiting command sequence on M29W128G device.

Table 10 CFI exit sequence

Entering CFI Sequence	Exiting from CFI to main array read command sequence	
	S29GL128P	M29W128G
Main Array Read --> CFI	0xF0h	0xF0h
Main Array Read --> Auto Select Mode --> CFI	0xF0h	0xF0h --> 0xF0h (twice cmd)

S29GL128P will enter main array read mode when it is issued Read/Reset command (0xF0h).

In x8 mode, reading CFI data in odd address from M29W128G device is different from reading CFI data in odd address from S29GL128P device. Refer to ***Table 11 CFI x8 read difference comparison*** for details.

Table 11 CFI x8 read difference comparison

Address (x8)	S29GL128P Read-out	M29W128G Read-out	Description
20h	51h	51h	Query unique ASCII string ‘QRY’, "Q"
21h	51h	00h	Invalid due to x8 mode
22h	52h	52h	Query unique ASCII string ‘QRY’, "R"
23h	52h	00h	Invalid due to x8 mode
24h	59h	59h	Query unique ASCII string ‘QRY’, "Y"
25h	59h	00h	Invalid due to x8 mode
26h	02h	02h	Primary algorithm command set and control interface ID code 16 bit ID code defining a specific algorithm
27h	02h	00h	Invalid due to x8 mode
28h	00h	00h	Primary algorithm command set and control interface ID code 16 bit ID code defining a specific algorithm
29h	00h	00h	Invalid due to x8 mode
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
9Eh	xxh	xxh	Top/bottom boot block flag xx = 04 = M29W128GL. First block protected by V_{PP}/WP xx = 05 = M29W128GH. Last block protected by V_{PP}/WP
9Fh	xxh	00h	Invalid due to x8 mode
A0h	01h	01h	Program suspend, 00 = not supported, 01 = supported
A1h	01h	00h	Invalid due to x8 mode

4 Performance and characteristics

The S29GL128P and the M29W128G have almost compatible DC and AC characteristics (see the respective datasheets for details). The M29W128G memories offer better performance in terms of access, programming and erase times than the S29GL128N devices.

4.1 Access time

The M29W128G has a random access time of 70 ns or 90 ns, depending on the V_{CCQ} supply voltage, whereas the S29GL128P has an access time of 90 ns, 100 ns or 110 ns.

4.2 Page read mode

The page mode is available on the S29GL128P and M29W128G to speed up read operations. The data is internally read and stored in an 8-word (or 16-byte) page buffer.

Using page read, the access time for subsequent read operations is reduced to 25 ns for both devices with $V_{CCQ} = V_{CC}$, while it is reduced to 30 ns for the M29W128G with V_{CCQ} = 1.65 V.

4.3 Program and erase times

The time required to program or erase the whole memory is lower on the M29W128G compared to the S29GL128P. The memory can be either programmed using a Fast Program or an Enhanced Buffered Program command (see ***Section 3.1***), or using the word by word program command.

Refer to ***Section 3.1*** for details on fast program commands.

Table 12 M29W128G program and erase times

Parameter			Min	Typ(1)(2)	Max(2)	Unit
Chip Erase				40	400(3)	s
Block Erase (128 Kbytes)(4)				0.5		s
Erase Suspend latency time				5	50	µs
Block Erase time-out			50			µs
Byte Program	Single Byte Program			16	200(3)	µs
	Write to Buffer Program (64 bytes at-a-time)	$V_{PP}/WP = V_{PPH}$		51		µs
		$V_{PP}/WP = V_{IH}$		78		
Word Program	Single Word Program			16	200(3)	µs
	Write to Buffer Program (32 words at-a-time)	$V_{PP}/WP = V_{PPH}$		51		µs
		$V_{PP}/WP = V_{IH}$		78		
Chip Program (byte by byte)				270	800(3)	s
Chip Program (word by word)				135	400(3)	s
Chip Program (Write to Buffer Program with $V_{PP}/WP = V_{IH}$)(5)				20	200(3)	s
Chip Program (Write to Buffer Program with $V_{PP}/WP = V_{PPH}$)(5)				13	50(3)	s
Chip Program (Enhanced Buffered Program with $V_{PP}/WP = V_{IH}$)(5)				8	40	s
Chip Program (Enhanced Buffered Program with $V_{PP}/WP = V_{PPH}$)(5)				5	25	s
Program Suspend latency time				5	15	µs
Program/Erase cycles (per block)			100,000			cycles
Data retention			20			years

1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,000 program/erase cycles.
4. Block Erase Polling cycle time (see Figure 23: Data polling AC waveforms in the M29W128G datasheet).
5. Intrinsic program timing, that means without the time required to execute the bus cycles to load the program commands.

Table 13 Comparison between S29GL128P and M29W128G performance and characteristics

Parameter	S29GL128P	M29W128G
Access time	90, 100, 110 ns	60 ns, 70 and 80 ns with V_{CCQ} = 1.65 V
Page Read	25 ns (8-word page)	
Fast Program	Write to Buffer	Program
	-	Enhanced Buffered Program
Chip Program time	113 s (using the Write to Buffer Program)	20 s (V_{PP}/WP = V_{IH}) 13 s (V_{PP}/WP = V_{PPH}) (using the Write to Buffer Program)
		8 s (V_{PP}/WP = V_{IH}) 5 s (V_{PP}/WP = V_{PPH}) (using the Enhanced Buffered Program)
Supply voltage	2.7 to 3.6 V	2.7 to 3.6 V
Temperature range	–40 to 85 °C	
V_{CCQ} or V_{IO} input/output supply	1.65 V to V_{CC}	
Chip Erase time	64 s (typical), except all 0000h programmed prior to erasing	40 s (typical)

5 Block protection

The M29W128G memories, as the S29GL128P devices, feature three techniques to control block protection. The table below shows how the three techniques are called in the M29W128G and S29GL128P devices, respectively.

Table 14 Block protection techniques in M29W128G and S29GL128P Flashes

M29W128G(1)	S29GL128P
Hardware method (V_{PP}/WP)	Hardware Data Protection (WP/ACC)
Volatile/non-volatile protection	Advanced protection/unprotection
Password protection method	Password protection method

1. Please refer to the M29W128G datasheet for further details.

The S29GL128P and M29W128G both feature hardware protection. In particular in the M29W128G memories, when:

- V_{PP}/WP = V_{IL}, the highest or lowest blocks are protected
- V_{PP}/WP = V_{IH}, the highest or lowest blocks are unprotected.

Advanced protection/unprotection in S29GL128P corresponds to volatile/non-volatile protection in M29W128G:

- In the volatile protection mode, each block can be protected/unprotected with power-down or by a command
- In the non-volatile protection mode, each block can be protected/unprotected by a command. Power-down or hardware reset does not change the protection status.

The password protection method is available in both S29GL128P and M29W128G devices. It is a high level security protection mode that requires a 64-bit password to unlock the device. Program or erase operations are not allowed if the password is not correct. The password protection method is a non-volatile protection.

The S29GL128P and M29W128G devices feature the same commands with the same functions (see ***Table 15 Commands cross reference***), so protection commands are fully compatible.

Table 15 Commands cross reference

M29W128G	S29GL128P
Protection commands	Protection commands
Lock register	Lock register
Password protection	Password protection
Non-volatile protection	Global non-volatile
NVPB lock bit	Global volatile freeze (PPB Lock)
Volatile protection	Volatile
Exit protection command set	Command set exit

5.1 Temporary block unprotect

In the M29W128G, when held at V_{ID}, the RP or V_{PP}/WP pin temporarily unprotects all the blocks previously protected using a volatile/non-volatile protection with the NVPB lock bit not set.

To unprotect blocks with a temporary block unprotect mode and a password mode, it is necessary to provide the password and then put the RP or V_{PP}/WP pin at V_{ID}.

In the M29W128G, this functionality is only available upon customer request, while it is not available at all in S29GL128P devices.

6 Power-up waiting timing

The time needed to power up the M29W128G devices is different from the one needed by S29GL128P devices. In particular, M29W128G needs 500 µs to accept commands (program, erase, read CFI, etc.) and 50 µs to read content in memory cells after power-up.

The power-up waiting timing differences are shown in ***Table 16 Power-up waiting timings***.

Table 16 Power-up waiting timings

Waiting timing	M29W128G		S29GL128P		Unit
Time to accept commands after power-up	Min	500	Min	35	µs
Time to read memory cells after power-up	Min	50	Min	35	µs

Please refer to the M29W128G and S29GL128P datasheets for further details.

7 Conclusion

Applications can be easily migrated from an S29GL128P to an M29W128G Flash memory. In addition, the M29W128G features better performance with respect to the S29GL128P devices.

8 Revision history

Table 17 Document revision history

Date	Version	Changes
13-Feb-2008	1	Initial release.
19-Mar-2008	2	Applied Numonyx branding.
26-Jun-2008	3	Corrected S29GL128P supply voltage from 3.0 to 2.7 in ***Table 13 Comparison between S29GL128P and M29W128G performance and characteristics*** on page 18.
01-Aug-2008	4	Add up three incompatibilities.

Please Read Carefully: