Technical Note

Designing for 1Gb DDR SDRAM

Introduction

The 1Gb device incorporates the same footprint as lower-density DDR components, promoting an easy migration path as well as a cost-effective solution. This technical note provides system designers with essential information relevant to utilizing the 1Gb double data rate (DDR) synchronous dynamic random access memory (SDRAM). The significant changes with the 1Gb SDRAM that are discussed in this technical note are:

- Pin 17 changes from a no connect (NC) to an address pin, A13.
- Increased AUTO REFRESH command period time (^{t}RFC).
- Method to calculate average periodic refresh interval time (^{t}REFI).

1Gb Architecture

As with earlier DDR devices, the 1Gb component comprises the same basic architecture. It is available in a 256 Meg x 4, 128 Meg x 8, or 64 Meg x 16 configuration. To increase the array size, the 1Gb has one additional row address, making the array 16,384 rows deep (using addresses A0 through A13). The column addressing remains the same as the 512Mb device (4096 column addresses for the 256 Meg x 4, 2048 column addresses for the 128 Meg x 8, and 1024 column addresses for the 64 Meg x 16). For the standard 66-pin TSOP package, the additional row address (A13) is located at pin 17, shown in Figure 1 on page 2. Pin 17 is considered a no connect (NC) pin for all lower densities.

DRAM Refresh

To refresh all DRAM cells within the allotted refresh period, an AUTO REFRESH command must be issued at the average periodic refresh interval time (^{t}REFI). To increase the density of the DRAM, either an additional row or column address is added. Traditionally, if a row address is added, the ^{t}REFI time will decrease, and refreshes are required more frequently.

Conventional Calculation of ^{t}REFI Values

Formula to determine ^{t}REFI:

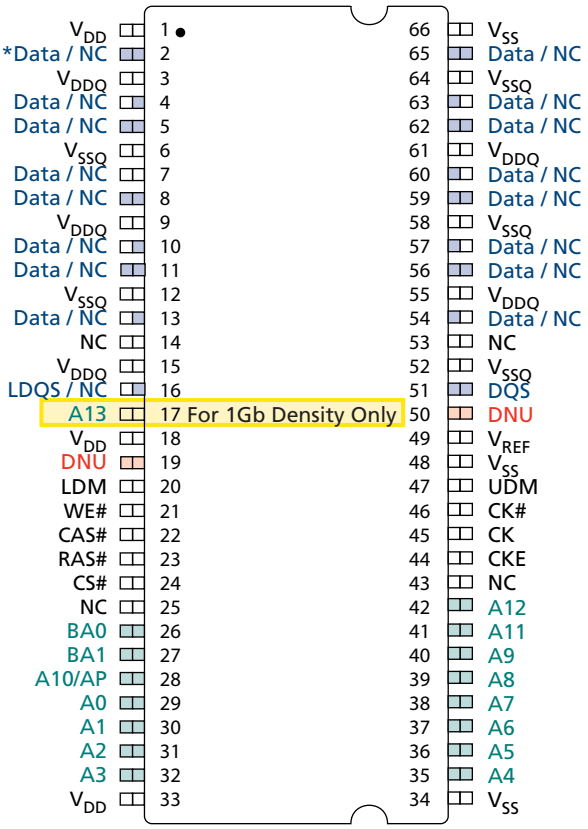
^{t}REFI = Static Refresh ÷ Number of Row Addresses

Static Refresh = 64ms

Examples:

- 128Mb has 4096 row addresses
- 256Mb has 8192 row addresses
  ^{t}REFI (128Mb)= 64ms ÷ 4096
  = 15.63µs
  ^{t}REFI (256Mb)= 64ms ÷ 8192
  = 7.81µs

Figure 1: 66-Pin TSOP Identifying Placement of A13



* Data for x16 configuration, may be NC for x4 or x8 DRAM

During the refresh cycle, the DRAM controls all row addressing and keeps track of which rows have or have not been refreshed. The memory controller needs to guarantee only the appropriate number of refresh commands for the particular device. Normally, for each AUTO REFRESH command, the DRAM will refresh one full row, then increment the internal refresh counter by one. The amount of time it takes the DRAM to perform the refresh cycle is called the AUTO REFRESH command period (^{t}RFC).

1Gb Refresh Times

In theory, using the conventional method to calculate ^{t}REFI, the 1Gb DDR SDRAM would have an average refresh interval that would be equal to 3.9µs because it has 14 address rows, but this is not the case. The refresh interval has been kept at 7.8µs. This is accomplished by refreshing two internal rows for each single AUTO REFRESH command. During the refresh cycle, the SDRAM still controls all of the row addressing and keeps track of each row that has been refreshed. Due to the dual refresh cycle, the ^{t}REFI time for the 1GB DDR SDRAM has increased, but the average internal periodic refresh remains constant. See Table 1 for a comparison of refresh times as related to density.

Formula to determine ^{t}REFI for 1Gb DDR SDRAM only

^{t}REFI = (Static Refresh ÷ Number of Row Addresses)÷ 2

Example:

^{t}REFI (1Gb) = (64ms ÷ 16,368) ÷ 2
= 7.81µs

Table 1: Refresh Parameters for DDR266 Devices

Device Size	Number of Row Addresses	^{t}RFC[1]	^{t}REFI	^{t}REFC
128Mb	4096	75ns	15.63µs	140.63µs
256Mb	8192	75ns	7.81µs	70.31µs
512Mb	8192	75ns	7.81µs	70.31µs
1Gb	16,384	120ns	7.81µs	70.31µs
128Mb	4096	75ns	15.63µs	140.63µs

Notes: 1. Will vary by speed grade

High-Density Modules

When designing for high-density modules built with the 1Gb component, an additional row address needs to be included. For the JEDEC-defined 184-pin DIMM, pin 167 has been reserved for A13. For the 200-pin SODIMM, pin 123 has been reserved for A13.

The module serial presence-detect (SPD) also has three key bytes identifying the number of row addresses, the number of column addresses, and the value of ^{t}RFC. Byte 3 identifies the number of row addresses by module bank; the lower four bits specify the number of row addresses for bank one; and the higher four bits specify the number of row addresses for bank two (if bank two addressing is different than bank one). Byte 4 identifies the number of column addresses by module bank. Again, the lower four bits specify the number of column addresses for bank one, and the higher four bits specify the number of column addresses for bank two (if bank two addressing is different from bank one addressing). Byte 42 identifies the AUTO REFRESH cycle time, ^{t}RFC. All values are in hexadecimal, and complete explanations are provided in the SPD document on Micron's Web site at http://download.micron.com/pdf/toolbox/4_01_2_4R11a.pdf.

Figure 2: Key SPD Bytes and an Example for a Module Using 128 Meg x 4 DDR SDRAM

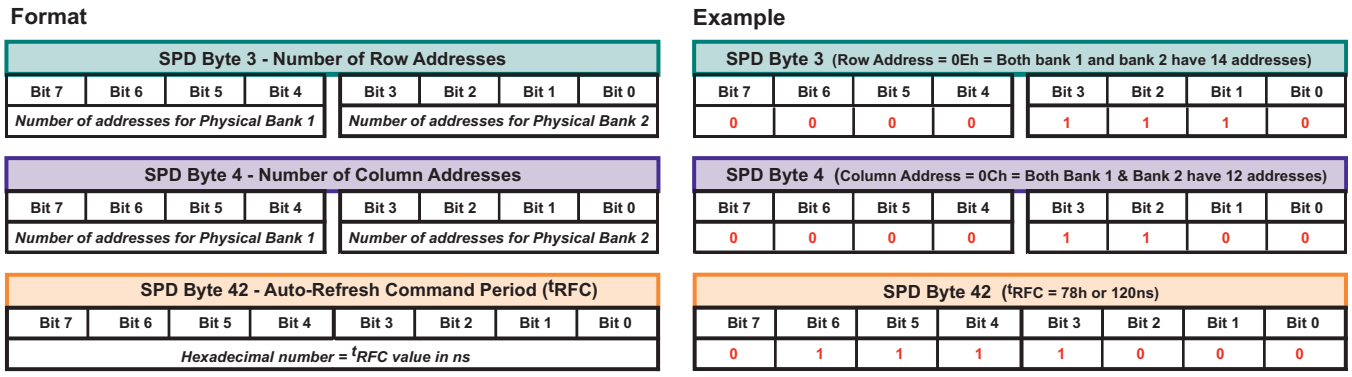


Table 2: Serial Presence-Detect Matrix[1]

1/0: Serial Data, driven to HIGH/driven to LOW

Byte	Description	Entry (Version)	MT36VDDT12872	MT36VDDT25672	MT36VDDT51272
0	Number of bytes used by Micron	128	80	80	80
1	Total number of SPD memory bytes	256	08	08	08
2	Memory type	SDRAM DDR	07	07	07
3	Number of row addresses	13, 14	0D	0D	0E
4	Number of column addresses	11 or 12	0B	0C	0C
5	Number of module ranks	2	02	02	02
...	...	...	...	...	...
42	Minimum auto refresh to active/ auto refresh command period, tRFC	75ns (-262/-26A/-265) 80ns (-202) 120ns (512MB, all speeds)	4B 50 –	4B 50 –	– – 78
...	...	...	...	...	...

Notes: 1. Excerpted SPD Table from a 4GB DDR Registered DIMM data sheet.

Summary

There is an easy migration path for the 1Gb DDR SDRAM if the following key items are understood.

1. The 1Gb has an additional row address. For the 66-pin TSOP, pin 43 is A13. For the 184-pin DIMM, pin 167 is reserved for A13; for the 200-pin SODIMM, pin 123 is utilized for A13.
2. Module SPD bytes 3 and 4 identify the number of row and column addresses, respectively, by module bank.
3. For 1Gb devices, the AUTO REFRESH command period (^{t}RFC) has increased; see Micron's 1Gb data sheet for exact values.
4. 1Gb-based modules also have an increased ^{t}RFC value. SPD byte 42 identifies the exact value for each module.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992

Revision History

Rev. B 11/09

- Updated format.

Rev. A 12/03

- Initial release.