

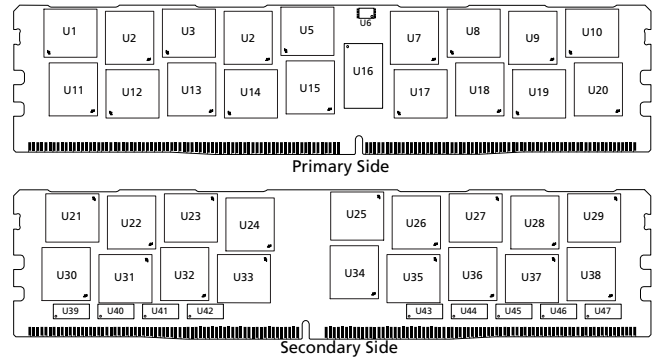
DDR4 SDRAM LRDIMM Addendum

MTA36ASF8G72LZ – 64GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 LRDIMM core data sheet
- 288-pin, command/address/control registered, data buffered dual in-line, load reduced memory module (LRDIMM)
- Fast data transfer rates: PC4-3200, PC4-2933
- 64GB (4 Gig x 72)
- Dual-rank
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 288-Pin LRDIMM (MO-309, R/C-B2)



Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$)
- Package
 - 288-pin DIMM (Green)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)
 - 0.682ns @ CL = 21 (DDR4-2933)

Marking

None
Z
-3G2
-2G9

Table 1: Addressing

Parameter	64GB
Row address	256K A[17:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (4 Gig x 4), 16 banks
Module rank address	2 CS_n[1:0]



Table 2: Part Numbers and Timing Parameters – 64GB Modules

Base device: MT40A4G4,¹ 16Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ⁿ RCD- ⁿ RP)
MTA36ASF8G72LZ-3G2__	64GB	8 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA36ASF8G72LZ-2G9__	64GB	8 Gig x 72	23.47 GB/s	0.682ns/2933 MT/s	21-21-21

- Notes:
1. The data sheet for the base device can be found on micron.com.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA36ASF8G72LZ-3G2B1.

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DQ Map

Table 3: Component-to-Module DQ Map, Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	0	5	U2	0	10	23
	1	2	12		1	8	16
	2	1	150		2	11	168
	3	3	157		3	9	161
U3	0	22	32	U4	0	31	188
	1	21	170		1	29	181
	2	23	177		2	30	43
	3	20	25		3	28	36
U5	0	CB6	54	U7	0	34	104
	1	CB5	192		1	32	97
	2	CB7	199		2	35	249
	3	CB4	47		3	33	242
U8	0	40	108	U9	0	50	126
	1	42	115		1	48	119
	2	41	253		2	51	271
	3	43	260		3	49	264
U10	0	60	128	U11	0	7	155
	1	62	135		1	5	148
	2	61	273		2	6	10
	3	63	280		3	4	3
U12	0	14	21	U13	0	17	172
	1	12	14		1	19	179
	2	15	166		2	16	27
	3	13	159		3	18	34
U14	0	25	183	U15	0	CB0	49
	1	27	190		1	CB3	201
	2	24	38		2	CB1	194
	3	26	45		3	CB2	56
U17	0	38	102	U18	0	46	113
	1	36	95		1	44	106
	2	39	247		2	47	258
	3	37	240		3	45	251
U19	0	52	117	U20	0	58	137
	1	54	124		1	57	275
	2	53	262		2	59	282
	3	55	269		3	56	130



Table 4: Component-to-Module DQ Map, Back

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U21	0	62	135	U22	0	48	119
	1	60	128		1	50	126
	2	63	280		2	49	264
	3	61	273		3	51	271
U23	0	42	115	U24	0	32	97
	1	40	108		1	34	104
	2	43	260		2	33	242
	3	41	253		3	35	249
U25	0	CB5	192	U26	0	29	181
	1	CB6	54		1	31	188
	2	CB4	47		2	28	36
	3	CB7	199		3	30	43
U27	0	21	170	U28	0	8	16
	1	22	32		1	10	23
	2	20	25		2	9	161
	3	23	177		3	11	168
U29	0	2	12	U30	0	57	275
	1	0	5		1	58	137
	2	3	157		2	56	130
	3	1	150		3	59	282
U31	0	54	124	U32	0	44	106
	1	52	117		1	46	113
	2	55	269		2	45	251
	3	53	262		3	47	258
U33	0	36	95	U34	0	CB3	201
	1	38	102		1	CB0	49
	2	37	240		2	CB2	56
	3	39	247		3	CB1	194
U35	0	27	190	U36	0	19	179
	1	25	183		1	17	172
	2	26	45		2	18	34
	3	24	38		3	16	27
U37	0	12	14	U38	0	5	148
	1	14	21		1	7	155
	2	13	159		2	4	3
	3	15	166		3	6	10

I_{DD} Specifications

Table 5: DDR4 I_{DD} Specifications and Conditions – 64GB (Die Revision B)

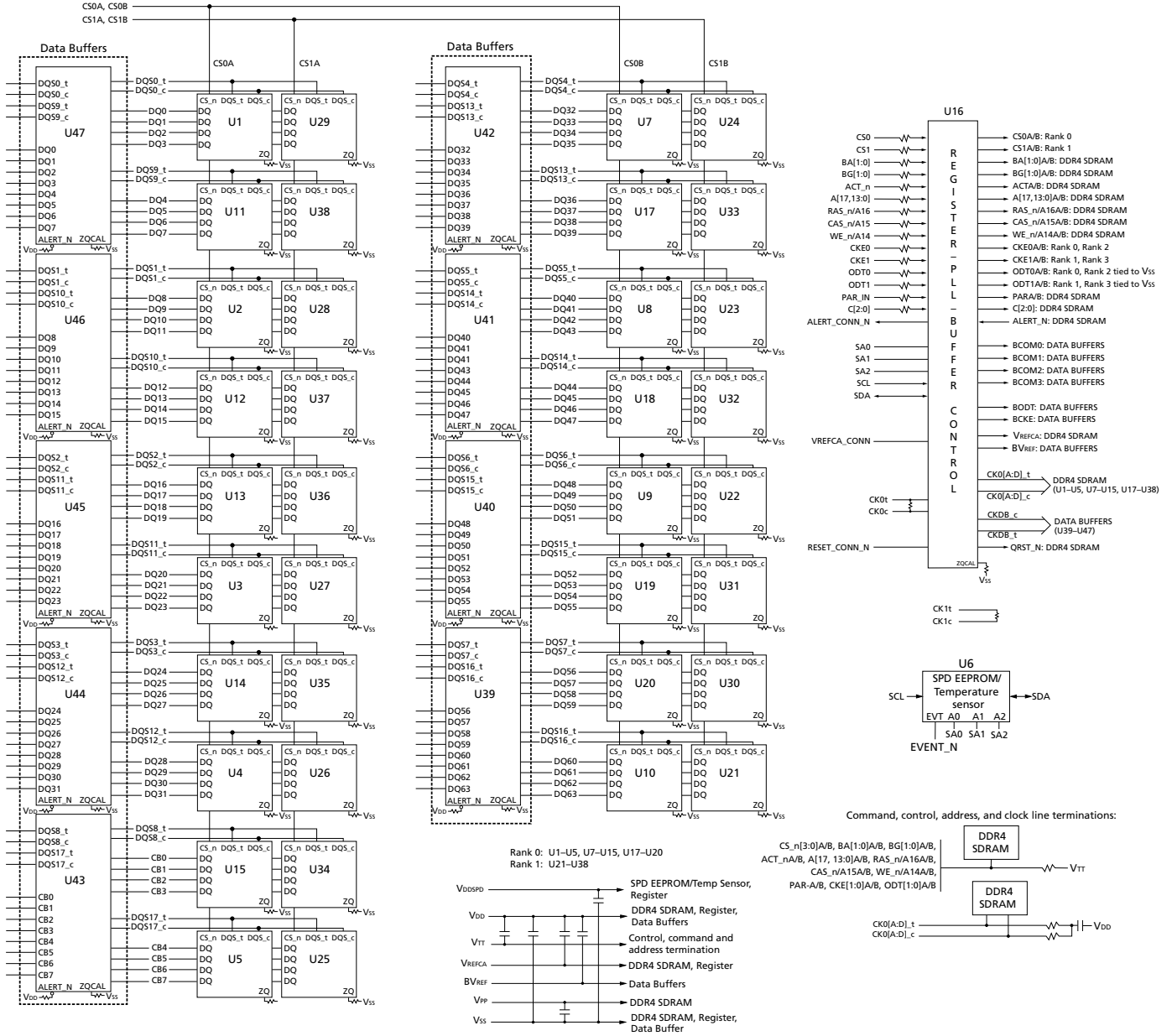
Values are for the MT40A4G4 DDR4 SDRAM only and are computed from values specified in the DDR4 (4 Gig x 4) component data sheet

Parameter	Symbol	3200	2933	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	1854	1836	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I _{pp} current	I _{PP0}	126	126	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	2034	2016	mA
Precharge standby current	I _{DD2N}	1872	1836	mA
Precharge standby ODT current	I _{DD2NT}	1782	1764	mA
Precharge power-down current	I _{DD2P}	1548	1548	mA
Precharge quiet standby current	I _{DD2Q}	1692	1692	mA
Active standby current	I _{DD3N}	2808	2772	mA
Active standby I _{pp} current	I _{PP3N}	108	108	mA
Active power-down current	I _{DD3P}	2484	2448	mA
Burst read current	I _{DD4R}	3870	3726	mA
Burst write current	I _{DD4W}	3726	3600	mA
Different logic rank burst refresh current (1x REF)	I _{DD5R}	2196	2178	mA
Different logic rank burst refresh I _{pp} current (1x REF)	I _{PP5R}	144	144	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N (0–85°C)}	2412	2412	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E (0–95°C)}	4356	4356	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R (0–45°C)}	1044	1044	mA
Auto self refresh current (25°C)	I _{DD6A (25°C)}	360	360	mA
Auto self refresh current (45°C)	I _{DD6A (45°C)}	1044	1044	mA
Auto self refresh current (75°C)	I _{DD6A (75°C)}	2196	2196	mA
Auto self refresh current (95°C)	I _{DD6A (95°C)}	4356	4356	mA
Auto self refresh I _{pp} current (0°C to 95°C)	I _{PP6X}	396	396	mA
Bank interleave read current	I _{DD7}	5058	4932	mA
Bank interleave read I _{pp} current	I _{PP7}	252	252	mA
Maximum power-down current	I _{DD8}	1440	1440	mA

Note: 1. For all I_{DD} values, one package rank in active I_{DD} condition, all other package ranks in I_{DD2P} or I_{PP3N}.

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



64GB (x72, ECC, DR) 288-Pin DDR4 LRDIMM Functional Block Diagram

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Although considered final, these specifications are subject to change, as further product development and data characterization some-
times occur.