DATA SHEET

16Gb DDR3 Mobile RAM™ PoP (14.0mm × 14.0mm, 220-ball FBGA)

EDFA164A1PF

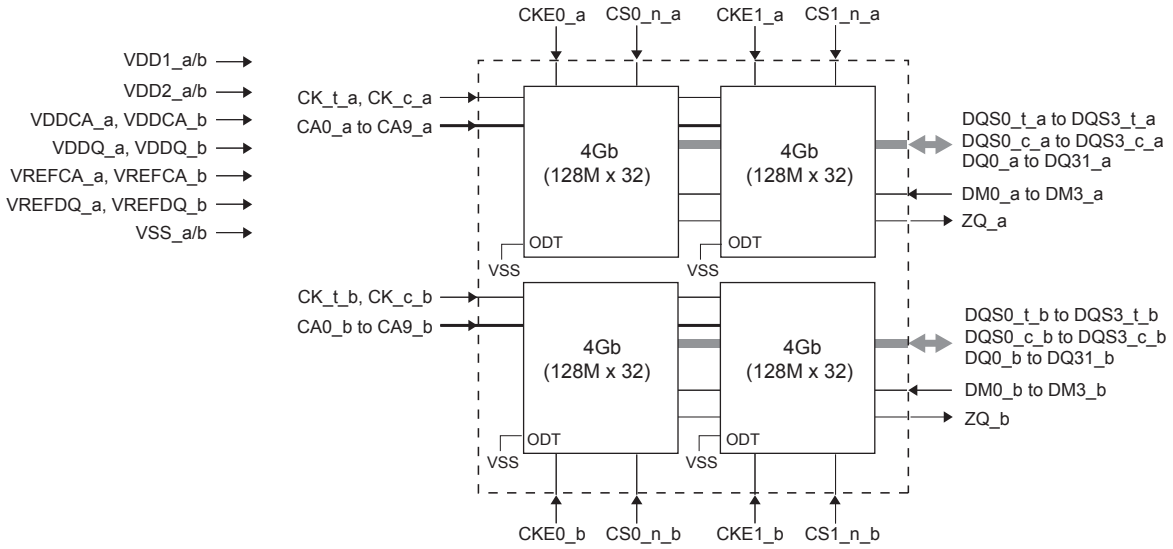
Specifications

- Density: 16Gb
- Organization
  - 4 pieces of 4Gb (16M words × 32 bits × 8 banks) in one package
  - Independent 2-channel bus
- Package
  - 220-ball FBGA
  - Package size: 14.0mm (X) × 14.0mm (Y)
  - Ball pitch: 0.50mm
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply
  - VDD1 = 1.70V to 1.95V
  - VDD2, VDDCA, VDDQ = 1.14V to 1.30V
- Data rate: 1600Mbps max (RL = 12)
- Interface: HSUL_12
- Operating case temperature range
  - TC = –30°C to +85°C

Features

- Low power consumption
- Per Bank Refresh
- Partial Array Self-Refresh (PASR)
  - Bank Masking
  - Segment Masking
- Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
- Deep power-down mode
- CA training for CA input timing adjustment
- Write leveling for clock to DQ, DQS_t, DQS_c and DM timing adjustment
- Suitable for Package on Package (PoP)

Block Diagram



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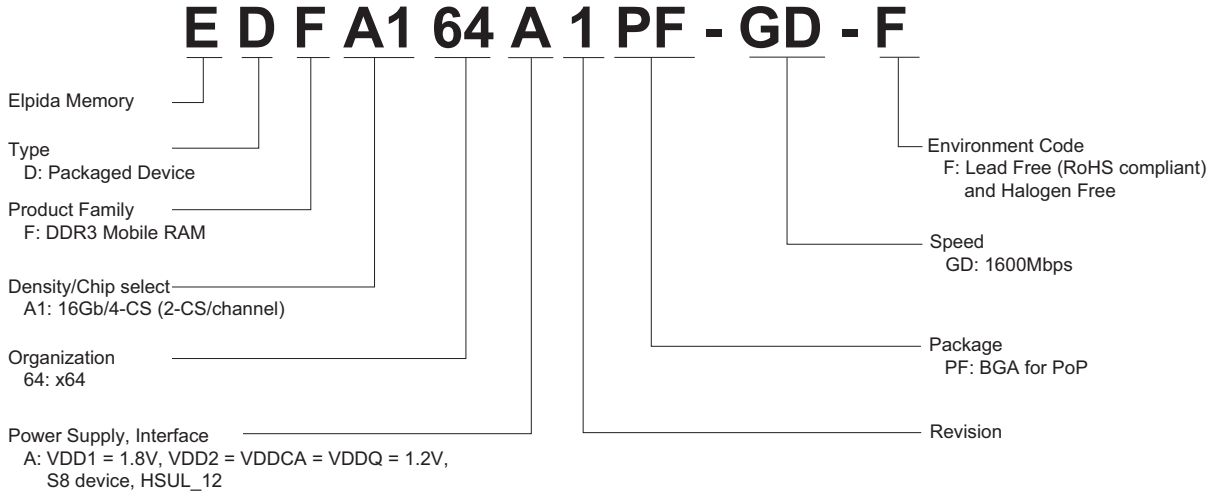
Ordering Information

Part number	Organization (words × bits)	Clock frequency	Data rate	Read latency	Package
EDFA164A1PF-GD-F	256M × 64 (128M × 32 × 4pcs)	800MHz	1600Mbps	12	220-ball FBGA

Part Number



Detailed Information

For detailed electrical specification and further information, please refer to the DDR3 Mobile RAM General Functionality and Electrical Condition data sheet (E1853E).

CONTENTS

Pin Configurations

220-ball FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
A	NC	VSS_a/b	VDD2_a/b	VSS_a/b	DQ29_b	DQ28_b	VSS_a/b	DQ25_b	DQ24_b	DQS3_c_b	DM3_b	DQ15_b	VSS_a/b	DQ13_b	DQ11_b	VSS_a/b	DQ9_b	DQS1_c_b	DM1_b	VSS_a/b	VSS_a/b	VDD2_a/b	DQS0_c_b	DQ7_b	VSS_a/b	VSS_a/b	NC
B	VDD1_a/b	NC	VDDQ_b	DQ31_b	DQ30_b	VDDQ_b	DQ27_b	DQ26_b	VDDQ_b	DQS3_t_b	VSS_a/b	VDDQ_b	DQ14_b	DQ12_b	VDDQ_b	DQ10_b	DQ8_b	DQS1_t_b	VDDQ_b	VREFDQ_b	VDD1_a/b	DM0_b	DQS0_t_b	VDDQ_b	DQ6_b	NC	VDD2_a/b
C	DQ16_a	DQ17_a																								DQ5_b	DQ4_b
D	DQ18_a	VDDQ_a																								VDDQ_b	DQ3_b
E	VSS_a/b	DQ20_a	DQ19_a																						DQ2_b	DQ1_b	VSS_a/b
F	DQ21_a	VDDQ_a																								VDDQ_b	DQ0_b
G	VSS_a/b	DQ22_a	DQ23_a																						DM2_b	DQS2_t_b	VSS_a/b
H	DQS2_t_a	DQS2_c_a																								DQS2_c_b	DQ23_b
J	VSS_a/b	DM2_a	DQ0_a																						DQ21_b	DQ22_b	VSS_a/b
K	DQ1_a	VDDQ_a																								VDDQ_b	DQ20_b
L	VSS_a/b	DQ2_a	DQ3_a																						DQ19_b	DQ18_b	VSS_a/b
M	DQ4_a	VDDQ_a																								VDD2_a/b	DQ17_b
N	VSS_a/b	DQ5_a	DQ6_a																						DQ16_b	VDDQ_b	VSS_a/b
P	DQ7_a	VDDQ_a																								VDDCA_a	CA0_a
R	VSS_a/b	DQS0_c_a	DQS0_t_a																						CA1_a	CA2_a	VSS_a/b
T	DM0_a	VDDQ_a																								CA3_a	CA4_a
U	VSS_a/b	VSS_a/b	VREFDQ_a																						CS0_n_a	CS1_n_a	VSS_a/b
V	VDD2_a/b	VDD1_a/b																								CKE0_a	CKE1_a
W	VSS_a/b	VDD2_a/b	DM1_a																						CK_c_a	CK_t_a	VSS_a/b
Y	DQS1_c_a	DQS1_t_a																								VDDCA_a	CA5_a
AA	VSS_a/b	DQ9_a	DQ10_a																						VREFCA_a	CA6_a	VDD2_a/b
AB	DQ8_a	VDDQ_a																								CA7_a	VSS_a/b
AC	VSS_a/b	DQ11_a	DQ12_a																						CA8_a	CA9_a	VSS_a/b
AD	DQ13_a	DQ14_a																								VDDCA_a	VDD2_a/b
AE	VSS_a/b	DQ15_a																								VDD1_a/b	ZQ_a
AF	VSS_a/b	VDDQ_a	DM3_a	DQS3_t_a	DQS3_c_a	DQ25_a	DQ27_a	VDDQ_a	DQ29_a	DQ31_a	VDD2_a/b	VDD1_a/b	VDDCA_b	CA9_b	CA7_b	VDD2_a/b	VREFCA_b	VDDCA_b	CK_t_b	CKE1_b	CS0_n_b	CA4_b	VDDCA_b	CA2_b	CA0_b	VDD2_a/b	VSS_a/b
AG	NC	VDD2_a/b	VSS_a/b	VDDQ_a	DQ24_a	DQ26_a	VSS_a/b	DQ28_a	DQ30_a	VSS_a/b	VSS_a/b	ZQ_b	VSS_a/b	CA8_b	CA6_b	CA5_b	VSS_a/b	VSS_a/b	CK_c_b	CKE0_b	CS1_n_b	VSS_a/b	CA3_b	CA1_b	VSS_a/b	VDD1_a/b	NC

(Top view)

Pin Descriptions

[DDR3 Mobile RAM_a channel]

Pin name	Function
CK_t_a, CK_c_a	Clock
CKE0_a, CKE1_a	Clock enable
CS0_n_a, CS1_n_a	Chip select
CA0_a to CA9_a	DDR command/address inputs (Address configurations: Row:R0-R13, Column:C0-C9, Bank:BA0-BA2)
DM0_a to DM3_a	Input data mask
DQ0_a to DQ31_a	Data input/output
DQS0_t _a to DQS3_t_a, DQS0_c_a to DQS3_c_a	Data strobe
VDDCA_a *3	Input receiver power supply
VDDQ_a *4	I/O power supply
VREFCA_a	Reference voltage for CA input receiver
VREFDQ_a	Reference voltage for DQ input receiver
ZQ_a	Reference pin for output drive strength calibration

[DDR3 Mobile RAM_b channel]

Pin name	Function
CK_t_b, CK_c_b	Clock
CKE0_b, CKE1_b	Clock enable
CS0_n_b, CS1_n_b	Chip select
CA0_b to CA9_b	DDR command/address inputs (Address configurations: Row:R0-R13, Column:C0-C9, Bank:BA0-BA2)
DM0_b to DM3_b	Input data mask
DQ0_b to DQ31_b	Data input/output
DQS0_t _b to DQS3_t_b, DQS0_c_b to DQS3_c_b	Data strobe
VDDCA_b *3	Input receiver power supply
VDDQ_b *4	I/O power supply
VREFCA_b	Reference voltage for CA input receiver
VREFDQ_b	Reference voltage for DQ input receiver
ZQ_b	Reference pin for output drive strength calibration

[Common]

Pin name	Function
VDD1_a/b	Core power supply 1
VDD2_a/b	Core power supply 2
VSS_a/b	Ground
NC*1	No connection

Notes: 1. Not internally connected.
2. ODT pins are not listed above since they are internally connected to VSS. ODT function is disabled accordingly.
3. VDDCA_a and VDDCA_b are merged on the package substrate.
4. VDDQ_a and VDDQ_b are merged on the package substrate.

Pin Capacitance

Parameter	Symbol	Pins	min	max	Unit	Note
Input capacitance	CCK	CK_t_a, CK_c_a, CK_t_b, CK_c_b	1.5	3.6	pF	1, 2
	CI1	All other DDR3 Mobile RAM input only pins except CS_n, CKE	1.5	3.6	pF	1, 2
	CI2	CS_n, CKE	0.5	3.0	pF	1, 2
Data input/output capacitance	CIO	DQ_a, DQ_b, DM_a, DM_b, DQS_t_a, DQS_c_a, DQS_t_b, DQS_c_b	2.5	5.5	pF	1, 2, 3
	CZQ	ZQ_a, ZQ_b	0.0	6.0	pF	1, 2, 3

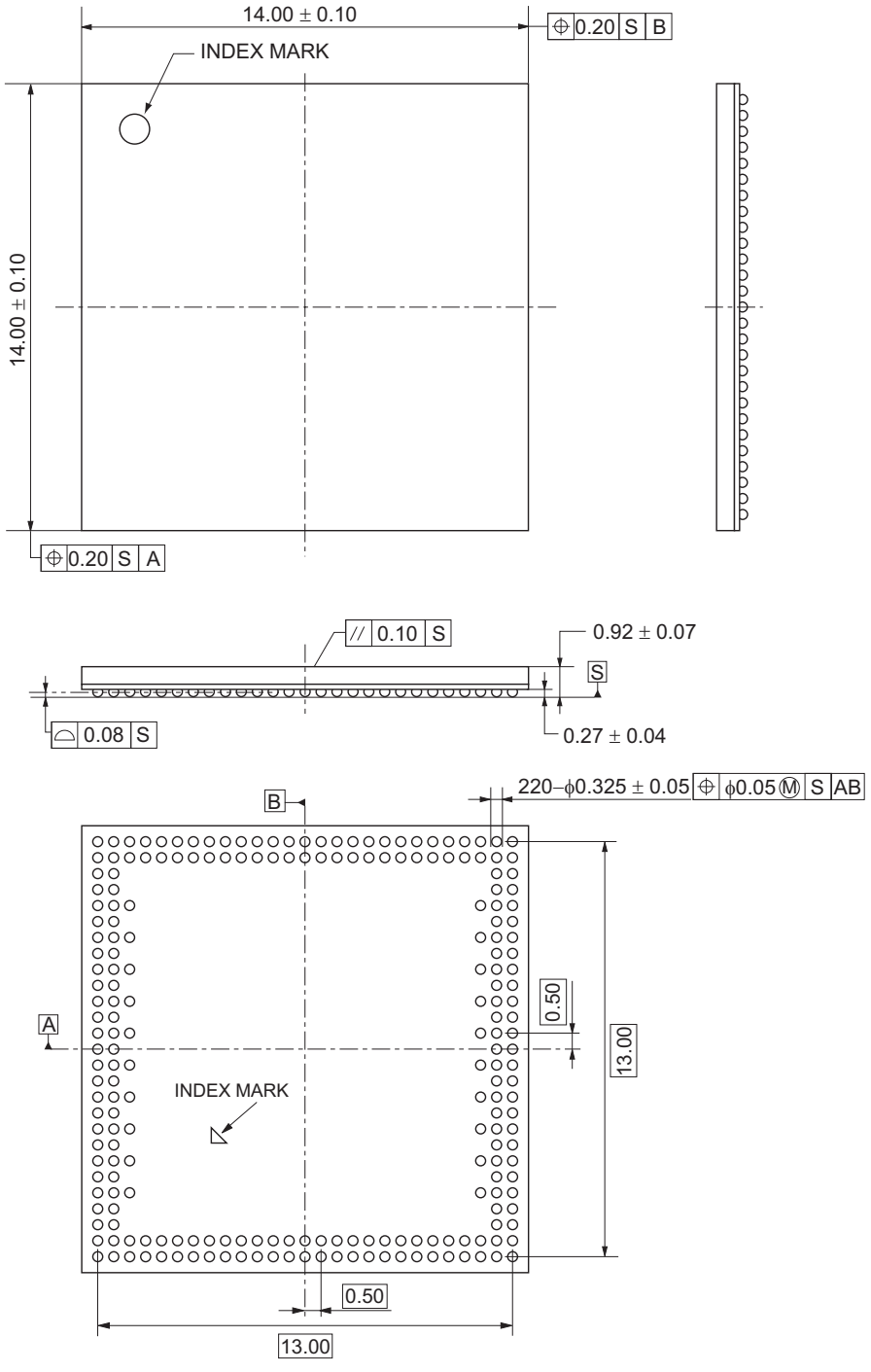
Notes: 1. This parameter is not subject to production test. It is verified by design and characterization.
2. These parameters are measured on f = 100MHz, VOUT = VDDQ/2, TA = +25°C.
3. DOUT circuits are disabled.

Package Drawing

220-ball FBGA

Solder ball: Lead free

Unit: mm



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1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.
- Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR3 Mobile RAM Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

1.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	min	max	Unit	Note
VDD1 supply voltage relative to VSS	VDD1	–0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	–0.4	1.6	V	2
VDDCA supply voltage relative to VSS	VDDCA	–0.4	1.6	V	2, 3
VDDQ supply voltage relative to VSS	VDDQ	–0.4	1.6	V	2, 4
Voltage on any ball relative to VSS	VIN, VOUT	–0.4	1.6	V	
Storage Temperature	TSTG	–55	125	°C	5

Notes: 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. See Power-Ramp section “Power-up, initialization and Power-Off” in the ”DDR3 Mobile RAM General Functionality and Electrical Condition” specification for relationship between power supplies.
3. VREFCA ≤ 0.6 × VDDCA; however, VREFCA may be ≥ VDDCA provided that VREFCA ≤ 300mV.
4. VREFDQ ≤ 0.7 × VDDQ; however, VREFDQ may be ≥ VDDQ provided that VREFDQ ≤ 300mV.
5. Storage Temperature is the case surface temperature on the center/top side of the DDR3 Mobile RAM Device. For the measurement conditions, please refer to JESD51-2 standard.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

1.2 Recommended DC Operating Conditions

Table 2: Recommended DC Operating Conditions (TC= –30°C to +85°C)

Parameter	Symbol	min	typ	max	Unit
Core Power1	VDD1	1.70	1.80	1.95	V
Core Power2	VDD2	1.14	1.20	1.30	V
Input Buffer Power	VDDCA	1.14	1.20	1.30	V
I/O Buffer Power	VDDQ	1.14	1.20	1.30	V

2. Electrical Specifications

2.1 DC Characteristics 1

Table 3: IDD Specification Parameters and Operating Conditions
(TC = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V)

Symbol	Power Supply	1600 max	1333 max	Unit	Parameter/Condition	Note
IDD0_1	VDD1	9.2	9.2	mA	**Operating one bank active-precharge**	
IDD0_2	VDD2	63	63	mA	**Conditions for operating devices are**	
IDD0_IN	VDDCA VDDQ	3.3	3.3	mA	tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	1, 2, 3
IDD2P_1	VDD1	1.6	1.6	mA	**Idle power-down standby current**	
IDD2P_2	VDD2	3.6	3.6	mA	tCK = tCK(avg)min; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	1, 2
IDD2P_IN	VDDCA VDDQ	0.4	0.4	mA		
IDD2PS_1	VDD1	1.6	1.6	mA	**Idle power-down standby current with clock stop**	
IDD2PS_2	VDD2	3.6	3.6	mA	CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE	1, 2
IDD2PS_IN	VDDCA VDDQ	0.4	0.4	mA		
IDD2N_1	VDD1	1.6	1.6	mA	**Idle non power-down standby current**	
IDD2N_2	VDD2	15.7	13.7	mA	tCK = tCK(avg)min; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	1, 2, 3
IDD2N_IN	VDDCA VDDQ	3.3	3.3	mA		
IDD2NS_1	VDD1	1.6	1.6	mA	**Idle non power-down standby current with clock stop**	
IDD2NS_2	VDD2	6.7	6.7	mA	CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE	1, 2, 3
IDD2NS_IN	VDDCA VDDQ	3.3	3.3	mA		
IDD3P_1	VDD1	1.9	1.9	mA	**Active power-down standby current**	
IDD3P_2	VDD2	8.2	8.2	mA	tCK = tCK(avg)min; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	1, 2, 3
IDD3P_IN	VDDCA VDDQ	0.4	0.4	mA		
IDD3PS_1	VDD1	1.9	1.9	mA	**Active power-down standby current with clock stop**	
IDD3PS_2	VDD2	8.2	8.2	mA	CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	1, 2, 3
IDD3PS_IN	VDDCA VDDQ	0.4	0.4	mA		
IDD3N_1	VDD1	2.2	2.2	mA	**Active non power-down standby current**	
IDD3N_2	VDD2	19.7	17.7	mA	tCK = tCK(avg)min; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	1, 2, 3
IDD3N_IN	VDDCA VDDQ	3.3	3.3	mA		
IDD3NS_1	VDD1	2.2	2.2	mA	**Active non power-down standby current with clock stop**	
IDD3NS_2	VDD2	10.7	10.7	mA	CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	1, 2, 3
IDD3NS_IN	VDDCA VDDQ	3.3	3.3	mA		

Table 3: IDD Specification Parameters and Operating Conditions
(TC = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V) (cont'd)

Symbol	Power Supply	1600 max	1333 max	Unit	Parameter/Condition	Note
IDD4R_1	VDD1	4.0	4.0	mA	**Operating burst read**	1, 2, 3
IDD4R_2	VDD2	235	205	mA	**Conditions for operating devices are**	
IDD4R_IN	VDDCA	3.3	3.3	mA	tCK = tCK(avg)min; CS_n is HIGH between valid commands; One bank active; BL = 8; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	
IDD4W_1	VDD1	4.0	4.0	mA	**Operating burst write**	1, 2, 3
IDD4W_2	VDD2	245	215	mA	**Conditions for operating devices are**	
IDD4W_IN	VDDCA VDDQ	3.3	3.3	mA	tCK = tCK(avg)min; CS_n is HIGH between valid commands; One bank active; BL = 8; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	
IDD5_1	VDD1	29.2	29.2	mA	**All bank auto-refresh**	1, 2, 3
IDD5_2	VDD2	152.7	152.7	mA	**Conditions for operating devices are**	
IDD5_IN	VDDCA VDDQ	3.3	3.3	mA	tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE	
IDD5AB_1	VDD1	3.2	3.2	mA	**All bank auto-refresh**	1, 2, 3
IDD5AB_2	VDD2	20.7	18.7	mA	tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE	
IDD5AB_IN	VDDCA VDDQ	3.3	3.3	mA		
IDD5PB_1	VDD1	3.2	3.2	mA	**Per bank auto-refresh**	1, 2, 3
IDD5PB_2	VDD2	20.7	18.7	mA	tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tREFIpb; CA bus inputs are SWITCHING; Data bus inputs are STABLE	
IDD5PB_IN	VDDCA VDDQ	3.3	3.3	mA		
IDD8_1	VDD1	64	64	µA	**Deep power-down**	1, 2
IDD8_2	VDD2	24	24	µA	CK_t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	
IDD8_IN	VDDCA VDDQ	48	48	µA		

Notes: 1. IDD values published are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.
3. These specification values are under IDD2PS condition of the other unselected channel.

Table 4: IDD6 Full and Partial Array Self-Refresh Current
(TC = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V)

Parameter		Symbol	Value	Unit	Condition	Note
Self-Refresh Current +45°C	Full Array	IDD6_1	920	µA	**All devices in self-refresh** CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	1
		IDD6_2	3520	µA		
		IDD6_IN	40	µA		
	1/2 Array	IDD6_1	600	µA		
		IDD6_2	2000	µA		
		IDD6_IN	40	µA		
	1/4 Array	IDD6_1	440	µA		
		IDD6_2	1200	µA		
		IDD6_IN	40	µA		
	1/8 Array	IDD6_1	360	µA		
		IDD6_2	840	µA		
		IDD6_IN	40	µA		
Self-Refresh Current +85°C	Full Array	IDD6_1	3800	µA		
		IDD6_2	12000	µA		
		IDD6_IN	48	µA		
	1/2 Array	IDD6_1	3000	µA		
		IDD6_2	7200	µA		
		IDD6_IN	48	µA		
	1/4 Array	IDD6_1	2600	µA		
		IDD6_2	5200	µA		
		IDD6_IN	48	µA		
	1/8 Array	IDD6_1	2400	µA		
		IDD6_2	4000	µA		
		IDD6_IN	48	µA		

Note: 1. IDD6 85°C is the maximum and IDD6 45°C is typical of the distribution of the arithmetic mean.

2.2 DC Characteristics 2

Table 5: Electrical Characteristics and Operating Conditions
(TC = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V)

Symbol	min	max	Unit	Parameter/Condition	Note
IL	–2	+2	µA	**Input leakage current:** For CA, CKE, CS_n, CK_t, CK_c Any input 0V ≤ VIN ≤ VDDCA (All other pins not under test = 0V)	2
IVREF	–1	+1	µA	**VREF supply leakage current:** VREFDQ = VDDQ/2 or VREFCA = VDDCA/2 (All other pins not under test = 0V)	1

Notes: 1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t, DQS_c output leakage specification. Please refer to the DDR3 Mobile RAM General Functionality and Electrical Condition data sheet (E1853E) for details.

2.3 AC Characteristics

Table 6: AC Characteristics Table*3, *5, *9
(TC = −30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V)

Parameter	Symbol	min max	min tCK*8	1600	1333	Unit
Max. Frequency			—	800	667	MHz
Clock Timing						
Average clock period	tCK(avg)	min	—	1.25	1.50	ns
		max	—	100		ns
Average high pulse width	tCH(avg)	min	—	0.45		tCK(avg)
		max	—	0.55		
Average low pulse width	tCL(avg)	min	—	0.45		tCK(avg)
		max	—	0.55		
Absolute clock period	tCK(abs)	min	—	tCK(avg)min + tJIT(per)min		ns
Absolute clock high pulse width (with allowed jitter)	tCH(abs), allowed	min	—	0.43		tCK(avg)
		max	—	0.57		
Absolute clock low pulse width (with allowed jitter)	tCL(abs), allowed	min	—	0.43		tCK(avg)
		max	—	0.57		
Clock period jitter (with allowed jitter)	tJIT(per), allowed	min	—	−70	−80	ps
		max	—	70	80	
Maximum clock jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	max	—	140	160	ps
Duty cycle jitter (with allowed jitter)	tJIT(duty), allowed	min	—	min((tCH(abs)min − tCH(avg)min), (tCL(abs)min − tCL(avg)min)) × tCK(avg)		ps
		max	—	max((tCH(abs)max − tCH(avg)max), (tCL(abs)max − tCL(avg)max)) × tCK(avg)		
Cumulative error across 2 cycles	tERR(2per), allowed	min	—	−103	−118	ps
		max	—	103	118	
Cumulative error across 3 cycles	tERR(3per), allowed	min	—	−122	−140	ps
		max	—	122	140	
Cumulative error across 4 cycles	tERR(4per), allowed	min	—	−136	−155	ps
		max	—	136	155	
Cumulative error across 5 cycles	tERR(5per), allowed	min	—	−147	−168	ps
		max	—	147	168	
Cumulative error across 6 cycles	tERR(6per), allowed	min	—	−155	−177	ps
		max	—	155	177	
Cumulative error across 7 cycles	tERR(7per), allowed	min	—	−163	−186	ps
		max	—	163	186	
Cumulative error across 8 cycles	tERR(8per), allowed	min	—	−169	−193	ps
		max	—	169	193	
Cumulative error across 9 cycles	tERR(9per), allowed	min	—	−175	−200	ps
		max	—	175	200	
Cumulative error across 10 cycles	tERR(10per), allowed	min	—	−180	−205	ps
		max	—	180	205	
Cumulative error across 11 cycles	tERR(11per), allowed	min	—	−184	−210	ps
		max	—	184	210	
Cumulative error across 12 cycles	tERR(12per), allowed	min	—	−188	−215	ps
		max	—	188	215	

Table 6: AC Characteristics Table*3, *5, *9
(TC = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V) (cont'd)

Parameter	Symbol	min max	min tCK*8	1600	1333	Unit
Cumulative error across n = 13, 14 . . . 19, 20 cycles	tERR(nper), allowed	min	—	tERR(nper),allowed,min = (1 + 0.68ln(n)) × tJIT(per),allowed,min		ps
		max	—	tERR(nper),allowed,max = (1 + 0.68ln(n)) × tJIT(per),allowed,max		
Read Parameters						
DQS output access time from CK_t, CK_c	tDQSCK	min	—	2500		ps
		max	—	5500		
DQSCK delta short*15	tDQSCKDS	max	—	220	265	ps
DQSCK delta medium*16	tDQSCKDM	max	—	511	593	ps
DQSCK delta long*17	tDQSCKDL	max	—	614	733	ps
DQS – DQ skew	tDQSQ	max	—	135	165	ps
DQS output high pulse width	tQSH	min	—	tCH(abs) – 0.05		tCK(avg)
DQS output low pulse width	tQSL	min	—	tCL(abs) – 0.05		tCK(avg)
DQ output hold time from DQS	tQH	min	—	min (tQSH, tQSL)		ps
Read preamble*11, *12	tRPRE	min	—	0.9		tCK(avg)
Read postamble*11, *13	tRPST	min	—	0.3		tCK(avg)
DQS low-Z from clock*11	tLZ(DQS)	min	—	tDQSCK(min) – 300		ps
DQ low-Z from clock*11	tLZ(DQ)	min	—	tDQSCK(min) – 300		ps
DQS high-Z from clock*11	tHZ(DQS)	max	—	tDQSCK(max) – 100		ps
DQ high-Z from clock*11	tHZ(DQ)	max	—	tDQSCK(max) + (1.4 × tDQSQ(max))		ps
Write Parameters*10						
DQ and DM input hold time (VREF based)	tDH	min	—	150	175	ps
DQ and DM input setup time (VREF based)	tDS	min	—	150	175	ps
DQ and DM input pulse width	tDIPW	min	—	0.35		tCK(avg)
Write command to 1st DQS latching transition	tDQSS	min	—	0.75		tCK(avg)
		max	—	1.25		
DQS input high-level width	tDQSH	min	—	0.4		tCK(avg)
DQS input low-level width	tDQSL	min	—	0.4		tCK(avg)
DQS falling edge to CK setup time	tDSS	min	—	0.2		tCK(avg)
DQS falling edge hold time from CK	tDSH	min	—	0.2		tCK(avg)
Write postamble	tWPST	min	—	0.4		tCK(avg)
Write preamble	tWPRE	min	—	0.8		tCK(avg)
CKE Input Parameters						
CKE min. pulse width (high and low pulse width)	tCKE	min	3	7.5		ns
CKE input setup time	tISCKE*1	min	—	0.25		tCK(avg)
CKE input hold time	tIHCKE*2	min	—	0.25		tCK(avg)
Command path disable delay	tCPDED	min	2	2		tCK(avg)
Command Address Input Parameters*10						
Address and control input setup time	tISCA	min	—	150	175	ps
Address and control input hold time	tIHCA	min	—	150	175	ps
CS_n input setup time	tISCS	min	—	270	290	ps
CS_n input hold time	tIHCS	min	—	270	290	ps
Address and control input pulse width	tIPWCA	min	—	0.35		tCK(avg)
CS_n input pulse width	tIPWCS	min	—	0.7		tCK(avg)

Table 6: AC Characteristics Table*3, *5, *9
(TC = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V) (cont'd)

Parameter	Symbol	min max	min tCK*8	1600	1333	Unit
Boot Parameters (10 MHz – 55 MHz)*4, *6, *7						
Clock cycle time	tCKb	max	—	100		ns
		min	—	18		
CKE input setup time	tISCKEb	min	—	2.5		ns
CKE input hold time	tIHCKEb	min	—	2.5		ns
Address & control input setup time	tISb	min	—	1150		ps
Address & control input hold time	tIHb	min	—	1150		ps
DQS output data access time from CK_t, CK_c	tDQSCKb	min	—	2.0		ns
		max	—	10		
Data strobe edge to output data edge	tDQSQb	max	—	1.2		ns
Mode Register Parameters						
Mode register write command period (MRW command to MRW command interval)	tMRW	min	10	10		tCK(avg)
Mode register set command delay (MRW command to non-MRW command interval)	tMRD	min	10	14		ns
Mode register read command period	tMRR	min	4	4		tCK(avg)
Additional time after tXP has expired until MRR command may be issued	tMRRI	min	—	tRCD (min)		ns
DDR3 Mobile RAM Core Parameters						
Read latency	RL	min	6	12	10	tCK(avg)
Write latency	WL	min	3	6	6	tCK(avg)
ACTIVATE to ACTIVATE command period	tRC	min	—	tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)		ns
CKE min. pulse width during self-refresh (low pulse width during self-refresh)	tCKESR	min	3	15		ns
Self-refresh exit to next valid command delay	tXSR	min	2	tRFCab + 10		ns
Exit power-down to next valid command delay	tXP	min	2	7.5		ns
CAS to CAS delay	tCCD	min	4	4		tCK(avg)
Internal read to precharge command delay	tRTP	min	4	7.5		ns
RAS to CAS delay	tRCD	min	3	18		ns
Row precharge time (single bank)	tRPpb	min	3	18		ns
Row precharge time (all banks)	tRPab	min	3	21		ns
Row active time	tRAS	min	3	42		ns
		max	—	70		µs
Write recovery time	tWR	min	3	15		ns
Internal write to read command delay	tWTR	min	4	7.5		ns
Active bank A to active bank B	tRRD	min	2	10		ns
Four bank activate window	tFAW	min	8	50		ns
Minimum deep power-down time	tDPD	min	—	500		µs

Table 6: AC Characteristics Table*3, *5, *9
(TC = −30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V) (cont'd)

Parameter	Symbol	min max	min tCK*8	1600	1333	Unit
Temperature Derating						
DQS output access time from CK_t, CK_c (derated)	tDQSCK	max	—	5620		ps
RAS to CAS delay (derated)	tRCD	min	—	tRCD + 1.875		ns
ACTIVATE to ACTIVATE command period (derated)	tRC	min	—	tRC + 1.875		ns
Row active time (derated)	tRAS	min	—	tRAS + 1.875		ns
Row precharge time (derated)	tRP	min	—	tRP + 1.875		ns
Active bank A to active bank B (derated)	tRRD	min	—	tRRD + 1.875		ns
DDR3 Mobile RAM Refresh Requirement Parameters						
Refresh window	tREFW	max	—	32		ms
Required number of REFRESH commands	R	min	—	8192		
Average time between REFRESH commands (for reference only)	tREFI	max	—	3.9		µs
	tREFIpb	max	—	0.4875		µs
Refresh cycle time	tRFCab	min	—	130		ns
Per bank refresh cycle time	tRFCpb	min	—	60		ns
Burst refresh window = 4 × 8 × tRFCab	tREFBW	min	—	4.16		µs
ZQ Calibration Parameters						
Initialization calibration time	tZQINIT	min	—	1		µs
Long calibration time	tZQCL	min	6	360		ns
Short calibration time	tZQCS	min	6	90		ns
Calibration reset time	tZQRESET	min	3	50		ns
Write Leveling Timings						
First DQS_t, DQS_c edge after write leveling mode is programmed*14	tWLMRD	min	—	40		ns
DQS_t, DQS_c delay after write leveling mode is programmed*14	tWLDQSEN	min	—	25		ns
Write leveling output delay	tWLO	min	—	0		ns
		max	—	20		ns
Write leveling hold time	tWLH	min	—	175	205	ps
Write leveling setup time	tWLS	min	—	175	205	ps
CA Training Timing parameters						
First CA calibration command after CA calibration mode is programmed	tCAMRD	min	—	20		tCK(avg)
First CA calibration command after CKE is low	tCAENT	min	—	10		tCK(avg)
CA calibration exit command after CKE is high	tCAEXT	min	—	10		tCK(avg)
CKE low after CA calibration mode is programmed	tCACKEL	min	—	10		tCK(avg)
CKE high after the last CA calibration results are driven	tCACKEH	min	—	10		tCK(avg)
Data out delay after CA training calibration command is programmed	tADR	max	—	20		ns
MRW CA exit command to DQ tristate	tMRZ	min	—	3		ns
CA calibration command to CA calibration command delay	tCACD	min	—	RU (tADR/tCK) + 2		tCK(avg)

Notes: 1. CKE input setup time is measured from CKE reaching high/low voltage level to CK_t, CK_c crossing.
2. CKE input hold time is measured from CK_t, CK_c crossing to CKE reaching high/low voltage level.
3. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
4. To guarantee device operation before the DDR3 Mobile RAM Device is configured a number of AC boot timing parameters are defined in the Table 6 on page 12. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
5. Measured with 4V/ns differential CK_t/CK_c slew rate and nominal VIX (differential input cross point voltage).
6. The DDR3 Mobile RAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in Section 3 Mode Register Definition on page 18.
7. The output skew parameters are measured with Ron default settings into the reference load.
8. These parameters should be satisfied with both specification, analog (ns) value and min. tCK.
9. All AC timings assume an input slew rate of 2V/ns.
10. Read, Write and input setup and hold values are referenced to VREF.
11. For low-to-high and high-to-low transitions the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 1 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

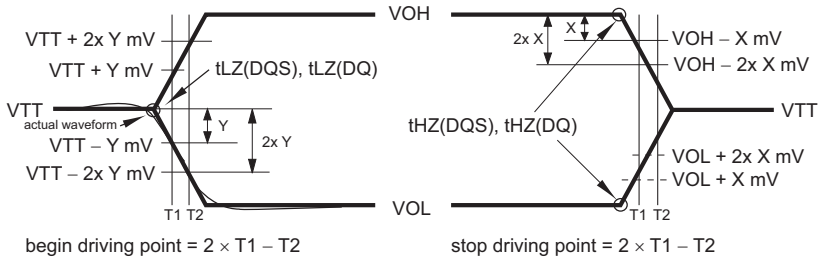

Figure 1: tLZ and tHZ Method for Calculating Transition and Endpoints

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t – DQS_c.

12. Measured from the start driving of DQS_t – DQS_c to the start driving the first rising strobe edge.
13. Measured from the start driving the last falling strobe edge to the stop driving DQS_t – DQS_c.
14. The max values are system dependent.
15. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
16. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
17. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.

2.3.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

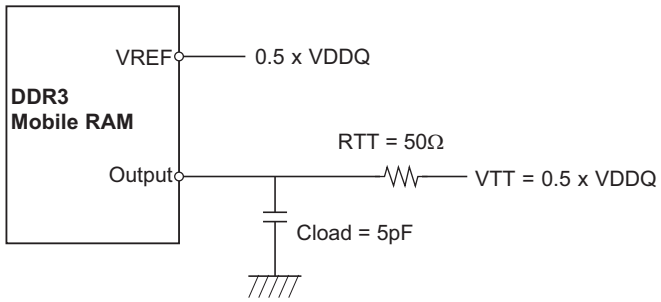

Figure 2: HSUL_12 Driver Output Reference Load for Timing and Slew Rate

Note: 1. All output timing parameter values (like tDQSCK, tDQSQ, tHZ, tRPRE etc) are reported with respect to this reference load. This reference load is also used to report slew rate.

3. Mode Register Definition

Table 7 shows the mode registers for DDR3 Mobile RAM.
Each register is denoted as “R” if it can be read but not written and “W” if it can be written but not read. Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Table 7: Mode Register Assignment

MR#	MA <7:0>	Function	Acce-ss	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Info.	R	RL, nWR, WL Support	WL (Set B) Support	(RFU)	RZQI		(RFU)		DAI	MR#0
1	01H	Device Feature 1	W	nWR (for AP)			(RFU)		BL			MR#1
2	02H	Device Feature 2	W	Write Leveling	WL Select	(RFU)	nWRE	RL & WL				MR#2
3	03H	I/O Config-1	W	(RFU)				DS				MR#3
4	04H	Refresh Rate	R	TUF	(RFU)				Refresh Rate			MR#4
5	05H	Basic Config-1	R	Manufacturer ID								MR#5
6	06H	Basic Config-2	R	Revision ID1 (Die Revision)								MR#6
7	07H	Basic Config-3	R	Revision ID2 (RFU)								MR#7
8	08H	Basic Config-4	R	I/O width		Density				Type		MR#8
9	09H	Test Mode	W	Vendor-Specific Test Mode								
10	0AH	IO Calibration	W	Calibration Code								MR#10
11	0BH	ODT Feature	W	(RFU)					PD control	DQ ODT		MR#11
12:15	0CH~0FH	(Reserved)		(RFU)								
16	10H	PASR_Bank	W	Bank Mask								MR#16
17	11H	PASR_Seg	W	Segment Mask								MR#17
18:19	12H~13H	(Reserved)		(RFU)								
32	20H	DQ Calibration Pattern A	R	See “DQ Calibration”.								MR#32
33:39	21H~27H	(Do Not Use)										
40	28H	DQ Calibration Pattern B	R	See “DQ Calibration”.								MR#40
41	29H	CA Training mode 1 entry	W	1	0	1	0	0	1	0	0	
42	2AH	CA Training mode exit	W	1	0	1	0	1	0	0	0	
43:47	2BH~2FH	(Do Not Use)		(RFU)								
48	30H	CA Training mode 2 entry		1	1	0	0	0	0	0	0	
49:62	31H~3EH	(Reserved)		(RFU)								
63	3FH	Reset	W	X								MR#63
64:126	40H~7EH	(Reserved)		(RFU)								
127	7FH	(Do Not Use)										
128:190	80H~BEH	(Reserved)		(RFU)								
191	BFH	(Do Not Use)										
192:254	C0H~FEH	(Reserved)		(RFU)								
255	FFH	(Do Not Use)										

Notes: 1. RFU bits shall be set to ‘0’ during Mode Register writes.
2. RFU bits shall be read as ‘0’ during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

MR#0_Device Information (MA<7:0> = 00H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL, nWR, WL Support	WL (Set B) Support	(RFU)	RZQI		(RFU)		DAI

OP<0>	DAI (Device Auto-Initialization Status) 0B: DAI complete 1B: DAI still in progress
OP<4:3>	RZQI (Built in Self Test for RZQ Information) 01B: ZQ-pin may connect to VDDCA or float 10B: ZQ-pin may short to GND 11B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)
OP<6>	WL (Set B) Support 0B: DRAM does not support WL (Set B)
OP<7>	RL, nWR, WL Support 0B: DRAM does not support RL = 3, nWR = 3, WL = 1 1B: Reserved

Notes: 1. RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.

2. If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 2), the LPDDR3 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ± 1%).

MR#1_Device Feature 1 (MA<7:0> = 01H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			(RFU)		BL		

OP<2:0>	BL 011B: BL8 All others: Reserved
OP<7:5>	If nWRE (in MR2) = 0 100B: nWR = 6 110B: nWR = 8 (default) 111B: nWR = 9 else (if nWRE = 1) 000B: nWR = 10 001B: nWR = 11 010B: nWR = 12 All others: Reserved

Notes: 1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).
2. The range of nWR is extended using an extra bit (nWRE) in MR2.

Table 8: Burst Sequence by BL, BT, and WC

						Burst Cycle Number and Burst Address Sequence							
C2	**C1**	**C0**	**WC**	**BT**	**BL**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0B	0B	0B	Wrap	Seq	8	0	1	2	3	4	5	6	7
0B	1B	0B				2	3	4	5	6	7	0	1
1B	0B	0B				4	5	6	7	0	1	2	3
1B	1B	0B				6	7	0	1	2	3	4	5
Others			Any	Any		Illegal (Not allowed)							

Notes: 1. C0 input is not present on CA bus. It is implied zero.
2. The burst address represents C2 - C0.

MR#2_Device Feature 2 (MA<7:0> = 02H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Write Leveling	WL Select	(RFU)	nWRE	RL & WL			

OP<3:0>	RL & WL 0100B: RL = 6 / WL = 3 0110B: RL = 8 / WL = 4 (default) 0111B: RL = 9 / WL = 5 1000B: RL = 10 / WL = 6 1001B: RL = 11 / WL = 6 1010B: RL = 12 / WL = 6 All others: Reserved
OP<4>	nWRE 0B: Enable nWR programming ≤ 9 (default) 1B: Enable nWR programming > 9
OP<6>	WL Select 0B: Select WL Set A (default) 1B: Reserved
OP<7>	Write Leveling 0B: Write Leveling Mode disabled (default) 1B: Write Leveling Mode enabled

Table 9: DDR3 Mobile RAM Read and Write Latency

Data Rate [Mbps]	800	1066	1200	1333	1466	1600
tCK [ns]	2.5	1.875	1.67	1.5	1.36	1.25
RL	6	8	9	10	11	12
WL	3	4	5	6	6	6

MR#3_I/O Configuration 1 (MA<7:0> = 03H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

OP<3:0>	DS 0000B: Reserved 0001B: 34.3Ω typ 0010B: 40Ω typ (default) 0011B: 48Ω typ All others: Reserved

MR#4_Device Temperature (MA<7:0> = 04H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				Refresh Rate		

OP<2:0>	Refresh Rate 000B: Low temperature operating limit exceeded 001B: 4 × tREFI, 4 × tREFIpb, 4 × tREFW 010B: 2 × tREFI, 2 × tREFIpb, 2 × tREFW 011B: 1 × tREFI, 1 × tREFIpb, 1 × tREFW(≤ +85°C) 100B: 0.5 × tREFI, 0.5 × tREFIpb, 0.5 × tREFW 101B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, do not de-rate AC timing 110B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, de-rate AC timing 111B: High temperature operating limit exceeded
OP<7>	TUF(Temperature Update Flag) 0B: OP<2:0> value has not changed since last read of MR4. 1B: OP<2:0> value has changed since last read of MR4.

Notes: 1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up. OP<2:0> bits are undefined after power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to "1" if OP2:OP0 has changed at any time since the last read of MR4.
5. DDR3 Mobile RAM will drive OP<6:5> to '0'.
6. Specified operating temperature range and maximum operating temperature are refer to Section 1 Electrical Conditions on page 8. If maximum temperature is 85°C, functionality for over 85°C is not guaranteed.

MR#5_Basic Configuration 1 (MA<7:0> = 05H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

OP<7:0>	Manufacturer ID 00000011B (Elpida)

MR#6_Basic Configuration 2 (MA<7:0> = 06H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1 (Die Revision)							

OP<7:0>	Revision ID1 (Die Revision) 00000000B: A-version

MR#7_Basic Configuration 3 (MA<7:0> = 07H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2 (RFU)							

OP<7:0>	Revision ID2 (RFU) 00000000B: Default Value

MR#8_Basic Configuration 4 (MA<7:0> = 08BH): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

OP<1:0>	Type 11B: S8
OP<5:2>	Density 0110B: 4G
OP<7:6>	I/O width 00B: ×32

MR#10_Calibration (MA<7:0> = 0AH): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

OP<7:0>	Calibration Code FF: Calibration command after initialization AB: Long calibration 56: Short calibration C3: ZQ Reset others: Reserved

Notes: 1. Host processor shall not write MR10 with “Reserved” values.
2. DDR3 Mobile RAM Devices shall ignore calibration command when a “Reserved” value is written into MR10.
3. See AC timing table for the calibration latency.

MR#11_ODT Feature (MA<7:0> = 0BH): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)					PD Control	DQ ODT	

OP<1:0>	DQ ODT 00B : Disabled (Default) 01B : Reserved 10B : RZQ/2 11B : RZQ/1
OP<2>	PD Control (Power-down Control) 0B: ODT disabled by DRAM during power-down 1B: ODT enabled by DRAM during power-down

MR#16_PASR_Bank Mask (MA<7:0> = 010H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

OP<7:0>

Bank Mask
0B: refresh enable to the bank (=unmasked, default)
1B: refresh blocked (=masked)

Bank and OP corresponding table

OP<7:0>	Bank	
	Bank #	Bank Address
OP0	Bank 0	000B
OP1	Bank 1	001B
OP2	Bank 2	010B
OP3	Bank 3	011B
OP4	Bank 4	100B
OP5	Bank 5	101B
OP6	Bank 6	110B
OP7	Bank 7	111B

Note: 1. Each bank can be masked independently by setting each OP value.

MR#17_PASR_Segment Mask (MA<7:0> = 0H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

OP<7:0>

Segment Mask
0B: refresh enable to the segment (=unmasked, default)
1B: refresh blocked (=masked)

Segment and OP corresponding table

OP<7:0>	Segment	
	Segment #	Row Address (R13:11)
OP0	Segment 0	000B
OP1	Segment 1	001B
OP2	Segment 2	010B
OP3	Segment 3	011B
OP4	Segment 4	100B
OP5	Segment 5	101B
OP6	Segment 6	110B
OP7	Segment 7	111B

Note: 1. Each segment can be masked independently by setting each OP value.

MR#32_DQ Calibration Pattern A (MA<7:0> = 20H):

Reads to MR32 return DQ Calibration Pattern “A”.

MR#40_DQ Calibration Pattern B (MA<7:0> = 28H):

Reads to MR40 return DQ Calibration Pattern “B”.

MR#63_Reset (MA<7:0> = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Note: 1. For additional information on MRW RESET.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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