SDR SDRAM Data Sheet Addendum

MT48LC32M4A2 - 8 Meg x 4 x 4 Banks
MT48LC16M8A2 - 4 Meg x 8 x 4 Banks
MT48LC8M16A2 - 2 Meg x 16 x 4 Banks

Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths (BL): 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh modes: Standard and low power (not available on AT devices)
- Auto Refresh
  - 64ms, 4096-cycle refresh (commercial and industrial)
  - 16ms, 4096-cycle refresh (automotive)
- LVTTL-compatible inputs and outputs
- Single 3.3V ±0.3V power supply

Options	Marking
• Configurations	
– 32 Meg x 4 (8 Meg x 4 x 4 banks)[1]	32M4
– 16 Meg x 8 (4 Meg x 8 x 4 banks)	16M8
– 8 Meg x 16 (2 Meg x 16 x 4 banks)	8M16
• Write recovery (^{t}WR)	
– ^{t}WR = 2 CLK	A2
• Plastic package – OCPL[2]	
– 54-pin TSOP II (400 mil)	TG
– 54-pin TSOP II (400 mil) Pb-free	P
– 60-ball TFBGA (8mm x 16mm)	FB[1]
– 60-ball TFBGA (8mm x 16mm) Pb-free	BB[1]
– 54-ball VFBGA (x16 only) (8mm x 8mm)	F4
– 54-ball VFBGA (x16 only) (8mm x 8mm) Pb-free	B4
• Timing – cycle time	
– 7.5ns @ CL = 3 (PC133)	-75[3]
– 7.5ns @ CL = 2 (PC133)	-7E
– 6.0ns @ CL = 3 (x16 only)	-6A
• Special Options	
– Product Longevity Program (PLP)	X
• Self refresh	
– Standard	None
– Low power	L[3]
• Revision	:G/:L
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
– Automotive (–40°C to +105°C)	AT[1]

Notes:
1. Contact Micron for availability.
2. Off-center parting line.
3. Only available on Revision G.

Table 1: Key Timing Parameters

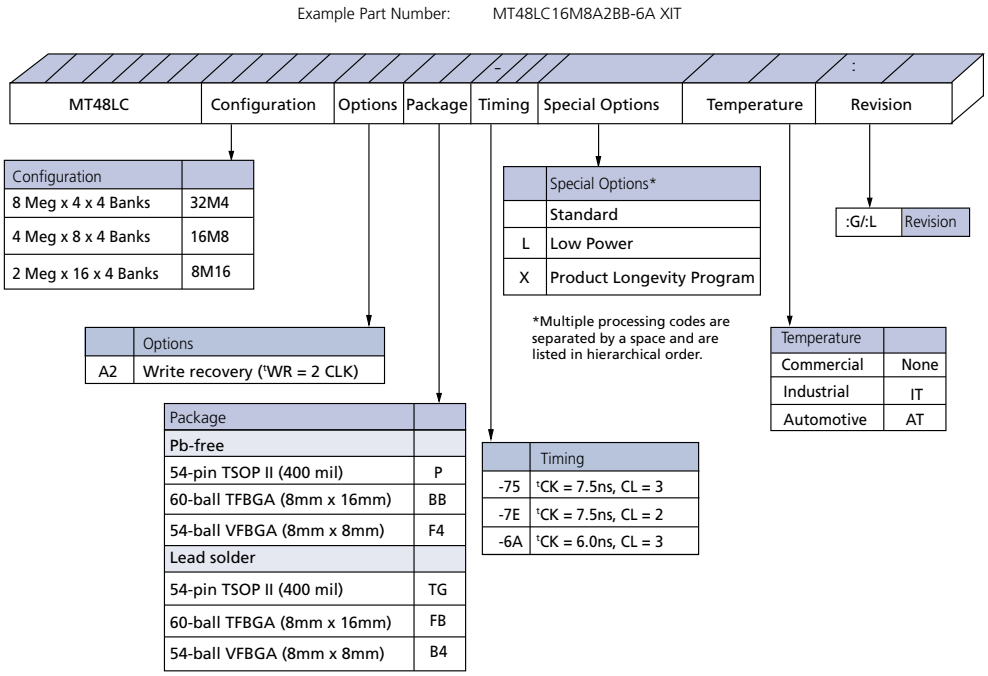
CL = CAS (READ) latency

Speed Grade	Clock Frequency (MHz)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-6A	167	3-3-3	18	18	18
-75	133	3-3-3	20	20	20
-7E	133	2-2-2	15	15	15

Table 2: Address Table

Parameter	32 Meg x 4	16 Meg x 8	8 Meg x 16
Configuration	8 Meg x 4 x 4 banks	4 Meg x 8 x 4 banks	2 Meg x 16 x 4 banks
Refresh count	4K	4K	4K
Row addressing	4K A[11:0]	4K A[11:0]	4K A[11:0]
Bank addressing	4 BA[1:0]	4 BA[1:0]	4 BA[1:0]
Column addressing	2K A[9:0], A11	1K A[9:0]	512 A[8:0]

Figure 1: DDR3L Part Numbers



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Revision History

Rev. A – 03/14

- Initial release based on the 128Mb x4, x8, x16 SDR SDRAM, Rev. U 01/14 data sheet

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.