Customer Service Note

Design Considerations for Bare Die SiPs and MCMs

Introduction

Due to the growth in small form factor solutions, bare die has become an excellent choice for designers who wish to make the most out of their board space. The following questionnaire is provided to help guide potential customers through the various details that need to be taken into account when considering a bare die solution. Customers are encouraged to use this guide to define their system needs and thereby enable Micron to recommend an optimal memory solution.

1. Desired Memory Type

a. ❑ SDRAM ❑ Mobile SDRAM
❑ DDR SDRAM ❑ Mobile DDR SDRAM
❑ DDR2 SDRAM ❑ NAND Flash
❑ DDR3 SDRAM ❑ PSRAM

b. Density: _____

c. Configuration: _____

d. Bus widths: _____

e. Voltage:

Core _____

I/O _____

f. Clock speed: _____

g. Is low power required? _____

1. Active current target _____
2. Power-down target _____
3. Power-down current target _____
4. Self refresh current target

@45°C _____ @70°C _____ @85°C _____

5. Deep power-down current _____

2. Application

a. System application: _____

b. Processor(s) and/or memory controller used: _____

c. Operating voltage of the system: _____

d. Operating temperature range of the system: _____

e. Bond pad requirements of the memory: ❑ Edge ❑ Center
If edge, single- or dual-sided? ❑ Single-Sided ❑ Dual-Sided

f. Expected time frame for:

Customer samples _____

Proto builds _____

Production _____

3. Package and Assembly Considerations

a. Internal assembly or sub contracted assembly? _____
Who may be selected as the subcontractor? _____
Will any post processing, such as RDL be performed?_____

b. Expected die thickness: _____
Will a stress relief process be used? _____
If so, which process?_____

c. Will there be complete access to the Micron® memory at the final package? _____
If no direct access, will there be a bypass mode to the memory?_____

d. Overall size of the final package:
Width _____ Length _____ Height _____

e. If there are multiple memories in this package, will they be sharing a bus? _____

f. Expected number of die per SiP/MCM: _____

g. If this is an SiP, what is the maximum measured junction temperature of the system? _____

h. Die size requirement of the memory (X, Y aspect ratio): _____

i. Where does the Micron memory reside in the stack (that is, bottom, top, etc.)?_____

j. Is an interposer used? _____

k. What other die will be included?
❑ DSPs ❑ CPUs ❑ NOR ❑ PSRAM ❑ LPSDRAM ❑ NAND ❑ Other

4. Test Methodology

a. Will the final package be tested for quality? _____
1. Type of tester used_____
2. Who will be developing the test code?_____
3. Will a BIST engine be employed? _____
Note: Micron memory does not include on-chip BIST circuitry.
4. Minimum and maximum temperatures package will be tested at _____
5. Will the memories be tested separately?_____

b. Will the final package be stressed for reliability? _____
1. If so, how? _____
Voltage range _____
Temperature range _____
Duration of stress _____

5. Quality and Reliability Requirements (refer to Micron technical note TN-00-14)

a. What are your initial "time zero" quality (DPM) expectations? _____

1. How will quality be measured in the final package? _____

b. What are your reliability expectations (extrinsic and intrinsic failure rates? _____

1. For NAND, please list any bit error rate requirements or expectations _____

2. How will reliability be measured? _____

7. Your Company

Name: _____

Title: _____

Division: _____

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Revision History

Rev. B 04/09

- Updated form
- Updated template

Rev. A 10/03

- Initial release