DDR3 Power

Estimates, Affect of Bandwidth, and Comparisons to DDR2

4/12/2007
Agenda

• Understanding datasheet $I_{DD}$ values
• How does bandwidth affect the power?
• How to estimate actual system power
  ‣ Includes two examples
• Power by R/C and comparisons to DDR2
DDR3 Power
Understanding $I_{DD}$ Values
Understanding Datasheet IDD Values

• What good are datasheet IDD values?
  ‣ Datasheet values can tell you what is going on within the DRAM itself
    ▪ For example, the delta between IDD2P(fast) and IDD2P(slow) tells you approximately how much power the DLL circuitry uses
  ‣ Datasheet IDD values can be used to compare the power consumption of like devices
  ‣ Datasheet IDD values can be used to “calculate” system power, but they do not directly indicate system power
Understanding Datasheet IDD Values

• A closer look at IDD values
  ▶ Each of Micron’s DDR3 devices are tested to meet datasheet specifications
    ▪ Datasheet specifications reflect a maximum current which is averaged over an extended period of time
      • \( \text{IDD}_0, \text{IDD}_1 \) – Active Powers
      • \( \text{IDD}_2N, \text{IDD}_2P \) – Power down
      • \( \text{IDD}_3N, \text{IDD}_3P \) – Standby
      • \( \text{IDD}_4R, \text{IDD}_4W \) – READs/WRITEs
      • \( \text{IDD}_5 \) – Refresh
      • \( \text{IDD}_6 \) – Extended power down
      • \( \text{IDD}_7 \) – Bank interleave, READs
  ▶ But what do these specifications mean?
Understanding Datasheet IDD Values

- **IDD0 as defined by the specification**

<table>
<thead>
<tr>
<th>IDD TEST</th>
<th>$I_{DD0}$ Operating Current 0 One Bank Activate -&gt; Precharge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command Inputs</td>
<td>SWITCHING - Table, only exceptions are Activate and Precharge commands; Example of -25E IDD0 pattern: A0DDDDDDDDDDDDDDDDDDDDDDDD0</td>
</tr>
<tr>
<td>Row, Column Addresses</td>
<td>Row addresses SWITCHING, as in Table 5; Address Input A10 must be LOW all the time!</td>
</tr>
<tr>
<td>Bank Addresses</td>
<td>Bank address is fixed (bank 0)</td>
</tr>
<tr>
<td>Data I/O</td>
<td>SWITCHING - Table</td>
</tr>
<tr>
<td>Output Buffer DQ,DQS</td>
<td>Off</td>
</tr>
<tr>
<td>ODT</td>
<td>Disabled</td>
</tr>
<tr>
<td>Burst length</td>
<td>n.a.</td>
</tr>
<tr>
<td>Active banks</td>
<td>Bank 0; ACT-PRE loop</td>
</tr>
<tr>
<td>Idle banks</td>
<td>All other</td>
</tr>
</tbody>
</table>
Understanding Datasheet $\text{IDD}_0$ Values

- $\text{IDD}_0$ as seen on the tester

$\text{IDD}_0$ is the “average” DRAM power while the DRAM is performing repetitive ACTIVE to PRECHARGE commands over an extended period.
Understanding Datasheet IDD Values

• IDD0 in the system?
  ‣ How often does your controller do just an ACTIVE followed by a PRECHARGE to the same bank?
    ▪ If the system does an ACTIVE followed by a PRECHARGE... how often is it to the same bank with the exact conditions as defined by the datasheet?

• The Point: **Datasheet IDD values do NOT reflect the actual system power**
  ‣ To determine the system power, actual DRAM bandwidth must be known
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- **How does bandwidth affect the power?**
- How to estimate actual system power
  - Includes two examples
- Power by R/C and comparisons to DDR2
Bandwidth and Power

- How the DRAM is operated will determine how much power it consumes
  - Key factors that contribute to DRAM power
    - Clock rate and if CKE used
    - Does the system utilize open or closed pages?
      - Closed page mode will consume more power
      - What is the hit rate for open page systems?
    - Number of modules in the system
Bandwidth and Power

• Typically, a faster clock rate will increase the active power proportionally to the increase in the clock frequency
  ‣ If possible, when the DRAM is not active – toggle CKE low
    ▪ Power savings can be substantial
      • For example per the (DDR3-1067) 1Gb datasheet
        Idd3N Active Standby (CKE = hi) = 75mA
        Idd3P Active Standby (CKE = low) = 45mA
        ‣ By dropping CKE low, each DRAM saves 30mA
The largest contributor to the amount of power a DRAM consumes is usually the time between ACTIVATE commands (open or closed pages).

- **Open page mode**
  (Active to Active is determined by page hit rate)

- **Closed Page, with Bank interleaving**
  (Active to Active time = tRRD_{min})
Bandwidth and Power

- Bandwidth distribution between the number of populated slots
  - Typically, the channel bandwidth will be distributed somewhat equally between all ranks in the system
  - Thus, Rank BW = channel BW/# Ranks, more Ranks = less power per Rank (or individual DRAM)

![Diagram showing bandwidth distribution between slots and ranks.](image-url)
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Estimating BW and Power

- Maximum sustainable DRAM bandwidth – as a rule of thumb is about:
  - 60%–70% for closed page accesses
  - 90%–100% for open page accesses
- DRAM bandwidth is usually limited by the channel due to command overhead or possible contention with other DRAMs
  - When there is more than one module in the channel, or if there are dual rank modules in the channel, individual DRAM bandwidth is almost always less
Before memory power is calculated, it is important to know how the controller is accessing the memory

- Open or closed banks
  - If closed banks, does it interleave between internal banks
  - If open banks, what is the page hit rate—how often does it return to the open row for data?

- How many slots will be populated
  - With only a single slot populated, there may be higher power per device than if two slots are populated
  - Will the system utilize SR, DR, x4, or x8 configurations
• What is 100% DRAM bandwidth?
  
  ‣ 100% BW occurs when there is data on all rising and falling clock edges
    
    ▪ For an open page this can be as simple as one Activate command and many back-to-back READ or WRITE commands
    
    ▪ With DDR3 (BL=8), for 100% BW, there must be a READ or WRITE command every four (4) clock cycles (BL/2)

Assumes bank already open, BL=8, CL=6
For a closed page policy, it is more difficult to achieve continuous data.

For example, when interleaving between banks, there must be one ACTIVATE/READ pair or one ACTIVATE/WRITE command for each memory access.

To estimate how many ACTIVATE/READ pairs are required for 100% BW, just divide tRC by 4 clocks.

For example:

- For DDR2-1066, tRC = 48.75ns (26 clocks).
- For 100% BW, there must be an average of 6.5 ACTIVE/READ pairs within the tRC period (26 clocks/4 clocks per Access).
Estimating BW and Power

- To determine the amount of power memory uses:
  1) Determine the sustained channel throughput
  2) Calculate the BW of each individual Rank
     - Closed Page
       • (Total channel BW/number of Ranks in the channel)
     - Open Page
       • (BW of single Rank + standby power of all other Ranks)
  3) Determine the actual DRAM bandwidth (% of 100%)
     - Estimate the % of READs and % of WRITEs
  4) Then use the Micron DDR3 power calculator
     - Also refer to the Micron DDR3 power technical note (TN-47-??)
Estimating BW and Power

• Two DDR3–1066 examples:
  ‣ Estimating power for two (2) DR x4 modules when the channel is running at 5.6GB/s
    ▪ Example 1 (closed page)
      • Assumes BW is disturbed equally between all four ranks
    ▪ Example 2 (open page)
      • Assumes all BW is comes from a single rank, all other ranks are in active standby mode (IDD3N)
Estimating BW and Power

- DDR3–1066 bandwidth example:

Sustainable Channel BW = 5.6GB/s
Assumes:
> 2x READs to WRITEs
Estimating BW and Power

- Three easy steps to determine % DRAM bandwidth (closed page)

**Equate Bandwidth per Slot**

- Bandwidth per slot = 2.8GB
  - (5.6GB/s ÷ 2 slots)

**Find Bandwidth per Rank**

- Bandwidth per Rank = 1.4GB
  - (2.8GB/s ÷ 2 Ranks)

**Calculate % BW for DRAM**

- DDR3-1067 = 8.5GB/s
  - (100% BW of 64 bit bus)

- % of Actual DRAM BW = 16%
  - (1.4GB/s ÷ 8.5GB/s)

- 2x READs = 11%
  - (0.66 x 16%)"
**Estimating BW and Power**

- Estimated module power (closed page)

<table>
<thead>
<tr>
<th># of Die</th>
<th>Channel BW</th>
<th>Slot 0</th>
<th>Slot 1</th>
<th>Per Rank</th>
<th>% Reads</th>
<th>% Writes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DR x4</td>
<td>36</td>
<td>5.6</td>
<td>2.8</td>
<td>2.8</td>
<td>1.4</td>
<td>11%</td>
</tr>
</tbody>
</table>

**Equate Bandwidth per Slot** → **Find Bandwidth per Rank** → **Calculate % BW for DRAM**

<table>
<thead>
<tr>
<th>Power (Watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Per Die</td>
</tr>
<tr>
<td>--------------</td>
</tr>
<tr>
<td>0.214</td>
</tr>
</tbody>
</table>

Use the Micron DDR3 power calculator and do the math...
Steps to determine % DRAM bandwidth (open page)

1. Calculate % of DRAM BW for active rank
2. Calculate power for unused ranks

Estimating BW and Power

- Sustainable Channel BW = 5.6GB/s
  - Assumes:
    - > 2x READs to WRITEs
    - > Open page policy, 100% hit rate
  - (DR x4)

- Bandwidth per slot (100% slot 1, 0% slot 2)
  - 5.6GB/s
  - 0GB/s

- Bandwidth per Rank
  - Slot 1 = 5.6GB Rank 1, 0% Rank 2
  - Slot 2 = 0% for both Ranks

- Rank 1 = 5.6GB/s
- Rank 3 = 0GB/s
- Rank 2 = 0GB/s
- Rank 4 = 0GB/s

- DDR3-1067 = 8.5GB/s
  - (100% BW of 64 hit bus)

- For Active Rank
  - % of Actual DRAM BW = 65%
  - (5.6GB/s ÷ 8.5GB/s)

- x4 DDR3 DRAM

- 2x READs = 43%
- 1x WRITEs = 22%
  - (0.66 x 65%)
  - (0.33 x 65%)

- For Standby Ranks = 0GB/s
  - All standby ranks = ldd3N
### Estimating BW and Power

- **Estimated module power (open page)**

<table>
<thead>
<tr>
<th># of Die per Rank</th>
<th>Channel BW</th>
<th>Slot 0</th>
<th>Slot 1</th>
<th>Per Active Rank</th>
<th>% Reads</th>
<th>% Writes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DR x4</td>
<td>18</td>
<td>5.6</td>
<td>5.6</td>
<td>0</td>
<td>5.6</td>
<td>43%</td>
</tr>
</tbody>
</table>

#### Calculate % of DRAM BW for active rank

<table>
<thead>
<tr>
<th></th>
<th>Per Active Rank</th>
<th>* Per Standby Rank</th>
<th>Memory Total</th>
<th>Logic</th>
<th>Per Slot</th>
<th>Channel Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slot 1</td>
<td>0.533</td>
<td>0.113</td>
<td>11.62</td>
<td>1.90</td>
<td>13.52</td>
<td>19.47</td>
</tr>
<tr>
<td>Slot 2</td>
<td>N/A</td>
<td>0.113</td>
<td>4.05</td>
<td>1.90</td>
<td>5.95</td>
<td>19.47</td>
</tr>
</tbody>
</table>

* Assumes standby Rank is in Idd3N mode

Use the Micron DDR3 power calculator and do the math...
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  › Includes two examples

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Reflects a channel bandwidth of 65% of maximum, distributed evenly between all ranks with a single slot populated. Power reflects expected datasheet values, and estimated Register/PLL power.
Reflects a channel bandwidth of 65% of maximum, distributed evenly between all ranks with a single slot populated. Power reflects expected datasheet values, and estimated Register/PLL power.

DDR3-1333 is slightly higher than DDR2-800 and about 2.2W more than DDR2-667

DDR3-1067 is about equal to DDR-667