DDR3 Advantages
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- Lower power
- Higher speed
- Master reset
- More performance
- Larger densities
- Modules for all applications
Lower Power

- Supply voltage reduced from 1.8V to 1.5V
  - ~30% reduction in power due to supply voltage alone
- Lower I/O buffer power
  - 34 ohm driver vs. 18 ohm driver

Source: Micron
Designed for High-Speed Signaling

- Improved pinout
- Fly-by architecture
- READ and WRITE leveling
- Data calibration through ZQ resistor
- Dynamic ODT for improved WRITE signaling
- 2 DIMMs/channel at DDR3 frequencies
Improved Pinout

- Improved power delivery
  - More power and ground balls
- Improved signal quality
  - Improved signal integrity
  - Improved power and ground distribution
  - Improved signal referencing
- Fully populated ball grid
  - Improved mechanical reliability
- Improved D/Q array
  - Less D/Q skew
  - Tighter D/Q timing
Improved Module Layout

• Fly-by architecture for C/A, control, clocks
  ‣ Improved signal integrity for high speeds
  ‣ On-module termination
  ‣ Used on UDIMM, SODIMM, RDIMM

• Not used on DDR2 – not needed at lower frequencies
READ/WRITE Leveling

- Allows for controller to determine the time delta for data command to data output of each DRAM (byte lane)
  - Enables controller to capture data for each byte lane
  - Enables controller to adjust receiver timing per byte lane
Master Reset

- Improved system stability
  - Eliminates unknown start-up states
  - Known initialization and recovery state
    - Cold boot reset
    - Warm boot reset
    - Removes controller burden to ensure no illegal commands
Increased Peak Performance

- **2X the bandwidth of DDR2**
  - Component per pin
    - 800 MT/s to 1600 MT/s
  - Bus bandwidth
    - 6400 MT/s to 12,800 MT/s
- **8 banks vs. 4 banks**
  - More open banks for back-to-back access
  - Hide turnaround time
  - Hide tRP
DDR3 Market

- DDR3 market dynamics
  - 512Mb/1Gb crossover
  - 1Gb/2Gb crossover
  - DDR3 life from 2007 through 2014

Source: Micron Marketing
### DDR3 Ramp

**Table:**

<table>
<thead>
<tr>
<th></th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
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<tbody>
<tr>
<td>DDR</td>
<td>14%</td>
<td>3%</td>
<td>2%</td>
<td>1%</td>
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<tr>
<td>DDR2</td>
<td>83%</td>
<td>78%</td>
<td>64%</td>
<td>33%</td>
</tr>
<tr>
<td>DDR3</td>
<td>3%</td>
<td>19%</td>
<td>34%</td>
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**Source:** Micron Marketing
## Maximum* Module Density

<table>
<thead>
<tr>
<th>Component Density</th>
<th>256Mb</th>
<th>512Mb</th>
<th>1Gb</th>
<th>2Gb</th>
<th>4Gb</th>
<th>8Gb</th>
<th>4Gb</th>
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<td>4 GB</td>
<td></td>
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*Maximum density requires stacked and/or high component count planar versions of modules

** 4Gb is a JEDEC standard; Micron has no plans to support it
## DDR3 Modules for All Applications

<table>
<thead>
<tr>
<th>Unbuffered DIMM</th>
<th>1H07</th>
<th>2H07</th>
<th>1H08</th>
<th>2H08</th>
<th>1H09</th>
<th>2H09</th>
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<td>Unbuffered DIMM</td>
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<td>Notebook</td>
<td>Small Outline DIMM</td>
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<td>Server</td>
<td>Registered DIMM</td>
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<td>Fully Buffered DIMM</td>
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<td>Networking</td>
<td>Very Low Profile DIMM</td>
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</table>
Summary

• DDR3 provides more bandwidth at lower power
• Package, pinout, and signaling improvements for higher-speed operation
• Master reset for improved system stability
• Larger densities
• Modules for all applications