VFBGA

**Product Status**

packages have an abbreviated part mark that is different from the part number.

- **Dimensions in millimeters**
  - LF PoP (168-ball SDP, 12 x 12 x 0.75) BF VFBGA (60-ball SDP, 8 x 9 x 1)

**Component Configuration**

- Blank = 50mil I/O
- C = Separate I/O

**Device Versions**

Alphanumeric character(s) specified by individual data sheet

- K = Kilobits
- A = 1.2V
- V = 2.5V
- HC = 1.8V
- JN CF FBGA (60-ball, 8 x 10)  -107  933 MHz with tRC (MIN) 10ns
- KL PoP (168-ball SDP & DDP, 12x12x .8) LV PoP (216-ball DDP 12 x 12 x .75)

**Mobile Package Codes**

- CV CY FBGA (84-ball, 60-ball, 8 x 12.2)
- TC F D2 50% pin spacing

**DDR SDRAM**

- D2 = 2-die stack (LPDDR)  DDR
- D4 = 4-die stack (LPDDR, LPDDR2, LPDDR3, LPDDR4)
- D6 = 6-die stack (LPDDR)

**Operating Temperatures**

- 41 = DDR3 SDRAM
- 40 = DDR4 SDRAM

**Voltage**

- A = 1.2V
- V = 2.5V
- KU PoP (216-ball 3DP, 12 x 12 x .9) NH PoP (272-ball DDP/QDP 15 x 15 x 0.7)

**Special Options**

- A = Automotive
- G = Graphics
- L = Low power
- M = Reduced standly
- X = Product Longevity Program [Automotive & Industrial only]

**Access/Acyclic Time**

- 107  933 MHz with tRC (MIN) 8ns
- 125 800 MHz with tRC (MIN) 8ns
- 250 1000 MHz with tRC (MIN) 10ns
- 500 1500 MHz with tRC (MIN) 5ns

**Die Revision Designator**

**Production Status**

ES = Engineering sample

**Mobile LPSDR**

- KH PoP (216-ball 3DP, 12 x 12 x .9) KH PoP (216-ball 3DP, 12 x 12 x 0.75)
- KL PoP (168-ball SDP & DDP, 12x12x .8) LV PoP (216-ball DDP 12 x 12 x .75)

**FCC**

- 125 800 MHz with tRC (MIN) 10ns
- 125 800 MHz with tRC (MIN) 10ns
- 107 933 MHz with tRC (MIN) 10ns
- 125 800 MHz with tRC (MIN) 10ns
- 15 667 MHz 10-10-10
- 18 533 MHz with tRC (MIN) 10ns

**Die Short**

- 25 400 MHz with tRC (MIN) 4ns
- 25 400 MHz with tRC (MIN) 4ns
- 18 533 MHz with tRC (MIN) 10ns

**Die Package**

- 125 800 MHz with tRC (MIN) 10ns
- 125 800 MHz with tRC (MIN) 10ns
- 107 933 MHz with tRC (MIN) 10ns
- 107 933 MHz with tRC (MIN) 10ns
- 107 933 MHz with tRC (MIN) 10ns

**Data Rate**

- 500 1500 MHz with tRC (MIN) 5ns
- 500 1500 MHz with tRC (MIN) 5ns
- 500 1500 MHz with tRC (MIN) 5ns